**ON Semiconductor** 

Is Now

# Onsemi

To learn more about onsemi<sup>™</sup>, please visit our website at <u>www.onsemi.com</u>

onsemi and ONSEMI. and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product factures, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using onsemi products, including compliance with all laws, regulations and asfety requirements or standards, regardless of any support or applications information provided by onsemi. "Typical" parameters which may be provided in onsemi data sheets and/or by customer's technical experts. onsemi products and actal performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. onsemi products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use onsemi products for any such unintended or unauthorized application, Buyer shall indemnify and hold onsemi and its officers, employees, subsidiari

# MOSFET Transient Junction Temperature Under Repetitive UIS/Short-Circuit Conditions



## **ON Semiconductor®**

http://onsemi.com

# **APPLICATION NOTE**

#### INTRODUCTION

Power MOSFET is a popular choice of switching device in a wide range of electronics. Majority of their applications is to control and regulate the high power section of a system. With technology advancements and cost competitiveness requirements, power MOSFETs are on die-shrinking trend. Smaller and cheaper MOSFETs are replacing the old bulky with additional improvements in efficiency and noise. For the same on-resistance, trench technology requires less than half the size of a planar counter part. For most markets, the improvements in efficiency and cost allow smaller packages and better profit margins. For some, the reduction in die size poses a potential hazardous problem in their systems. Several hazardous examples are discussed and methods to evaluate them are explained in details.

Thermal performance is an important parameter in most MOSFET applications such as dc/dc converters, uninterruptible power supplies (UPS), and motor control. In UPS or motor applications, MOSFETs are required to handle sudden surges of high current under fault conditions. Without a method of measuring the transient junction temperature of power devices, engineers are left to speculate about thermal failures. Junction temperature (Figure 1) is internal to the power device. Thermal measurements using thermocouples or IR cameras can only measure the average case temperature. Knowing the power applied to the power devices will allow peak junction temperature to be derived. The peak MOSFET junction temperature will determine the failure point. MOSFET datasheets' maximum values are derated for rated temperature range and do not represent any real significance in actual applications. Knowing the peak transient junction temperature will help in predicting the MOSFET survival time in fault conditions.



Figure 1. Junction and Case Temperature Transient for a Typical TO–220

Most repetitive avalanche energy ratings ( $E_{AR}$ ) are based on infinite heat sink model (fixed case temperature). In real applications, repetitive high power events contribute to a significant increase in average power dissipation and raise the case temperature. Also, the values are derived using rated temperature with the assumption of a rectangular power pulse. Under repetitive avalanche situations, the power pulses are triangular with respect to time.

#### PROCEDURES

There are several ways to create the transient temperature rise curves under high power dissipation conditions.

- 1. Spice modeling with the Cauer/Foster model
  - including the heat sink/PCB
- 2. Spreadsheet modeling thermal networks

Both methods require tools/software and information, which are not always available, and significant processing time to extend to the steady state. A simplified method uses the existing MOSFET datasheet's thermal impedance graph

- 1. Using a single event (single UIS, single short circuit cycle) transient temperature
- 2. Average temperature rise model
- 3. Superimpose both to have the overall transient behavior

The profile of a high power single event needs to be known to calculate the junction temperature rise. For unclamped inductive switching (UIS), the power pulse will have the shape of a right triangle.

Single event power loss = Psingle Normal operation power loss = P<sub>d-avg</sub>

24 V battery, 5 µH parasitic inductance, 5 kHz frequency, 10% duty cycle, 60 V TO-220 MOSFET NTP5863N.



Figure 2. Motor Drill Under UIS Fault

In single MOSFET trigger applications, such as the drill flyback circuit (Figure 2), repetitive UIS can occur. In this case, the MOSFET can be overstressed when the drill jams. The number of cycles or time the drill will survive in this situation is critical. When the drill is jammed, the current ramps up with parasitic inductance in the on-time. This stores energy in the parasitic inductor and can cause the MOSFET to avalanche during the off-time. The avalanche breakdown voltage (V<sub>BD</sub>) will increase by 30% from its rated voltage due to heating of the device. Finally, the drain voltage of the MOSFET will settle to battery voltage (V<sub>Battery</sub>) before another cycle begins. The avalanche time  $\left(t_{AV}\right)$  is the duration required for  $I_{peak}$  to reduce to zero during the off-time.

#### **Repetitive UIS Power Derivations (Figure 3)**

$$I_{peak} = \frac{V_{Battery} * D}{(F_{SW} * L)} = \frac{24 * 0.1}{5000 * 5 * 10^{-6}} = 96 \text{ A}$$

$$V_{BD} = - 1.3 * 60 \text{ V} * 1.1 = 86 \text{ V}^{+}$$

$$t_{AV} = L * I_{peak} / (V_{BD} - V_{Battery}) = 7.74 \text{ } \mu\text{s}$$
Energy Dissipated =  $\frac{1}{2} * V_{BD} * I_{peak} * t_{AV}$ 

$$= \frac{1}{2} * L * I_{peak} ^{2} * \frac{V_{BD}}{V_{BD} - V_{Battery}}$$

$$= 32 \text{ mJ}$$

The peak temperature rise for different power pulse shapes will differ. Using the method described by R. Stout [1], the transient temperature rise for a single event can be evaluated.

Average transient temperature =  $R_{thjA}(t) * (P_{single} + P_{d-avg})$ Overall transient = average transient + single event

#### **EXAMPLE: MOTOR DRILL REPETITIVE UIS CONDITIONS**

Power<sub>uis</sub> = 32 mJ \* 5000 Hz = 160 W

 $Power_{normal} = 10 W$  (assumed)

†60 V MOSFETs' have ~10% higher breakdown than rated and 30% increase due to avalanche heating.



Figure 3. UIS Waveform

#### Single UIS Temperature Transient (Figure 4)

Refer to the MOSFET's thermal response graph (Figure 5) and fit a line equation at the fast transient (up to atleast  $t_{AV}$ ). It follows a sqrt(t) relationship [2]. The die thickness determines the period of fast transient sqrt(t) relationship is valid [3] ( $\sim$ 500 µs for TO-220 package).

Fitted Fast 
$$R_{thjA} = K * \sqrt{t} = 13 * \sqrt{t} \left[\frac{°C}{W}\right]$$
 (Figure 5)

This fitted fast transient RthiA will help in creating a single UIS temperature transient. The power pulse of a single UIS event is transformed into 10 even discrete power pulses for the following equation and its detail derivation in Appendix I.

Temperature Rise =  $R_{thi}(t) * Power(t)$ 

Po = Peak Power = 86 V \* 96 A = 8256 W

$$T_{\text{rise}@n} \frac{t_{\text{av}}}{10} = \begin{cases} \frac{P_{0} * K}{10} * \sqrt{\frac{t_{\text{AV}}}{10}} * \left[ 10 * \sqrt{n} - \sum_{1}^{n} \sqrt{n} \right], & n \le 10 \\ \frac{P_{0} * K}{10} * \sqrt{\frac{t_{\text{AV}}}{10}} * \left[ 10 * \sqrt{n} - \sum_{n=9}^{n} \sqrt{n} \right], & n > 10 \end{cases}$$

Utilizing the above formula and plotting the transients, the peak temperature occurred at n = 5.



#### **Overall Repetitive UIS Temperature Transient**

The thermal impedance with a heatsink (Figure 5),  $R_{thjA}(t)$ , included can be obtained. The heat capacity of the material,  $C_{HS}$ , and thermal resistance,  $R_{HS}$ , provided by the heatsink vendor forms a  $R_{HS}$  C<sub>HS</sub> network to the  $R_{thjC}(t)$  [4].

$$R_{thjA}(t) = R_{thjC}(t) + R_{HS}^{*} \left(1 - e^{-t/(R_{HS}^{*C}_{HS})}\right)$$

NTP5863N Thermal Impedance 10 Single Pulse + Heatsink R(t) (°C/W) 0.1 0.0 Fast Transient Fitted <sup>–</sup>13 \* √<del>ī</del> 0.001 0.000001 0.0001 0.01 100 10k PULSE TIME (s) Figure 5. Thermal Impedance of NTP5863N

Average Temperature Transient

$$= R_{thjA}(t) * (Power_{UIS} + Power_{d-avg})$$
$$= R_{thiA}(t) * 170 W$$

Peak Single UIS Temperature =  $max(T_{rise}in t_{AV})$ 

Peak Junction Temperature Transient (Figure 6)

The peak temperature equation above ignored the transient between high power events. For most cases, it should be a good approximation. But for a much lower frequency where time between high power events are long, temperature transient between them might be needed.

Example Junction Temperature at 10 s + 10  $\mu$ s

$$T_{\text{rise}} @(10 + 10\mu)s = R_{\text{thjA}}(10s) * 170 \text{ W} + \frac{8256 * 13}{10} \\ * \sqrt{\frac{7.74E-6}{10}} \Big[ 10 * \sqrt{13} - \sqrt{4} - \sqrt{5} - \sqrt{6} - \sqrt{7} - \sqrt{8} - \sqrt{9} \\ - \sqrt{10} - \sqrt{11} - \sqrt{12} - \sqrt{13} \Big] = 1.25 * 170 + 69.4 \\ = 281.9^{\circ} \text{ C}$$

10 µs is approximate n = 13 (10 µs / (7.74 µs / 10) = -13)

The temperature calculations above are referring to the rise in temperature. Adding the ambient temperature will obtain the actual junction temperature.



Figure 6. Overall Transient Temperature rise

#### INTRINSIC TEMPERATURE

The silicon MOSFET junction temperature is limited by its intrinsic temperature. It was shown that localized hot spot (mesoplasma) occurs at intrinsic temperature [5].

With a theoretical intrinsic temperature of  $370^{\circ}$ C, NTP5863 will fail in around 10 seconds ( $T_{rise} = 345^{\circ}$ C)

Surface-mount device datasheet provides thermal

impedance  $(R_{thjA})$  graph of a specific copper area, thickness and PCB material.  $R_{thjA}$  will change significantly with different PCB conditions. ON Semiconductor does provide

different R<sub>thjA</sub> graphs for different copper area and thickness upon request; even so, these curves may not take into

account all significant variables of the actual customer

application [6].

under the previously specified repetitive UIS condition. If the peak temperature never reaches intrinsic temperature under steady state, the device will survive the repetitive avalanches assuming failure mode is thermal.

#### SURFACE-MOUNT DEVICES



#### **REPETITIVE SHORT-CIRCUIT**

In all UPS short circuit testing at the output is a requirement. With the output shorted (secondary side of transformer), the primary side H-bridge/Push-Pull MOSFETs turn on with little impedance passing huge current repetitively. This will incur tremendous power loss in a short period of time until the microcontroller shuts down. Low on-resistance devices are commonly used so power loss will be dominated by the switching losses.

#### Single Short-circuit Temperature Transient

The procedure for getting the peak temperature transient under short-circuit conditions is similar to the previous repetitive UIS example. Except that the power pulse for short-circuit,  $t_{SC}$ , will be different. Therefore, the previous  $T_{rise}$  equation (for right angle power pulse) will not apply. The exact power pulse depends on circuit implementations like MOSFETs' saturation current and parasitic inductances.

Fitted Fast  $R_{thiA} = K^* \sqrt{t} = 17^* \sqrt{t}$  [7]

An example of temperature rise for an isosceles triangle and rectangle power pulse is shown (Figure 8). The isosceles triangle was divided into 10 equal powers and 20 time divisions for deriving its discrete temperature transient formula below.

$$\begin{split} &\mathsf{T}_{\mathsf{rise}(\mathsf{rectangular})} \\ &= \left\{ \begin{array}{ll} \mathsf{P}_\mathsf{o} * \mathsf{K} * \sqrt{t} & t \leq t_{\mathsf{SC}} \\ \mathsf{P}_\mathsf{o} * \mathsf{K} * \left[ \sqrt{t} - \sqrt{t - t_{\mathsf{SC}}} \right] & t > t_{\mathsf{SC}} \end{array} \right. \end{split}$$

 $\mathsf{T}_{\mathsf{rise}(\mathsf{iso.\ triangle})}@\mathsf{n}\frac{\mathsf{t}_{SC}}{20}$ 

$$= \begin{cases} \frac{P_{o} * K}{10} * \sqrt{\frac{t_{SC}}{20}} * \sum_{1}^{n} \sqrt{n}, & n \leq 10 \\ \frac{P_{o} * K}{10} * \sqrt{\frac{t_{SC}}{20}} * \left[ \sum_{n=9}^{n} \sqrt{n} - \sum_{1}^{n-10} \sqrt{n-10} \right] \\ 10 < n \leq 20 \\ \frac{P_{o} * K}{10} * \sqrt{\frac{t_{SC}}{20}} * \left[ \sum_{n=9}^{n} \sqrt{n} - \sum_{n=19}^{n-10} \sqrt{n-10} \right] \\ n > 20 \end{cases}$$



Figure 8. Transient Temperature for Different Power Pulse Shapes

#### Example: Buck Converter Shoot-thru

Buck converter, 300 kHz frequency, 100 ns short-circuit with rectangular or triangular power pulse, 40 V SO–8 FL MOSFET NTP5863N, 2 W  $P_{d-avg}$ , Ambient = 25°C, assumed failure junction temperature of 370°C

Peak Single Short-circuit Temperature<sub>rect</sub> = 17°C

 $power_{rect} = 3200 \text{ W} * 100 \text{ ns} * 300 \text{ kHz} + 2 \text{ W} = 98 \text{ W}$ 

$$R_{\text{thjA}} = \frac{370^{\circ}\text{C} - 17^{\circ}\text{C} - 25^{\circ}\text{C}}{98 \text{ W}} = 3.35 \frac{^{\circ}\text{C}}{\text{W}}$$

Device reaches 3.4°C/W and failure temperature in 0.1sec with specified rectangular power pulse.

#### 2. Triangle Short-circuit Power Pulse

Peak Single Short-circuit Temperaturetri = 9°C

Power<sub>tri</sub> = 
$$\frac{1}{2}$$
\* 3200 W \* 100 ns \* 300 kHz + 2 W = 50 W  
R<sub>thjA</sub> =  $\frac{370^{\circ}C - 9^{\circ}C - 25^{\circ}C}{50 W} = 6.7 \frac{^{\circ}C}{W}$ 

Device reaches 6.7°C/W and failure temperature in 0.5 s with specified triangular power pulse.

#### **OTHER IMPLICATIONS**

The intrinsic temperature varies with MOSFET technologies. For different breakdown voltage MOSFETs, they will have different doping concentrations. A higher breakdown voltage usually has lower silicon doping than lower breakdown. A higher doping concentration results in a higher intrinsic temperature. Mounting conditions have a huge influence on the thermal resistance [7]. When thermal pads or grease are used, their thermal resistance should be included. Due to their negligible heat capacity compared to the heatsink, additional RC thermal network is not needed but simply adding the resistance to R<sub>HS</sub>.

#### CONCLUSION

The K term used in the fast transient also reveals the relative die size in the same MOSFET package family.

$$K = \frac{2}{A\sqrt{\rho\pi kc}} [2]$$

where:

A = Area

 $\varrho = Density$ 

K = Thermal Conductivity

c = Thermal Capacity of Silicon

It is obvious that the fast transient ( $<\sim 1$  ms) depends on the die size, slow transient ( $\sim 1$  ms to 1 s) depends on the package type, and steady state transient depends on the mounting conditions. If it is in the same package, a larger die will have a smaller peak junction temperature in the fast transient and a smaller steady state temperature rise for the same power pulse.

Although a lower thermal impedance indicates a better thermal capability, the breakdown voltage variations between different devices affect the UIS pulse time and energy. Also a larger die will have larger input capacitances resulting in higher switching power loss. Therefore, calculation of power losses and deriving the transient junction temperature will be a better determining factor in MOSFET selection.

This method is also applicable to other power devices through knowing the power pulse transient and average power applied.

# AND9042/D

# REFERENCES

- [1] "How to Generate Square Wave, Constant Duty Cycle, Transient Response Curves", <u>http://www.onsemi.com/pub\_link/Collateral/AND821</u> <u>9-D.PDF</u>
- [2] D.L. Blackburn, "Power MOSFET Failure Revisited", Proc. 1988 IEEE Power Electronics Specialists Conference, pp 681–688, April 1988
- [3] "Semiconductor Package Thermal Characterization", <u>http://www.onsemi.com/pub\_link/Collateral/AND821</u> <u>5-D.PDF</u>
- [4] "Thermal RC Ladder Networks", <u>http://www.onsemi.com/pub\_link/Collateral/AND822</u> <u>1-D.PDF</u>

- [5] A. C. English, "Physical Investigation of the Mesoplasma in Silicon", *IEEE Trans. Elec. Dev. Vol-13(8/9), pp. 662–667, Aug 1966*
- [6] "Predicting the Effect of Circuit Boards ON Semiconductor Package Thermal Performance", <u>http://www.onsemi.com/pub\_link/Collateral/AND822</u> <u>2-D.PDF</u>
- [7] "Mounting Considerations For Power Semiconductors", <u>http://www.onsemi.com/pub\_link/Collateral/AN1040</u> <u>-D.PDF</u>

## AND9042/D

# APPENDIX I. THERMAL RESPONSE TRANSFORMATION



Figure 9. Right Angle Triangle Power Pulse Decomposed and Constructed From Superposition to Form Thermal and Power Response

Approximate temperature rise at each time intervals,

...

$$\begin{split} t_{1} &: P_{0} * K * \sqrt{t_{1}} - \frac{P_{0}}{10} * K * \sqrt{t_{1}} \\ t_{2} &: P_{0} * K * \sqrt{t_{2}} - \left(\frac{P_{0}}{10} * K * \sqrt{t_{2}}\right) - \left(\frac{P_{0}}{10} * K * \sqrt{t_{2} - t_{1}}\right) \\ t_{3} &: P_{0} * K * \sqrt{t_{3}} - \left(\frac{P_{0}}{10} * K * \sqrt{t_{3}}\right) - \left(\frac{P_{0}}{10} * K * \sqrt{t_{3} - t_{1}}\right) - \left(\frac{P_{0}}{10} * K * \sqrt{t_{3} - t_{2}}\right) \\ \cdots \\ t_{10} &: P_{0} * K * \sqrt{t_{10}} - \left(\frac{P_{0}}{10} * K * \sqrt{t_{10}}\right) - \left(\frac{P_{0}}{10} * K * \sqrt{t_{10} - t_{1}}\right) - \left(\frac{P_{0}}{10} * K * \sqrt{t_{10} - t_{2}}\right) - \left(\frac{P_{0}}{10} * K * \sqrt{t_{10} - t_{3}}\right) \\ - \left(\frac{P_{0}}{10} * K * \sqrt{t_{10} - t_{4}}\right) - \left(\frac{P_{0}}{10} * K * \sqrt{t_{10} - t_{5}}\right) - \left(\frac{P_{0}}{10} * K * \sqrt{t_{10} - t_{6}}\right) - \left(\frac{P_{0}}{10} * K * \sqrt{t_{10} - t_{7}}\right) - \left(\frac{P_{0}}{10} * K * \sqrt{t_{10} - t_{8}}\right) \\ - \left(\frac{P_{0}}{10} * K * \sqrt{t_{10} - t_{9}}\right) \end{split}$$

#### AND9042/D

$$\begin{split} t_{21} &: \ \mathsf{P}_{o}^{*} \,\mathsf{K}^{*} \,\sqrt{t_{21}} - \left(\frac{\mathsf{P}_{o}}{10}^{*} \,\mathsf{K}^{*} \,\sqrt{t_{21}}\right) - \left(\frac{\mathsf{P}_{o}}{10}^{*} \,\mathsf{K}^{*} \,\sqrt{t_{21} - t_{1}}\right) - \left(\frac{\mathsf{P}_{o}}{10}^{*} \,\mathsf{K}^{*} \,\sqrt{t_{21} - t_{2}}\right) - \left(\frac{\mathsf{P}_{o}}{10}^{*} \,\mathsf{K}^{*} \,\sqrt{t_{21} - t_{3}}\right) \\ &- \left(\frac{\mathsf{P}_{o}}{10}^{*} \,\mathsf{K}^{*} \,\sqrt{t_{21} - t_{4}}\right) - \left(\frac{\mathsf{P}_{o}}{10}^{*} \,\mathsf{K}^{*} \,\sqrt{t_{21} - t_{5}}\right) - \left(\frac{\mathsf{P}_{o}}{10}^{*} \,\mathsf{K}^{*} \,\sqrt{t_{21} - t_{6}}\right) - \left(\frac{\mathsf{P}_{o}}{10}^{*} \,\mathsf{K}^{*} \,\sqrt{t_{21} - t_{7}}\right) - \left(\frac{\mathsf{P}_{o}}{10}^{*} \,\mathsf{K}^{*} \,\sqrt{t_{21} - t_{7}}\right) \\ &- \left(\frac{\mathsf{P}_{o}}{10}^{*} \,\mathsf{K}^{*} \,\sqrt{t_{21} - t_{9}}\right) \end{split}$$

For 10 division of right angle triangle power pulse,

$$t_{1} = \frac{t_{AV}}{10}, t_{10} - t_{4} = 6 * \frac{t_{AV}}{10}, t_{21} - t_{7} = 14 * \frac{t_{AV}}{10} \dots$$

$$T_{rise} @ n \frac{t_{AV}}{10} = \begin{cases} P_{0} * K \sqrt{\frac{n * t_{AV}}{10}} - \sum_{1}^{n} \left( \frac{P_{0} * K}{10} \sqrt{\frac{n * t_{AV}}{10}} \right) \rightarrow \frac{P_{0} * K}{10} * \sqrt{\frac{t_{AV}}{10}} * \left( 10 * \sqrt{n} - \sum_{1}^{n} \sqrt{n} \right), & n \le 10 \end{cases}$$

$$\int \frac{P_{o} * K}{10} * \sqrt{\frac{t_{AV}}{10}} * \left[ 10 * \sqrt{n} - \sum_{n=9}^{n} \sqrt{n} \right], \qquad n > 10$$

For higher resolutions, 30 divisions formula will be:

$$T_{\text{rise}} \otimes n \frac{t_{\text{AV}}}{30} = \begin{cases} \frac{P_0 * K}{30} * \sqrt{\frac{t_{\text{AV}}}{30}} * \left[ 30 * \sqrt{n} - \sum_{1}^{n} \sqrt{n} \right], & n \le 30 \end{cases}$$

$$\frac{P_{o} * K}{30} \left[ \frac{P_{o} * K}{30} * \sqrt{\frac{t_{AV}}{30}} * \left[ 30 * \sqrt{n} - \sum_{n=29}^{n} \sqrt{n} \right], \qquad n > 30 \right]$$

**ON Semiconductor** and **())** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemic.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC products are not designed, intended, or authorized for use as components insystems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and easonable attorney fees arising out of, directly or indirectly, or indirectly, any datin of personal injury or death associated with such unintended or unauthorized use, even it such claim alleges that SCILLC and is not for resale in any manner.

#### PUBLICATION ORDERING INFORMATION

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada Email: orderlit@onsemi.com N. American Technical Support: 800–282–9855 Toll Free USA/Canada Europe, Middle East and Africa Technical Support:

Phone: 421 33 790 2910 Japan Customer Focus Center Phone: 81–3–5817–1050 ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative