AND9035/D

BELASIGNA® 250 and 300 for Low-Bandwidth Applications

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APPLICATION NOTE

Introduction

This application note describes the use of BELASIGNA 250 and BELASIGNA 300 in low−bandwidth applications. The intended audience is portable electronics equipment designers who are working with low−bandwidth signals, typically under 200 Hz. An example application is the analysis of biological signals for monitoring and/or diagnosis. The goal of this document is to provide customers with information about the performance of these products in low−bandwidth situations, as well as information on how best to configure the devices for use in such environments.

This application note also describes the expected performance of BELASIGNA 250 and BELASIGNA 300 in terms of analog−to−digital conversion noise and accuracy, system current consumption and MIPS required in a typical application, and to suggest configuration and implementation strategies to ensure the best possible performance in these categories.

ANALOG TO DIGITAL CONVERSION

Analog to Digital Converters

BELASIGNA 250 and BELASIGNA 300 provide 16−bit, 8x over−sampled analog−to−digital converters with configurable sampling frequencies from 1.27 kHz to 60 kHz. BELASIGNA 250 offers two ADCs, while BELASIGNA 300 offers four.

The above sampling frequency range does not extend low enough for the low−bandwidth applications discussed in this application note. However, down−sampling can be performed in software on the DSP itself. Down−sampling by a factor of N typically consists of two steps:

- Low−pass filtering: limits the bandwidth of the incoming signal to prevent aliasing in the down-sampled signal
- Decimation: reduces the data rate by selecting every Nth sample and discarding the remaining samples

This process can be repeated (multi−stage decimation) to achieve a higher overall decimation rate.

On BELASIGNA 250 a custom down−sampling routine can be written for the RCore DSP, while on BELASIGNA 300 there are multiple options available. Such decimation can be efficiently performed by the HEAR Accelerator signal processing engine. While the standard library of HEAR functions does not include a specific down−sampling module, there are several filtering modules available (both FIR and IIR) that can be used to low−pass filter the incoming data, as well as vector copy modules that can be used to extract to the down−sampled stream from the filtered data. Alternatively, a custom decimation filter function can be written for execution on the CFX core. Finally, ON Semiconductor provides an optimized HEAR module that combines FIR filtering and deimation to achieve greater efficiency.

In the example described below, the system is configured for 16 kHz sampling. A custom HEAR module performs multi−stage decimation using low−pass FIR filters. The first stage decimates by a factor of 10 and the second by a factor of 4 to achieve an overall decimation factor of 40. The signal bandwidth is effectively reduced from 8 kHz to 200 Hz.

ADC Calibration on BELASIGNA 300

The operational amplifiers (op−amps) used in the input stage of BELASIGNA 300 produce DC offsets that are accumulated in the closed loop of the sigma−delta ADC. This results in undesirable spikes and/or bumps in the noise floor. The value of the DC offset is configurable through a dedicated register. To prepare BELASIGNA 300 for near−DC sampling the ADC must be properly calibrated. Typically this would be performed at the production line, with calibration values stored in an SPI EEPROM attached to BELASIGNA 300. These values are then loaded at boot time. Each ADC can be calibrated for each of the 8 available pre−amplifier gain settings. However, it is more efficient to calibrate the ADCs for only those pre−amplifier gain settings used in the application. For more information on ADC calibration for BELASIGNA 300, see Reference 1.

Input Stage Noise

In many low−bandwidth applications, the signals involved are of a very low level – often less than 10 mV. Input stage noise is thus an important consideration for the system designer. Noise characteristics of the input stages of BELASIGNA 250 and BELASIGNA 300 are given below.

Of interest are zero−input peak−to−peak and RMS noise in two bandwidth regions: 0.5 to 40 Hz and 0.5 to 150 Hz.

Measurements were made by acquiring a buffer containing 30 seconds of digital audio samples through the PCM interface at a sampling frequency of 16 kHz. The analog input pin was grounded through a 0.1 nF capacitor. The data was band−pass filtered offline (using MATLAB®) to the bandwidths mentioned above. The peak−to−peak noise is calculated as the maximum positive sample minus the minimum negative sample, and the RMS noise value is calculated as:

$$X_{RMS} = \sqrt{\frac{x_0^{\,2} + x_1^{\,2} + ... + x_{N-1}^2}{N}}$$

All values are in μV and are input−referred.

Table 1. RMS NOISE (μV, input referred) IN THE 0.5 − 150 Hz REGION

	BELASIGNA 300					BELASIGNA 250			
	Chopper Clock Divisor					Chopper Clock Divisor			
	Off	0x1	0x5	0x9	0xF	Off	0x1	0x5	0x9
0 dB	31.7	31.1	30.1	31.3	30.7	8.1	10.0	10.1	10.1
12 dB	8.1	7.8	7.8	7.9	8.0	3.1	2.8	3.1	3.1
18 dB	4.5	4.0	4.0	4.1	3.9	1.7	1.5	1.5	1.6
24 dB	3.0	2.3	2.2	2.0	2.1	1.0	0.9	0.8	0.9
30 dB	2.1	1.2	1.2	1.2	1.3	0.7	0.8	0.5	0.5

Table 2. PEAK−PEAK NOISE (μV, input referred) IN THE 0.5 − 150 Hz REGION

	BELASIGNA 300					BELASIGNA 250			
	Chopper Clock Divisor					Chopper Clock Divisor			
	Off	0x1	0x5	0x9	0xF	Off	0x1	0x5	0x9
0 dB	198.8	203.8	200.4	200.0	198.4	99.5	97.5	90.1	87.2
12 dB	54.1	53.4	50.0	51.3	50.9	27.2	23.6	29.4	28.5
18 dB	28.7	27.4	26.3	26.4	26.0	16.8	14.7	12.2	14.3
24 dB	19.0	15.1	13.9	13.6	13.7	9.0	8.0	7.2	7.2
30 dB	14.8	8.0	8.3	8.0	8.6	5.5	6.4	4.9	7.0

Table 3. RMS NOISE (μV, input referred) IN THE 0.5 − 40 Hz REGION

	BELASIGNA 300					BELASIGNA 250			
	Chopper Clock Divisor					Chopper Clock Divisor			
	Off	0x1	0x5	0x9	0xF	Off	0x1	0x5	0x9
0 dB	25.1	25.2	24.0	25.3	24.9	6.0	6.3	6.5	6.4
12 dB	6.6	6.2	6.3	6.3	6.4	2.2	1.7	2.1	2.1
18 dB	3.6	3.3	3.2	3.3	3.3	1.2	0.9	0.9	1.0
24 dB	2.6	2.0	1.8	1.7	1.7	0.7	0.5	0.5	0.6
30 dB	1.7	1.0	1.1	1.1	1.2	0.5	0.5	0.3	0.3

Table 4. PEAK−PEAK NOISE (μV, input referred) IN THE 0.5 − 40 Hz REGION

	BELASIGNA 300					BELASIGNA 250			
	Chopper Clock Divisor					Chopper Clock Divisor			
	Off	0x1	0x5	0x9	0xF	Off	0x1	0x5	0x9
0 dB	142.3	150.0	145.2	140.7	141.7	69.3	51.4	59.3	60.0
12 dB	37.8	36.4	35.0	37.4	37.4	19.2	15.3	16.4	19.2
18 dB	20.9	20.3	18.3	19.2	18.5	12.1	6.7	7.7	10.3

Table 4. PEAK−PEAK NOISE (μV, input referred) IN THE 0.5 − 40 Hz REGION (continued)

	BELASIGNA 300					BELASIGNA 250			
	Chopper Clock Divisor					Chopper Clock Divisor			
	Off	0x1	0x5	0x9	0xF	Off	0x1	0x5	0x9
24 dB	14.5	11.2	10.4	9.7	9.5	6.3	4.5	3.6	4.0
30 dB	10.7	6.3	6.1	6.4	7.0	3.7	4.1	2.7	2.7

Chopper Stabilization

When examining low−bandwidth signals close to DC, 1/f noise typically dominate the noise floor. In op−amps a modulation scheme called chopper stabilization can be used to reduce the effects of 1/f noise. This technique involves modulating the op−amp's input signal to a higher frequency where 1/f noise is minimal, and then demodulating following amplification. In BELASIGNA 250 chopper stabilization is implemented in the pre−amplifiers and the ADCs, and in BELASIGNA 300 chopper stabilization is implemented only in the pre−amplifiers. The chopper carrier signal is a square wave with a configurable frequency. The recommended chopper frequency is an integer multiple of the sampling frequency, typically 8x the sampling frequency.

On BELASIGNA 250, the chopper clock is derived from the Master Clock signal (MCLK) with the frequency defined by a 4−bit integer divisor. To enable the chopper, set bit 6 of analog control register A_ADC_CUR_CTRL (0x1C). The configuration value (CHOPPER_CTRL) used to define the frequency is stored in bits (7:4) of analog control register A_CLK_CTRL (0x11). The default CHOPPER_CTRL value of 0 disables chopper stabilization. For non−zero values, the chopper clock frequency is defined as:

$$\text{Chopper Frequency} = \frac{\text{MCLK}}{(\text{CHOPPER\_CTRL} + 1)}$$

On BELASIGNA 300, the chopper clock is derived from SLOW_CLK with the frequency defined by a 4−bit integer divisor. The configuration value (CHOPPER_CLK) used to define the frequency is stored in bits (19:16) of analog control register A_INPUT_CTRL (0xE141). The default CHOPPER_CLK value of 0 disables chopper stabilization. For non−zero values, the chopper clock frequency is defined as:

$$\text{Chopper Frequency} = \frac{\text{SLOW\_CLK}}{(\text{CHOPPER\_CTRL} + 1)}$$

Example: On BELASIGNA 300, if the SLOW_CLK frequency is set to 1.28 MHz and the sampling frequency is 16 kHz, the recommended chopper frequency is 8 * 16 kHz = 128 kHz. To obtain this frequency, SLOW_CLK must be divided by 10. Thus, the appropriate value for CHOPPER_CLK is 9.

Conversion Accuracy

Another important factor in ADC performance is conversion accuracy, often specified by differential nonlinearity (DNL). Nominal static DNL values for BELASIGNA 250 and BELASIGNA 300 ADCs with a 16 kHz sampling frequency are given in Table 5 below.

Table 5. STATIC DIFFERENTIAL NONLINEARITY

	BELASIGNA 250	BELASIGNA 300
DNL	±0.4 LSBs	±0.4 LSBs

NOTE: Typical, not qualified.

Conversion accuracy measurements were made using the histogram method with a sine wave input signal [2]. The sine wave signal was generated with a function generator (Audio Precision) and the digital converted values were transmitted to a PC through the Serial Peripheral Interface (SPI) port, collected with an SPI analyzer device. MATLAB was used to perform the final calculation to obtain DNL values. Since the ADCs provide 16−bit samples for both systems, the number of samples collected was in excess of 70 million to ensure DNL error of less than 0.1 LSB and a 99% level of confidence.

Example Low−Bandwidth Application

BELASIGNA 300 in a Cardiac Monitoring Application

To demonstrate the capabilities of BELASIGNA 300 in a low−bandwidth application, a simple cardiac monitoring application is presented. In this application, ECG lead signals (right arm (RA), left arm (LA), left leg (LL) and chest (V2)) are input to BELASIGNA 300 and the DSP is responsible for down−sampling (by a factor of 40), calculation of differential signals I (LA – RA), II (LL – RA) and III (LL − LA), heart rate detection, and for the transmission of this data back to a host PC through the I^2C interface.

System Configuration

In this application, the four input signals are capacitively coupled to the BELASIGNA 300 analog input pins. A buffer is used to match impedances between the sensor output and

the BELASIGNA 300 input stage. The front end used for this application is shown in Figure 1.

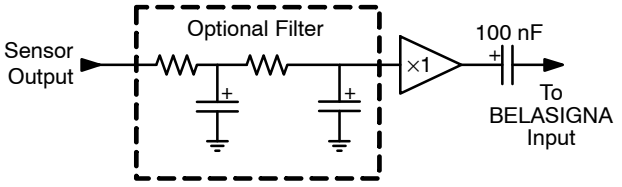

Figure 1. Front End for Cardiac Monitor Application

In this application, the op−amps are configured for unity gain and are used for buffering the input signals. The 100 nF coupling capacitor gives a cut−off frequency of ~3 Hz. The beat detection in this algorithm is based on the R peak in the ECG waveform. For a more detailed view of the ECG waveform a larger capacitor (and thus a lower cut−off frequency) is recommended.

While the ADCs provide effective anti−alias filtering through an 8x oversampled architecture, additional low−pass filtering can be performed in the analog domain to further improve performance. A sample low−pass filter is shown in the diagram above.

The BELASIGNA 300 system is configured by the application firmware as described in Table 6.

Table 6. SYSTEM CONFIGURATION

System Clock	2.56 MHz (internal oscillator, calibrated)
SLOW_CLK	1.28 MHz
Sampling Rate	16 kHz
ADC Chopper Rate	128 kHz
Preamp gain	30 dB

Four FIFOs are used in this application. The four input signals are combined into two interleaved signals and routed to two stereo FIFOs. The remaining two FIFOs are used to store the down−sampled versions of these signals.

Signal Processing

Processing in this application includes the following steps:

- Down−sampling by a factor of 10
- Down−sampling by a further factor of 4
- Differential signal calculation
- Feature computation
- Beat detection

The signal processing is split between the CFX and the HEAR, with the HEAR performing the filtering and decimation and the CFX performing feature computation and beat detection. The processing in this application is block−based, meaning the DSP waits for one full “block” of ADC samples and then processes all data samples in the block. This process is then repeated. The block size is determined by the down−sampling factors. With a block size of 160 samples per channel, the first stage of down−sampling (by a factor of 10) results in 16 new samples at an intermediate sampling rate of 1.6 kHz. A further stage of down−sampling by a factor of 4 results in four new samples at the target sampling rate of 400 Hz. All down−sampling is performed by the HEAR Accelerator. The HEAR uses a custom microcode module to efficiently perform stereo FIR low−pass filtering and decimation. The first stage uses a 16−tap filter while the second uses a 128−tap filter.

Upon completion of the decimation, the CFX begins feature computation using the V2 lead’s decimated signal. A simple derivative−based method is used for peak detection [3]. The steps performed in feature computation include:

- Calculation of first−order derivative:

$$y_0[n] = x[n] - x[n-1]$$

- Calculation of second−order derivative:

$$y_1[n] = y_0[n] - y_0[n-1]$$

- Linear combination of the magnitude of derivatives:

$$y_2[n] = 2 \times \left(w_0 \times |y_0[n]| + w_1 \times |y_1[n]|\right)$$

Where $w_0 = 0.65$ and $w_1 = 0.55$.

- Moving average filter:

$$y_3[n] = \text{sum}\left(y_2[n], \ldots, y_2[n-M+1]\right)/M$$

Where $M = 8$.

- Finally, set a binary variable to indicate peaks:

$$y_4[n] = \begin{cases} 1, \text{if } y_3[n] > \text{threshold} \\ 0, \text{otherwise} \end{cases}$$

The remaining processing consists of examining the y_4 signal to determine the likelihood of a peak. If a peak is detected, the peak−to−peak time interval is estimated as the number of blocks that have elapsed since the previously detected peak. If this block count falls within a valid range, corresponding to 40 to 200 beats per minute (BPM), then the block count is added to a circular buffer. The average block count in this buffer is calculated, and converted to a BPM value.

For this application a low−level I^2C slave handler was included to facilitate communications with a host PC. The PC communicates with BELASIGNA 300 through the ON Semiconductor Communications Accelerator Adaptor (CAA) to request BPM information, as well as up to three sets of decimated signal data (any three of the RA, LA, LL, V2, I, II and III signals).

Using an ECG patient simulator device, BELASIGNA 300 is able to perform heart rate detection with input signals down to 0.5 mV.

Resource Requirements

BELASIGNA 300 is capable of running the sample application described above with a current consumption of 511 μA at 1.8 V. In terms of CPU usage, BELASIGNA 300

requires roughly 3000 cycles to perform down−sampling and beat detection per block. At 16 kHz sampling and a block size of 160 samples, there are 0.01 seconds per block. With a 2.56 MHz system clock, this equates to 25600 available cycles per block. Thus, in this application BELASIGNA 300 is utilizing 12% of the CPU for the detection algorithm. Some additional CPU usage is required for communications with the host PC.

Design Considerations

When designing BELASIGNA 250 or BELASIGNA 300 into a low−bandwidth application, there are several considerations, both hardware and software, that must be taken into account.

Software Considerations

- Current consumption can be minimized by reducing the overall system clock. When designing the firmware for a given application, the best approach is to split processing between the CFX and HEAR as evenly as possible, maximizing parallel processing. By doing so, the system clock can be drastically reduced compared to a serial processing approach.
- When dividing processing between the CFX and the HEAR, it is advisable to allocate typical signal processing functionality to the HEAR while the CFX handles application−level processing and signal processing functions which are not available in the standard HEAR library.
- When performing down−sampling with a high decimation rate (e.g. 40, as seen in the above example), it is more efficient to split the decimation into multiple stages. While this approach may make the resulting firmware somewhat more complicated, it provides significant savings of both processing time and memory by replacing one large monolithic filter with multiple smaller filters with a lower overall number of taps.

Hardware Considerations

- System current consumption can be reduced by using the internal oscillator rather than an external oscillator. A properly calibrated internal oscillator offers accuracy to within ± 1% of the calibrated frequency. For higher accuracy, an external oscillator should be used.
- BELASIGNA 250 and BELASIGNA 300 can operate with a supply voltage down to 1 V, further reducing system current consumption.
- Input impedance for analog inputs is nominally 500 kΩ for both BELASIGNA 250 and BELASIGNA 300. When selecting decoupling capacitors, a value should be chosen such that the corner frequency is low enough to pass all desired frequencies.
- High impedances are frequently encountered when working with biological sensors. To deal with impedance mismatches between sensors and BELASIGNA's input stage, it is recommended that front end buffers be used.
- The ADCs in BELASIGNA 300 should always be calibrated to ensure best performance.

References

1. *"ADC Offset Calibration of the BELASIGNA® 300 Series"* (AND8341/D), ON Semiconductor, 2008.
2. W. Kester, *"The Data Conversion Handbook"*, Newnes, 2005.
3. B−U Köhler, C. Hennig and R. Orglmeister, *"The Principles of Software QRS Detection"*, IEEE Engineering in Medicine and Biology, 2002.

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