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How to Maintain USB Signal Integrity when Adding ESD Protection

ON Semiconductor®

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APPLICATION NOTE

Introduction

The Universal Serial Bus (USB) has become a popular feature of PCs, cell phones and other electronic devices. USB makes data transfer between electronic devices faster and easier. USB 2.0 transfers data at up to 480 Mbps. At these data rates, any small amount of capacitance added will cause disturbances to the data signals. Designers are left with the challenge of finding ESD protection solutions that can protect these sensitive lines without adding signal degrading capacitance. This document will discuss USB 2.0 and evaluate the importance of low capacitance ESD protection devices with the use of eye diagrams.

USB 2.0 Overview

Universal Serial Bus (USB) is a serial bus standard. USB was designed to allow peripherals to be connected using a single standardized interface socket and to improve plug-and-play capabilities by allowing devices to be connected and disconnected without rebooting the computer (hot swapping). USB has four lines, two data lines (D+ and D−) which are data transfer lines, bus voltage (Vbus) and ground (GND). Below are guidelines required for USB 2.0:

- 1.5 Mbit/s, 12 Mbit/s, 480 Mbit/s Supported
- USB Controller is Required to Control the Bus and Data Transfer
- Cable Up to 5 m
- Up to 127 Devices Supported
- Power Supply to External Devices is 500 mA/5 V (max)
- Full Compatibility with USB 1.1 Devices

Eye Diagrams

Eye diagrams, also known as eye patterns, are representations of digital signals that provide minimum and maximum voltage levels as well as signal jitter. With eye diagrams one can measure signal rise time, fall time, undershoot, overshoot, and jitter. Line capacitance and bandwidth effects of data transmission can also be evaluated. The eye diagram will expose any issues in USB data lines.

An eye diagram is produced by repetitively sampling a digital signal on an oscilloscope's vertical axis, while triggering the horizontal sweep with the data rate. The resulting pattern looks like an eye, as shown in Figure 1. The larger the eye the better the data signal integrity. Acceptable signal qualities are often defined with the use of a mask. The mask consists of a hexagon in the middle of the eye and rectangles above and below the eye. If the measured traces cross the mask boundaries the signal quality is considered unacceptable. USB 2.0 signal mask specifications are provided by the USB Implementers Forum, www.usb.org (USB Specification Rev. 2.0, Section 7.1.2.2). Figure 1 displays an eye diagram with details of the critical points.

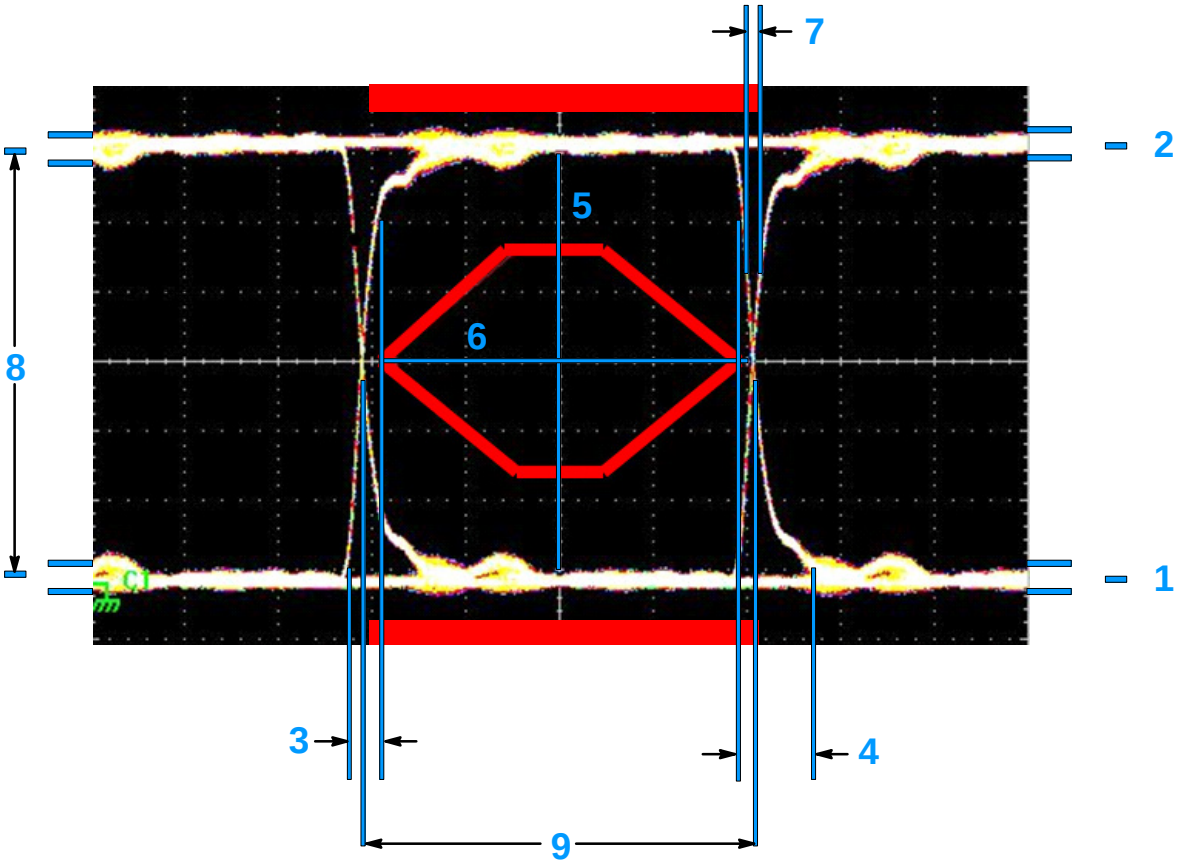

Figure 1. USB 2.0 Eye Diagram

1. Zero Level: Measure of the mean value of the logical 0.
2. One Level: Measure of the mean value of the logical 1.
3. Rise Time: Measure of the transition time of the data from the 10% level to the 90% level on the upward slope.
4. Fall Time: Measure of the transition time of the data from the 90% level to the 10% level on the downward slope.
5. Eye Height: Measure of the vertical opening. Determine eye closure due to noise.
6. Eye Width: Measure of the horizontal opening. Determine influence of jitter on the eye opening transitions and the logic 1 level histogram mean value.
7. Deterministic Jitter: Deviation of a transition from its ideal time caused by reflections relative to other transitions.
8. Eye Amplitude: Difference between the logic 0 level and the logic 1 level histogram mean value.
9. Bit Rate: Inverse of bit period.

Measured Results

For the study below a USB 2.0 high speed signal was used at 480 Mb/s. The eye diagrams of three different protection devices with different ranges of capacitance were measured and compared with the USB 2.0 mask. A board without a device was also evaluated for comparison and reference. Comparing the eye diagrams with different protection devices with the diagram for no protection device demonstrates the extent of signal degradation caused by the protection device. It should be noted that this article only takes into account the capacitance of the ESD protection diode and its effect on the USB 2.0 high speed signal. In a practical design there would also be capacitance added by other components on the line or by the board itself. Figure 2 illustrates the test signal without a protection device.

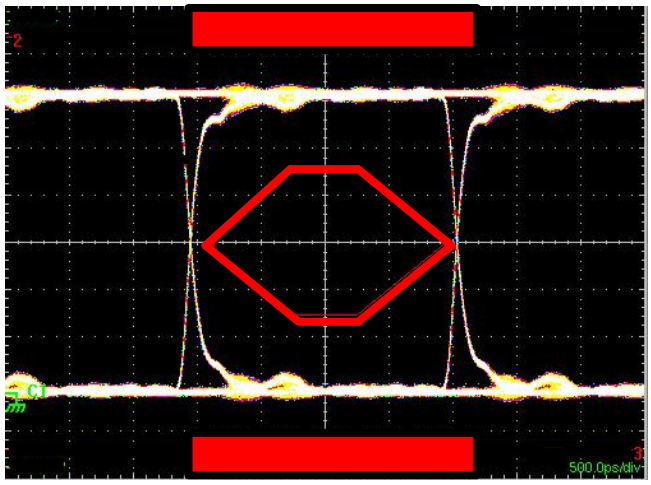

Figure 2. Test Without Device

This test signal represents a pure USB 2.0 high speed signal with no distortion since there is no capacitance added to the line.

Figure 3 illustrates an eye diagram of the USB 2.0 high speed signal with ON Semiconductor's ultra-low capacitance ESD device, ESD9L with 0.5 pF of capacitance. The eye diagram reveals no major changes or differences in the data signal. The mean value logical 1 and logic 0 and the rise and fall times operate with no interruptions. The ESD9L has no negligible adverse effect to the integrity of the data signal since the capacitance value is so low. This gives a designer an ESD protection option that will offer maximum flexibility with the capacitance budget to add other components.

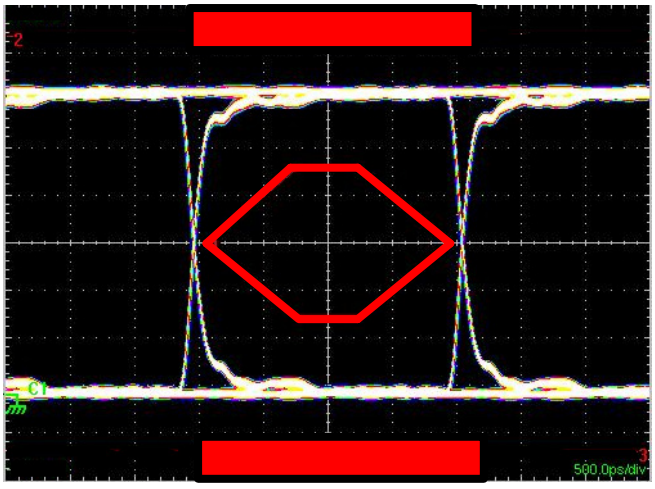

Figure 3. ESD9L 0.5 pF ESD Device

The next test uses the ON Semiconductor ESD9C5.0ST5G with 6 pF of capacitance, Figure 4. With the added capacitance a noticeable degradation of the signals is observed from the eye diagram compared to the test with no added capacitance. The main degradation is the increase in rise and fall times. The pattern in Figure 4 looks acceptable but shows that the protection device is consuming a significant portion of the capacitance budget. In most designs there would be a significant amount of added capacitance from other components on the design that would degrade the signal further making this 6 pF ESD protection device unacceptable at this data rate.

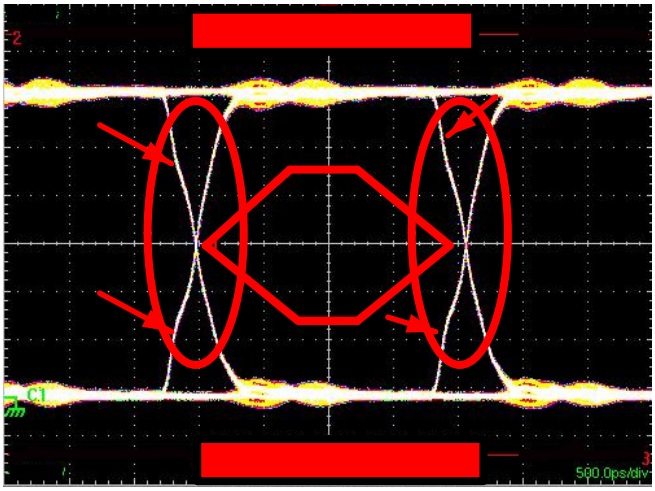

Figure 4. ESD9C 6 pF Device, the Arrows Highlight the Distortation Starting to Appear with Higher Capacitance Device

The final test is done with ON Semiconductor's ESD9X5.0ST5G with 65 pF capacitance (Figure 5). The eye diagram shows significant signal degradation; rise and fall times show significant increases. The use of a high capacitance device introduces distortion and degradation to the high speed data line. The signal traces cross the USB 2.0 mask, demonstrating that this protection device can not be used in a USB 2.0 application.

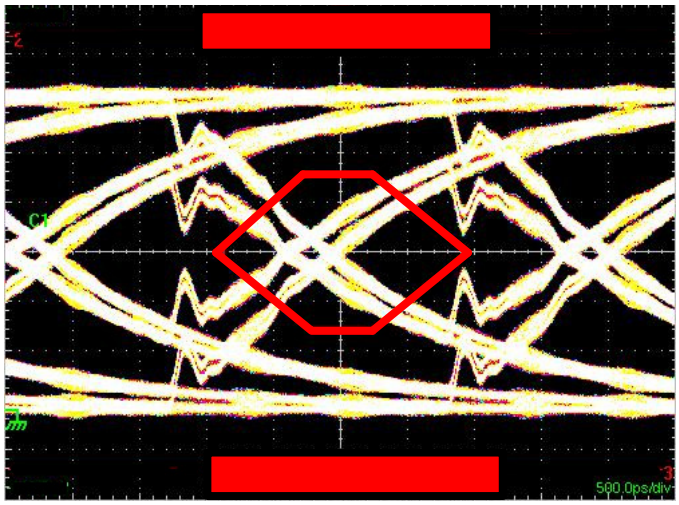

Figure 5. High Capacitance Device

Summary

The ultra low capacitance (0.5 pF) of the ESD9L offers the best design option of the semiconductor devices to use for USB 2.0 high speed applications. The eye diagram study above shows the ESD9L has extremely low impact on the logic levels and no distortion to the rise and fall times. This option will leave the designer with some budget for other components on the line to add capacitance while maintaining the signal integrity of the USB line.

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