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Theory of Operation of V2 Controllers

with Emphasis on Applications using MLCC's for Output Filtering

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APPLICATION NOTE

Every pulse width modulated controller configures basic control elements such that when connected to the feedback signal of a power converter, sufficient loop gain and bandwidth is available to regulate the voltage set point against line and load variations. These control elements include error amplifier, pulse width modulator, ramp, voltage reference, clock, latch and drive for the power switch, which may or may not be integrated within the controller. The arrangement of these elements differentiates a voltage mode, or a current mode controller from a V2 device.

Figure 1 shows a basic voltage mode controller.

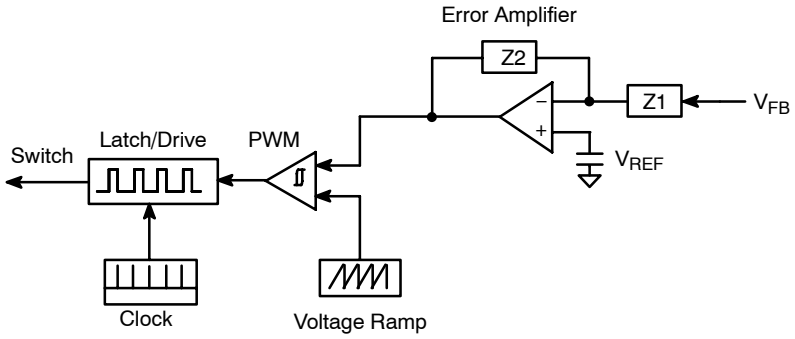

Figure 1. V Mode Control

The converter's feedback signal is compared against a voltage reference and an error signal is generated at the output of the voltage amplifier. This error signal is fed to one input of a PWM, the other input being a voltage ramp of fixed amplitude, generated from an internal clock. The internal clock sets the latch to initiate a drive cycle. When the error signal intersects the ramp, the PWM resets the latch and the power switch is turned off. A small change in output voltage, corresponding to input line or output load variations, results in a change in the error voltage relative to the ramp. This in turn causes the modulator's duty cycle D to change to regulate the output voltage.

Figure 2 highlights the elements of a current mode controller.

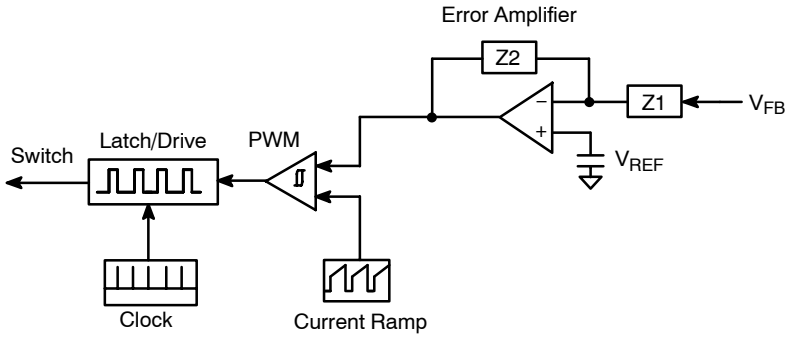

Figure 2. I Mode Control

In this control implementation, the error signal is again generated by a voltage amplifier comparing the feedback signal with a reference voltage at its inputs. As in voltage mode control, this signal is fed to one input of the PWM. However in current mode control, the second input is derived not from a fixed ramp but from the current flowing in the power switch. When the peak of the current ramp intersects the error signal, the power switch cycle is terminated. Hence when a change is detected by the outer voltage loop, the programmed current in the inner loop is modified up or down to correct the deviation.

Figure 3 illustrates the basic architecture of a V2 controller.

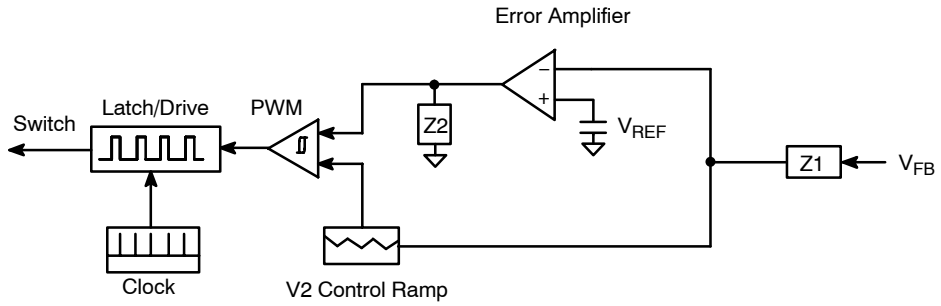

Figure 3. V2 Control

Here too, the feedback signal is compared with a reference voltage to develop an error signal which is fed to one input of the PWM. However in V2, the second input of the PWM is the feedback signal from the output of the converter. This feedback signal provides both dc information as well as ac information (the ramp) for the converter to regulate its set point. The internal clock initiates a drive pulse each switching cycle. When the feedback signal intersects the error signal, the switch cycle is terminated. As both PWM inputs, the error signal and the control ramp, are derived from the converter's output voltage, the control architecture is known as V2. This is a little misleading because the control ramp is typically generated from current information present in the converter. The control architecture can equally support voltage mode control. An application, using voltage feed forward is presented.

Lastly independent of whether a current or voltage mode control technique is employed in V2, there is one important differentiator to note between the arrangement of the control elements discussed in Figures 1, 2 and 3. In V2, high frequency information is processed without an error amplifier. Because the error amplifier is not part of the high frequency path, the converter's closed loop gain and transient performance can be optimized independently of the error amplifier's gain and phase characteristics. This becomes important when point of load converter's have to support 100 A/microsecond transient load requirements for microprocessor based applications.

V2 is deployed in a number of controller's in the ON Semiconductor's IC portfolio, each addressing a particular application. As an illustration of the high level of integration possible with this approach, the following more detailed discussion references the CS5141x buck regulator, shown in Figure 4.

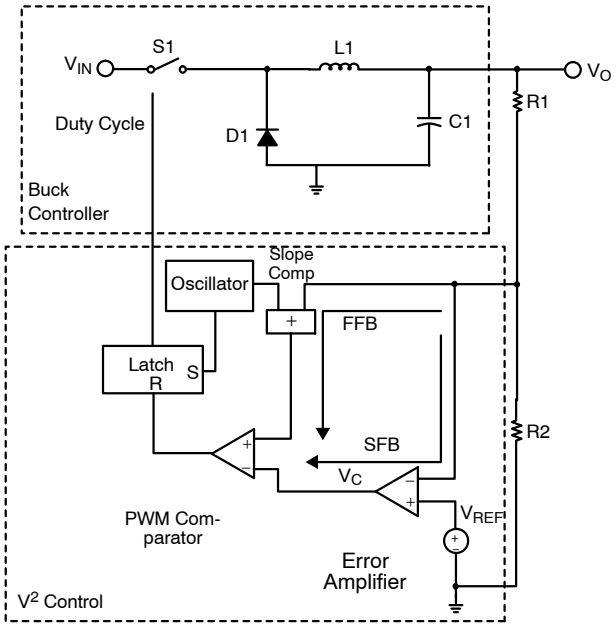

Figure 4. Buck Converter with V2 Control

The feedback signal from the buck converter is processed in one of two ways before being routed to the inputs of the PWM comparator. The Fast Feedback path (FFB) adds slope compensation to the feed back signal before passing it to one input of the PWM. The Slow Feedback path (SFB) compares the original feedback signal against a dc reference. The error signal generated at the output of the error amplifier VC is filtered by a low frequency pole, before being routed to the second input of the PWM.

Each switch cycle is initiated (S1 on), when the output latch is set by the oscillator.

Each switch cycle terminates (S1 off), when the FFB signal (ac plus output dc) exceeds SFB (error dc), and the output latch is reset. In the event of a load transient, the FFB signal changes faster, in relation to the filtered SFB signal, causing duty cycle modulation to occur. Actual oscilloscope waveforms taken from the converter, show the switch node V_{SWITCH}, the error signal V_C and the feedback signal V_{FB} (ac component only) are shown in Figure 5.

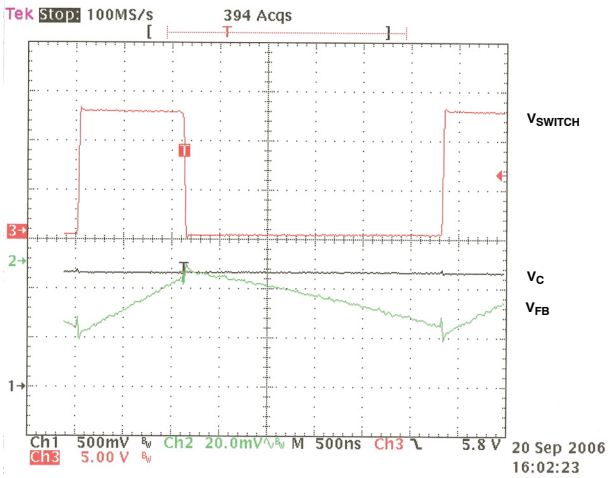

Figure 5.

Loop Gain of Converter

As with any PWM switching controller there are 3 gain blocks present in a V2 controller. (Figure 6) The first block includes the power circuit and PWM modulator, the second the output filter and the third, a gain block providing negative feedback via a compensated error amplifier.

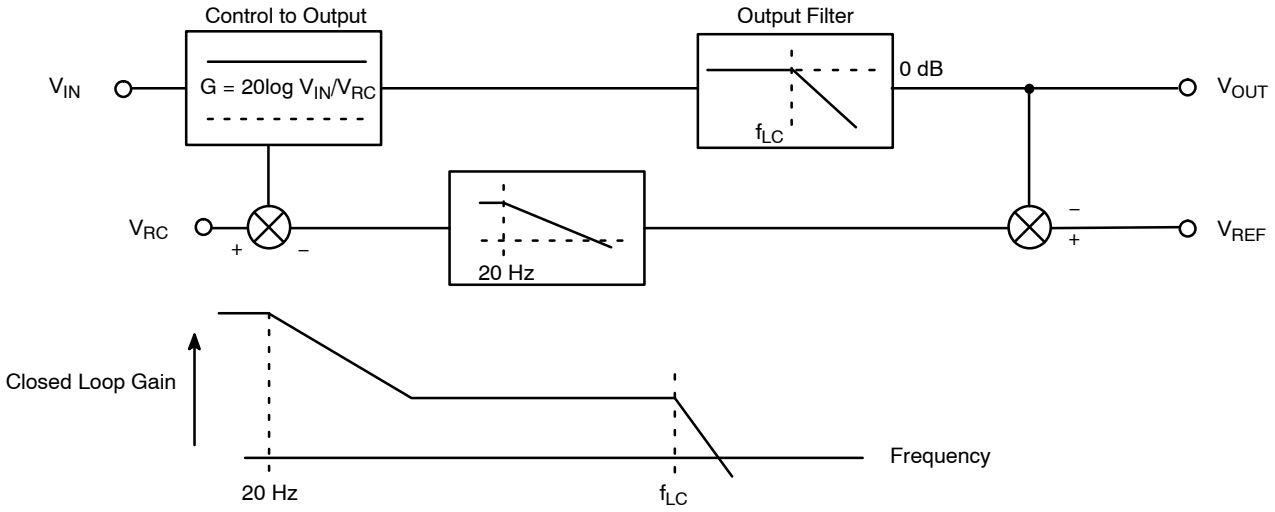

Figure 6. Closed Loop Gain

The gain of the power circuit and modulator, also referred to as control to output, is defined by the ratio of the input voltage V_{IN} to the amplitude of the control ramp V_{RC}.

The next block is the passive output filter stage, which attenuates at slope −2 (40 dB/decade) once the filter's crossover frequency f_{LC} $(1/2\,\pi\,\sqrt{LC})$ is exceeded.

Compensation around the error amplifier feedback block is as follows. The output impedance of the error amplifier is high (7 MΩ). Consequently a small output capacitor of 100 nF for example will create a low frequency pole, in this case at 20 Hz.

The overall closed loop gain can be found by superimposing (summing in dB's) the individual blocks also shown in Figure 6. To provide an unconditionally stable loop and well behaved transient response, phase shift around the loop is required to be in excess of 45 degrees at the loop's unity gain crossover. As the error amplifier has a fixed gain and its compensation set by a single low frequency pole, this is achieved by adjusting the amplitude and phase of the control ramp signal.

Control Ramp Generation

In original V2 designs, the control ramp VCR was generated from the converter's output ripple. Using a current derived ramp provides the same benefits as current mode, namely input feedforward, single pole output filter compensation and fast feedback following output load transients. Typically a tantalum or organic polymer capacitor was selected having a sufficiently large esr component, relative to its capacitive and esl ripple contributions, to ensure the control ramp was sensing inductor current and its amplitude was sufficient to maintain loop stability. This technique is illustrated in Figure 7. This is a very simple technique but contrarian to the basic requirement of a switching regulator to have low output ripple. Component tolerances over time and temperature also have to be considered.

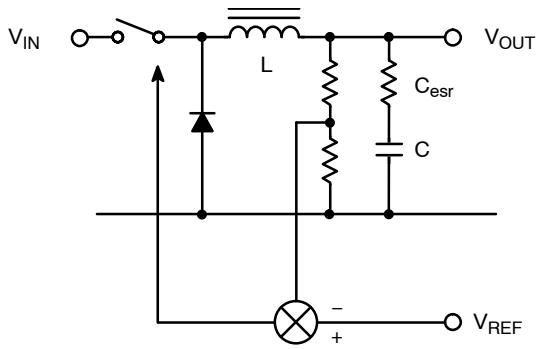

Figure 7. Control Ramp Generated from Output

Advances in multilayer ceramic capacitor technology are such that MLCC's can provide a cost effective filter solution for low voltage (<12 V), high frequency converters (>200 kHz) . For eg., a 10 μF MLCC 16 V in a 805 SMT package has a esr of 2 mΩ and a esl of 100 nH. Using several MLCC's in parallel, connected to power and ground planes on a PCB with multiple vias, can provide a "near perfect" capacitor. Using this technique, output switching ripple below 10 mV, can be readily obtained since parasitic esr and esl ripple contributions are nil. In this case, the control ramp is generated elsewhere in the circuit.

The control ramp used in V2 can be derived in a number ways limited only by the designer's individual creativity.

For example, one approach is to use the technique of inductor DCR sensing to add a RC integrating network across the output inductor and couple the "inductor sensed current" ramp into the feedback path.

Another approach is to generate a voltage ramp from the input switch node to add to the dc feedback signal. In this way a voltage mode controller with inherent feed forward is created.

Ramp Gerneration Using DCR Sensing

The technique is describes as referenced to the design of a 12 V to 3.3 V buck converter running at 1 A load, using MLCC capacitors for the output filter. The circuit of the converter is given in Figure 8. The emphasis here is on the control circuit and not on the loss terms in the power switch, freewheel diode or inductor defining converter efficiency.

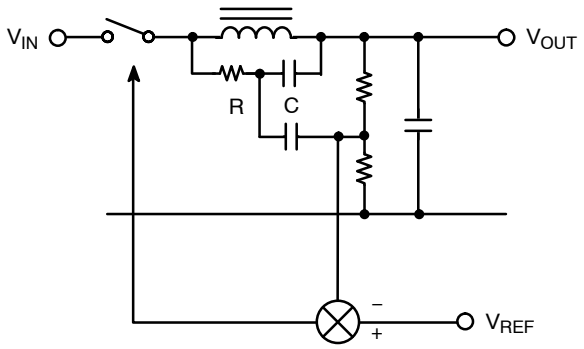

Figure 8. Control Ramp Generated from DCR Inductor Sensing

Design Equations

Nominal Duty cycle D given by Vo/Vin or 0.275

Switching period Ts = 1/260 kHz = 3.85 μS

The ripple current through the output inductor L is given by the equation:

$$\partial Io = Vin\ Ts\ D\ (1-D)\ /\ L$$

If we assume a typical inductor ripple current in the output inductor is 20% of the output current (200 mA), then the value of Lo is calculated from the ac flux equation.

$$\partial Lo = (12 \times 3.85 \times 0.275 \times 0.725)/\ 0.2 = 47\ \mu H$$

At this point in the design, we can go to a magnetic component vendor for a 47 μH inductor with a saturation current equal to 1 A. An example would be TDK SLF10145T−470M1R4 or Coiltronics xyz.

Assuming the inductor resistance is “dcr”, the voltage across this resistance is ∂Vdcr.

$$\partial Vdcr = Vin\ Ts\ D\ (1-D)\ dcr\ /\ L$$

When an integrating network is placed across the output inductor as shown (Figure 9), the voltage developed across the integrating capacitor C, is given by the expression:

$$\partial VCR = Vin\ Ts\ D\ (1-D)\ /\ CR$$

It is apparent that the two expressions are equal if the inductor’s L/r time constant matches the integrator’s CR time constant. In the case of the TDK inductor, Lo = 47 μH and r = 0.1 Ω, so its time constant is 470 μS. Selection of a 10 kΩ resistor and 47 nF integrating capacitor would provide the same 470 μS time constant. The amplitude of the control ramp is ∂Io x r or 0.2 A x 0.1 Ω so our ramp amplitude is 20 mV.

The control ramp is coupled back to the feedback signal using a small coupling capacitor also shown in Figure 8. The actual control ramp is shown in Figure 9 and the converter’s response to a ± 1 A repetetive load step illustrated in Figure 10. The 1 A off load transient is shown in Figure 11 using a reduced time step. Here the converter’s output ripple is observed in addition to the 60 mV load transient. The response illustrates a stable loop, with adequate gain and phase margin.

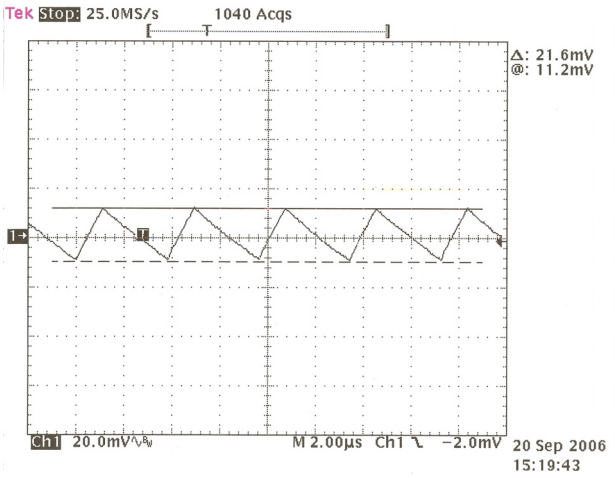

Figure 9.

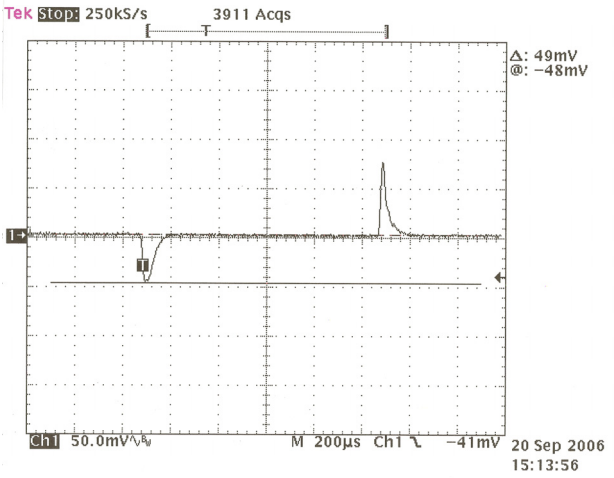

Figure 10.

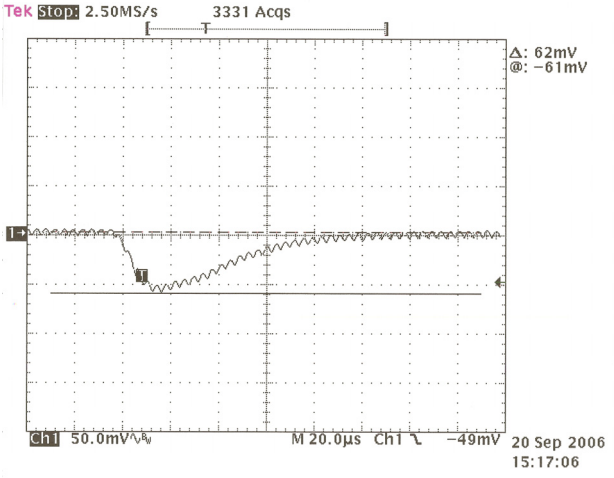

Figure 11.

Ramp Generation Using Voltage Feed Forward

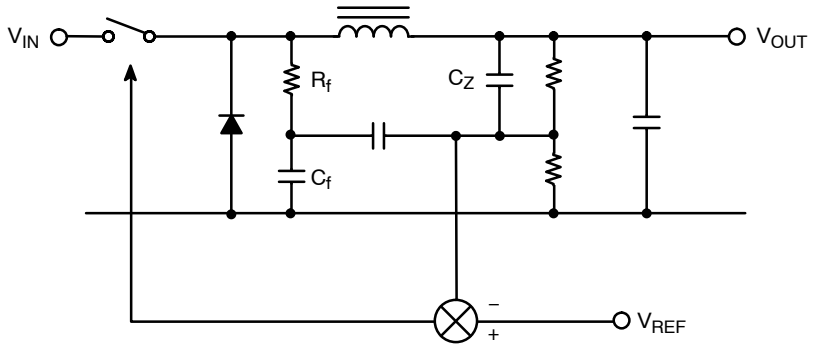

Figure 12. Control Ramp from Voltage Feed Forward

Figure 12 illustrates the technique. Resistor Rf and capacitor Cf form a filter network from the switch node to ground. Assuming this RfCf time constant is large compared to the 3.86 μS switching period, this network integrates the switch node voltage in the same way as does the LC output filter. Consequently the dc voltage appearing across Cf is 3.3 V and the voltage ramp across Cf is given by the following equation.

Vc = {(Vin/Rf) x DTs} / Cf = {DTs/CfRf} x Vin

This voltage ramp is coupled into the converter's feedback signal to provide voltage mode control. It is interesting to note that by itself, his is not sufficient to provide a stable loop. It is necessary to add additional compensation in the form of a zero to compensate for the –2 slope from the LC output stage. This is achieved by the addition of the capacitor Cz, in Figure 12.

The control ramp and 120 mV transient response is illustrated in Figures 13 and 14. Here it is noted that while the loop is stable, the transient waveform marginally overshoots its set point, suggesting the gain and phase margin could be improved.

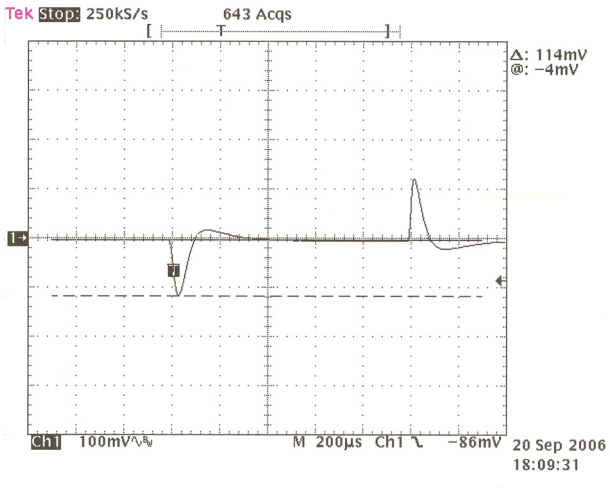

Figure 13.

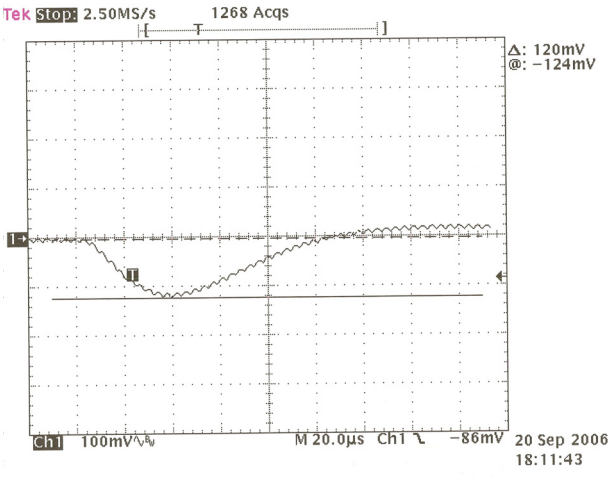

Figure 14.

Conclusion

This note discusses the basic achitecture of voltage mode, current mode and V2, PWM controllers. In V2 the control ramp may be created either from current or voltage information available within the converter. In the case of a buck converter, employing MLCC's at its output, an example of each control technique is presented. Analysis and experimental data are provided. The transient data confirms a loop gain in excess of 10 kHz is readily achievable with the V2 control technique. Additional design information, including Bode plots, is available by referencing the demo board associated with each V2 product.

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