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AND8269/D

Layout Guidelines to Reduce Switch-Node Jitter in the CS51411/NCV51411

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APPLICATION NOTE

Introduction

The CS5141x product family has shown some sensitivity to noise which shows up as jitter on the Switch Node pin (VSW). The CS51411 family uses V^2 control to achieve superior line and load. This control method enhances the load transient response, but under certain conditions can lead to jitter if proper care is not taken. V^2 performs similarly to current mode control, but that the gain is much higher. The gain is set up by the output ripple voltage plus the internal ramp. As you decrease the output voltage, you also decrease ripple voltage which, in turn, increases gain. With a high gain, the PCB layout becomes very critical. This report shows how minor changes in layout can greatly improve VSW jitter on the CS51411 family of buck converters.

Problem

Figures 1 and 2 show examples of this jitter phenomenon. The upper waveform (CH1) is the output voltage and the lower waveform (CH2) is the voltage at VSW.

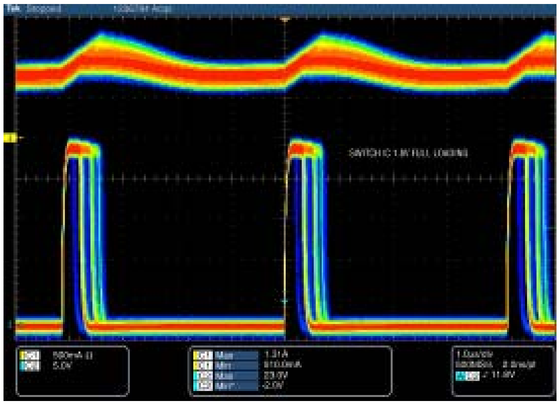


Figure 1. 18 VAC (24 VDC) to 1.8 V/1.4 A

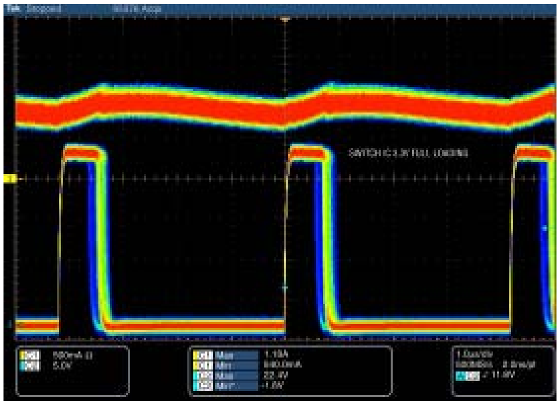


Figure 2. 18 VAC (24 VDC) to 3.3 V/1.3 A

Notice that the jitter at the lower output voltage of 1.8 V is much worse than that at 3.3 V which supports the claim in the introduction. The customer was using the ON Semiconductor evaluation board with their own components when they noted this behavior.

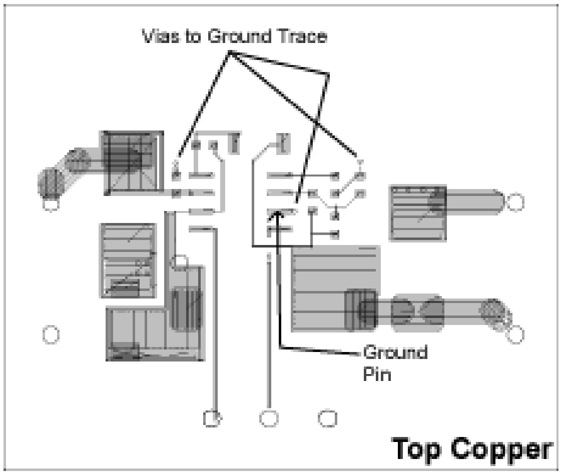


Figure 3. CS51411 Top Metal

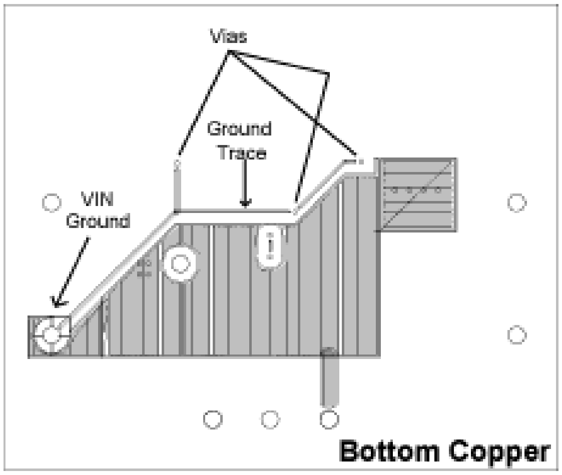


Figure 4. CS51411 Bottom Metal

One can see that the grounding layout is a high impedance connection that could pick up noise. Also one can see that the actual connection of the ground trace to the ground plane is at the V_{IN} ground point. Since the input of the buck converter has discontinuous current, this connection could be injecting unwanted noise. Connecting to the output ground should be a better layout due to the continuous current at the output. Connecting directly to the ground plane could also be a better layout.

SOIC−16W Layout Evaluation

As an experiment in layout optimization the NCV51411 evaluation board was utilized. NCV51411 is the same IC in a different package which uses a layout that connects the ground pin to the output ground and the bottom metal ground plane. Figures 5 and 6 show the layout for this board.

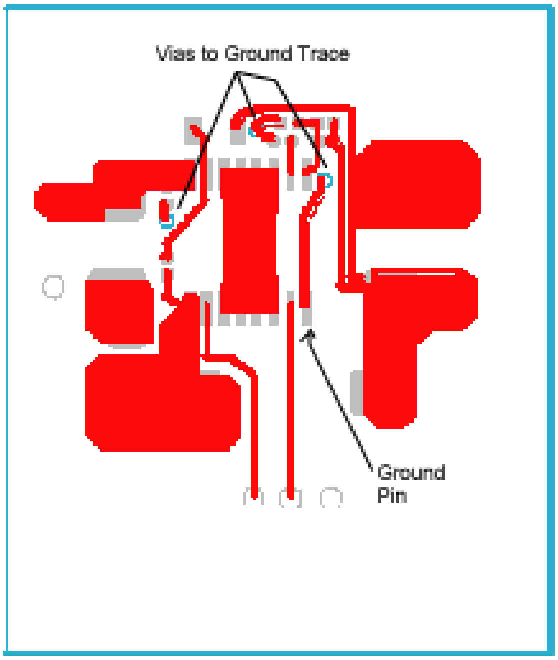


Figure 5. NCV51411 SOIC−16W Top Metal

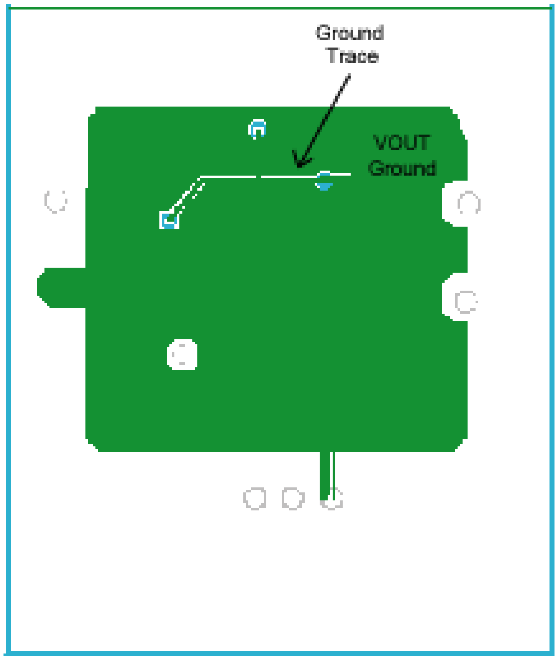


Figure 6. NCV51411 SOIC−16W Bottom Metal

The following waveforms and corresponding schematics show the jitter behavior with this new layout. The input and output capacitor and the inductor are the same as the customer used. The plots are taken with Analog Persistence enabled to plot any changes in the waveform. Figure 7 shows the schematic for the 1.8 V converter which exhibited the worst jitter behavior when using the original layout. Changing the layout and the decoupling capacitor C10 to 3.3 nF eliminated the jitter problem for this converter. The decoupling capacitor was required to provide a low impedance path to ground for unwanted noise. Figures 8 and 9 show the behavior for the 1.8 V converter.

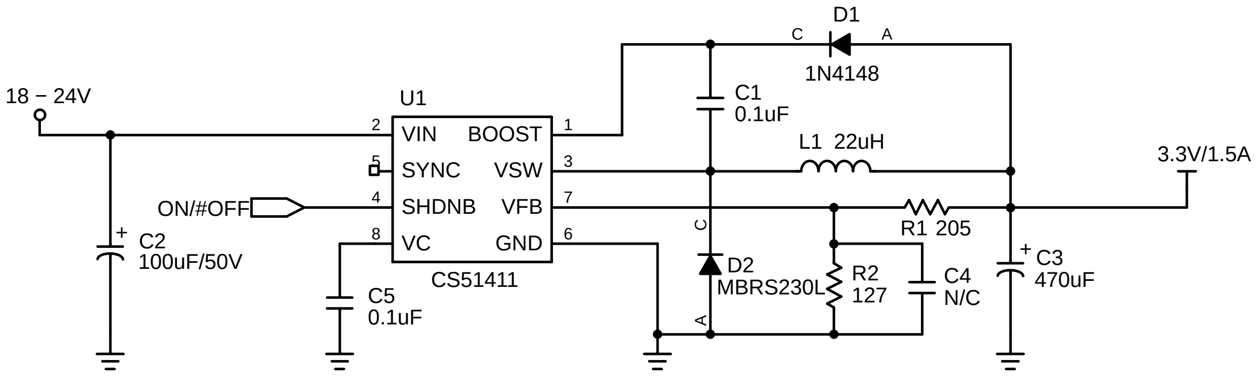
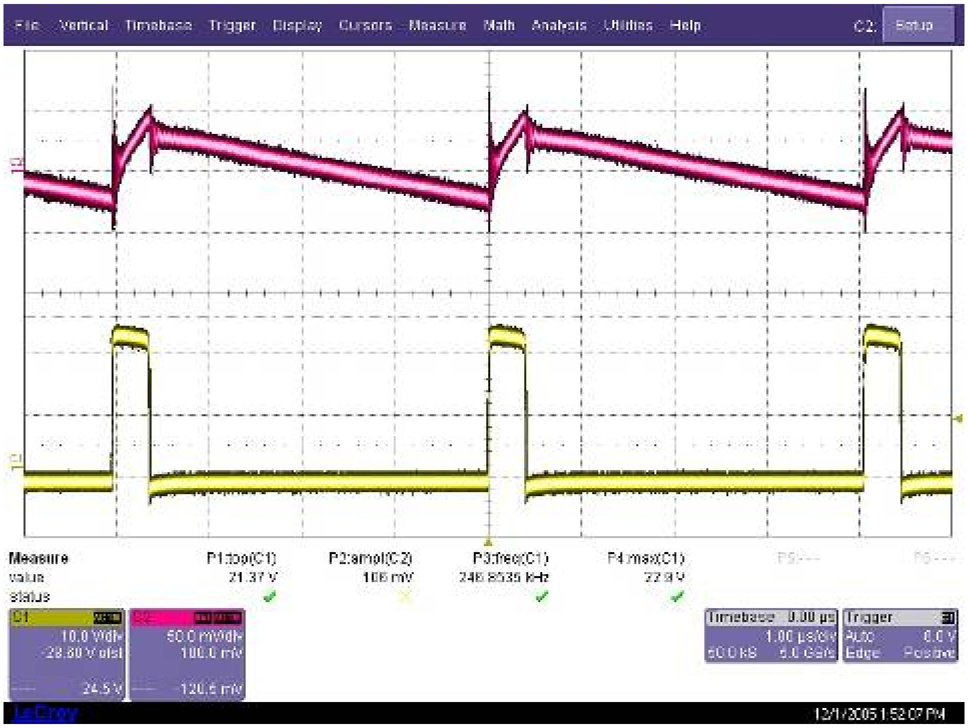


Figure 7. Schematic for a 1.8 V output converter using the NCV51411 SOIC−16W

Figure 8. Vin = 18 V, Vout = 1.8 V, Iout = 1.5 A, C1 = Vout, C2 = VSW



Measure	P1:top(C1)	P2:ampl(C2)	P3:freq(C1)	P4:max(C1)	P5:- - -	P6:- - -
value	21.37 V	106 mV	246.8535 kHz	22.9 V		
status	✓		✓	✓		

C1
10.0 V/div
-28.60 V ofst
24.5 V

C2
50.0 mV/div
100.0 mV
120.5 mV

Timebase 0.00 µs
1.00 µs/div
50.0 kS 5.0 GS/s

Trigger
Auto 0.0 V
Edge Positive

Figure 9. Vin = 24 V, Vout = 1.8 V, Iout = 1.5 A, C1 = Vout, C2 = VSW

Figure 10 shows the schematic for the 3.3 V converter. This converter did not show as much of jitter due to the higher duty cycle/output voltage. Changing the layout was all that was necessary to eliminate the jitter problem for this converter. Figures 11 and 12 show the behavior for the 3.3 V converter.

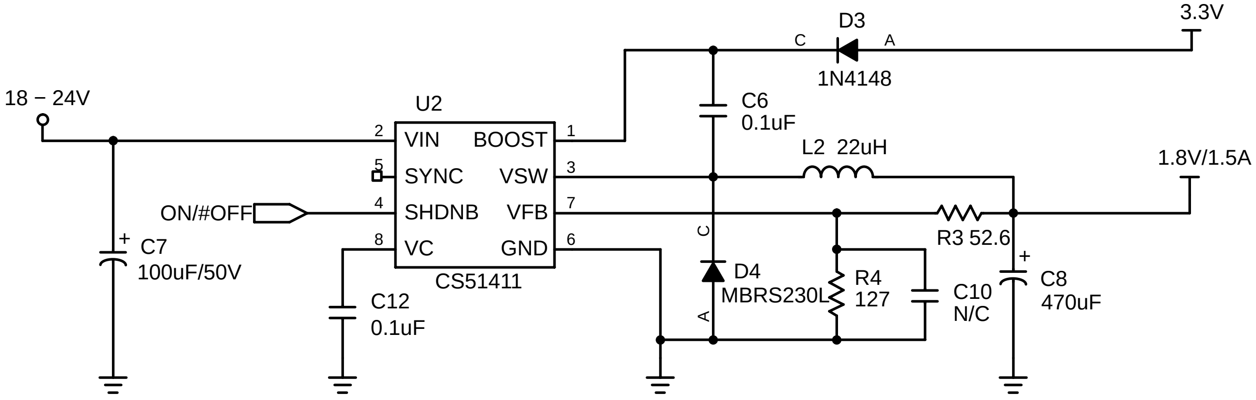
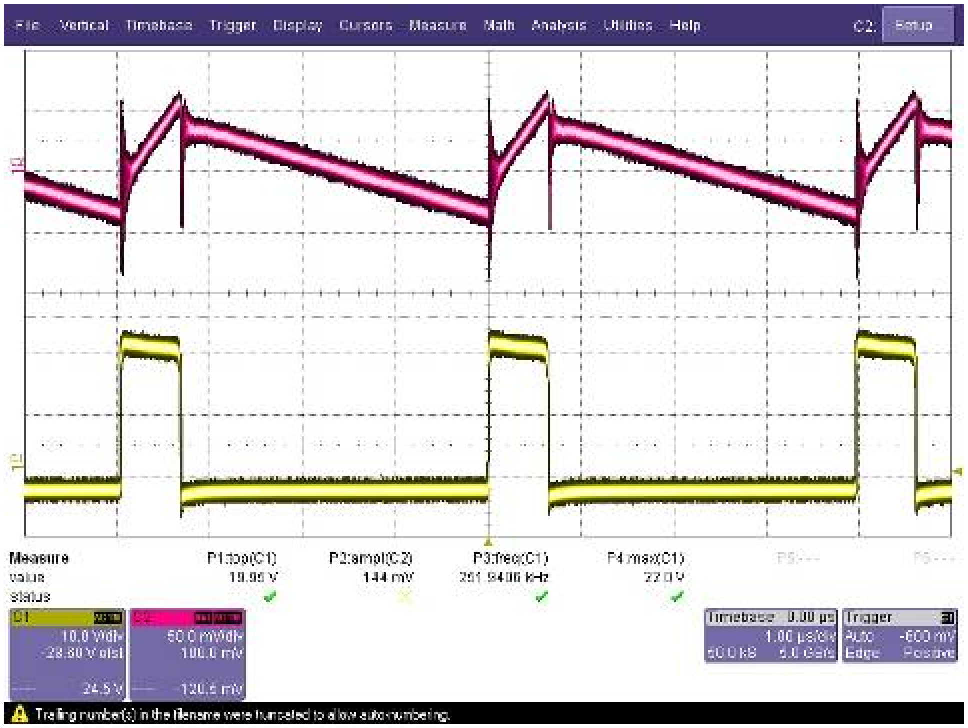


Figure 10. Schematic for a 3.3 V output converter using the NCV51411 SOIC−16W

Measure	P1:top(C1)	P2:ampl(C2)	P3:freq(C1)	P4:max(C1)	P5:---	P6:---
value	13.75 V	144 mV	263.2364 kHz	16.2 V		
status	✓		✓	✓		

Figure 11. Vin = 18 V, Vout = 3.3 V, Iout = 1.5 A, C1 = Vout, C2 = VSW



```
Measure    P1:top(C1)   P2:ampl(C2)   P3:freq(C1)    P4:max(C1)   P5:---   P6:---
value      19.95 V      144 mV        251.9406 kHz   22.0 V
status     ✓            ✗             ✓              ✓
```

```
C1                 C2                                      Timebase   0.00 µs   Trigger
  10.0 V/div         50.0 mV/div                                  1.00 µs/div   Auto    -600 mV
 -28.80 V ofst       100.0 mV                               50.0 kS   5.0 GS/s  Edge    Positive
       24.5 V        120.5 mV
```

Trailing number(s) in the filename were truncated to allow auto-numbering.

Figure 12. Vin = 24 V, Vout = 3.3 V, Iout = 1.5 A, C1 = Vout, C2 = VSW

DFN−18 Layout Evaluation

The same experiment was run on the DFN−18 version of the NCV51411. Figures 13 and 14 show the layout for this package. Again, the ground connection was made as close as possible to the V_{OUT} ground connection and the ground plane to reduce noise pickup.

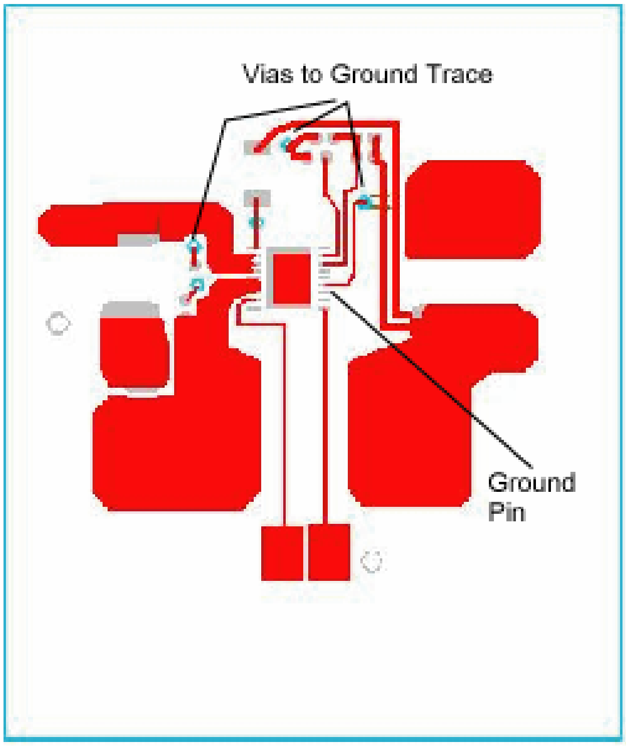


Figure 13. NCV51411 DFN Top Metal

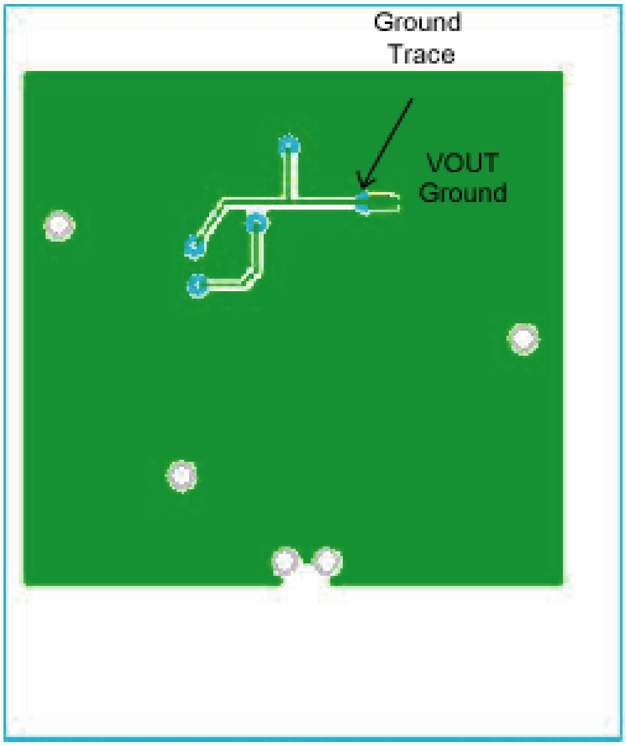


Figure 14. NCV51411 DFN Bottom Metal

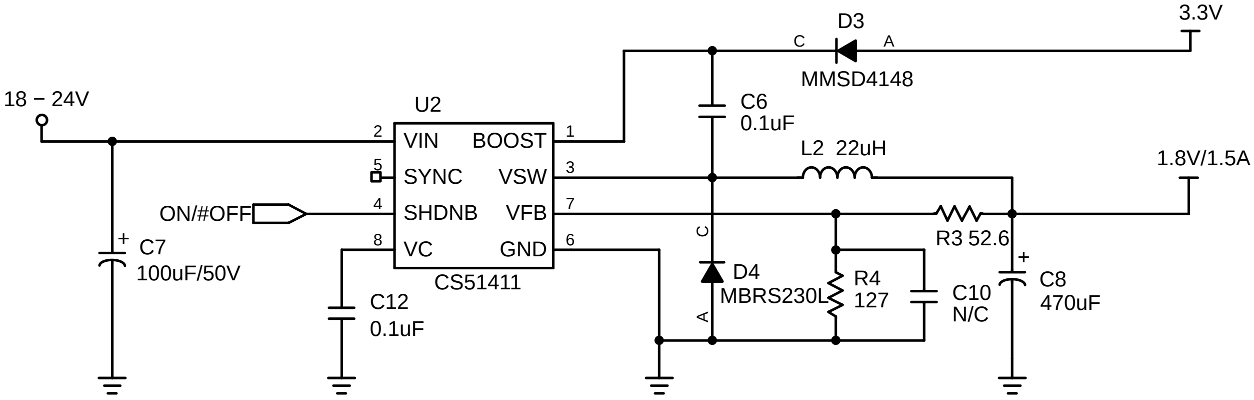


Figure 15. Schematic for a 1.8 V output converter using the NCV51411 DFN−18

Measure	P1:top(C1)	P2:ampl(C2)	P3:freq(C1)	P4:max(C1)	P5:---	P6:---
value	13.79 V	172 mV	251.6610 kHz	18.4 V		
status	✓		✓	✓		

Figure 16. Vin = 18 V, Vout = 1.8 V, Iout = 1.5 A, C1 = Vout, C2 = VSW

Measure	P1:top(C1)	P2:ampl(C2)	P3:freq(C1)	P4:max(C1)	P5:---	P6:---
value	20.01 V	159 mV	250.0786 kHz	22.0 V		
status	✓		✓	✓		

Figure 17. Vin = 24 V, Vout = 1.8 V, Iout = 1.5 A, C1 = Vout, C2 = VSW

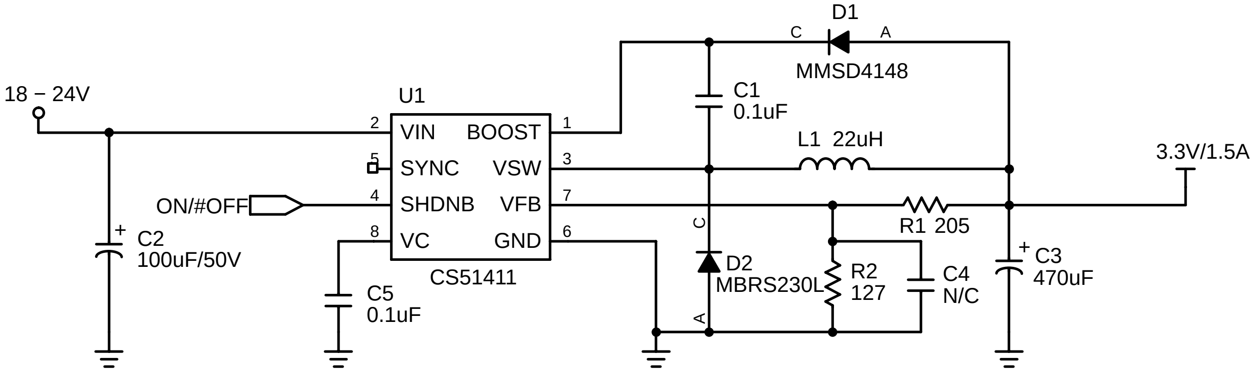
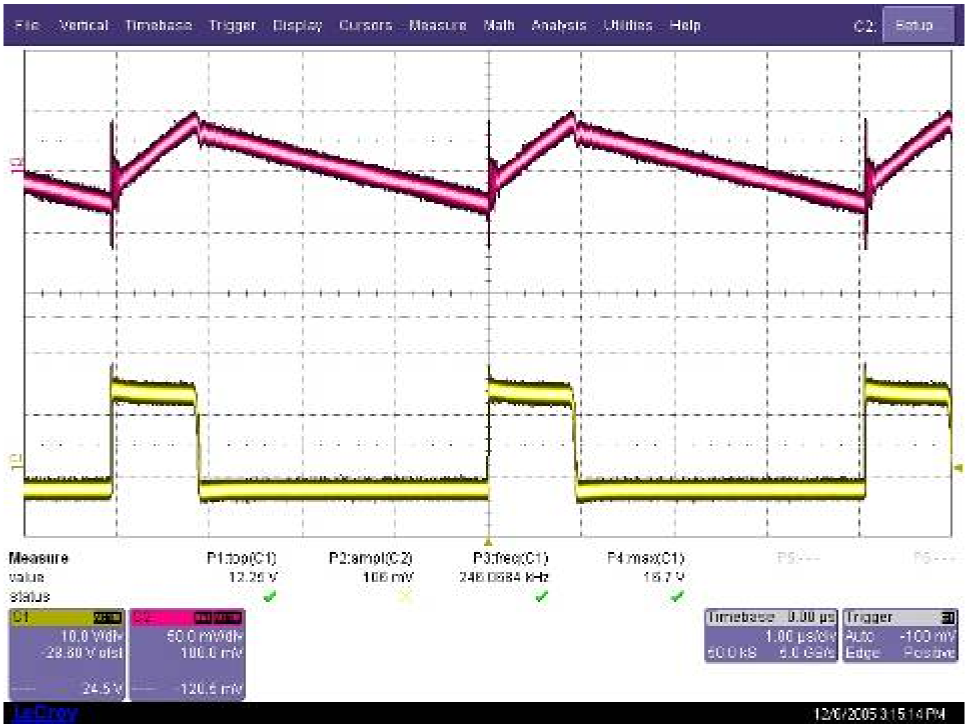
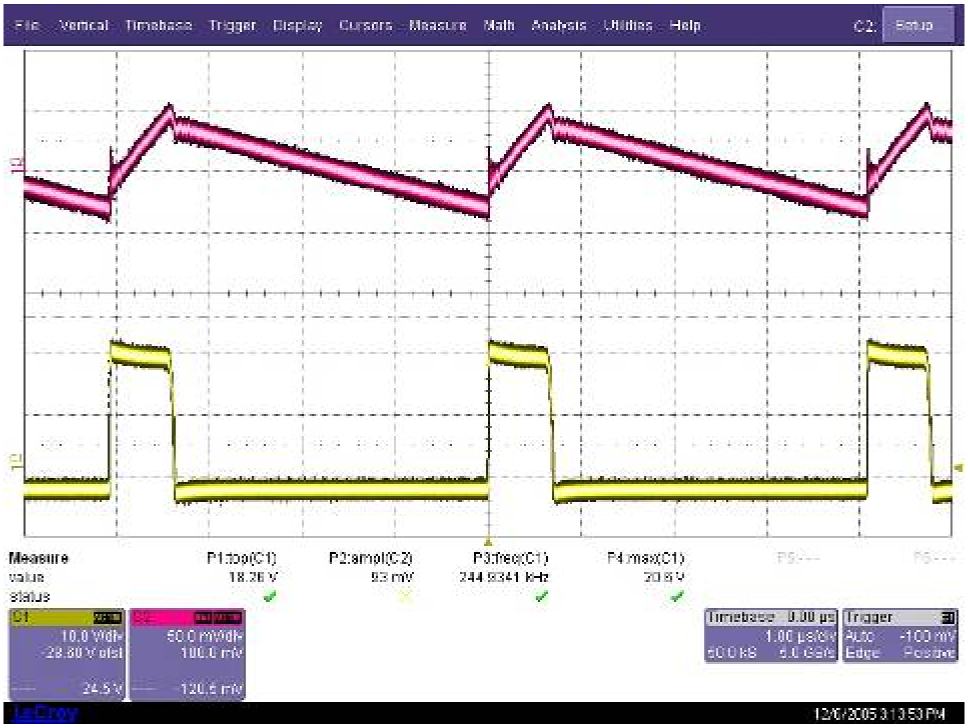


Figure 18. Schematic for a 3.3 V output converter using the NCV51411 DFN−18



Measure	P1:top(C1)	P2:ampl(C2)	P3:freq(C1)	P4:max(C1)	P5:---	P6:---
value	12.25 V	106 mV	246.0684 kHz	16.7 V		
status	✓		✓	✓		

Figure 19. Vin = 18 V, Vout = 3.3 V, Iout = 1.5 A, C1 = Vout, C2 = VSW



Measure	P1:top(C1)	P2:ampl(C2)	P3:freq(C1)	P4:max(C1)	P5:---	P6:---
value	18.26 V	93 mV	244.9341 kHz	20.6 V		
status	✓		✓	✓		

C1 10.0 V/div -28.80 V ofst 24.5 V

C2 50.0 mV/div 100.0 mV 120.5 mV

Timebase 0.00 µs 1.00 µs/div 50.0 kS 5.0 GS/s

Trigger Auto -100 mV Edge Positive

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Figure 20. Vin = 24 V, Vout = 3.3 V, Iout = 1.5 A, C1 = Vout, C2 = VSW

Summary

The above data shows that with proper layout and decoupling, the jitter in the CS51411 family can be eliminated. Proper layout involves connecting the IC ground close the V_{out} ground point, rather than V_{in}, and providing a via to a low impedance ground plane to prevent noise pickup. Also, as pointed out earlier, when you decrease the output voltage, you also decrease ripple voltage which, in turn, increases gain. For lower output voltages noise immunity improves even further by decoupling the feedback pin (V_{FB}), but the key to eliminating jitter is the layout.

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