# AND8202/D

# Low-Side Self-Protected MOSFET

ON Semiconductor®

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APPLICATION NOTE

### Introduction

The ever increasing density and complexity of automotive and industrial control electronics requires integration of components, wherever possible, so as to conserve space, reduce cost, and improve reliability. Integration of protection features with power switches continues to drive new product development. The often open environments of automotive and industrial electronics, subject to severe voltage transients, high power and high inductance loads, numerous external connections, and human intervention force the requirement of fault protection circuitry. Advancements in power MOSFET processing technology afford an economical marriage of protection features, such as current limitation, and standard MOSFET power transistor switches. This paper describes the technology and operation of ON Semiconductor's HDPlus monolithic low-side smart MOSFET family.

### Process Technology

Key to an economical monolithic process is to avoid high layer count bi-CMOS process flows. These flows allow for more complex and accurate control circuitry, but are very costly. Moreover, these flows typically utilize lateral power MOSFETs for the output drive stage, which significantly limits load capability due to the large size of the output transistor. Efficient vertical DMOS output transistors are possible, but require an even more complicated and expensive process flow, potentially up to three times the cost of a standard MOSFET flow.

ON Semiconductor's HDPlus low-side products utilize a standard vertical DMOS transistor process flow, integrating most protection elements without additional process steps. One additional process step allows for more complex protection circuitry. This process structure features control elements referenced to source ground and which can be isolated from the load supply voltage, since the control signal (gate) voltage supply often derives from a filtered and regulated source.

### General Topology

Figure 1 shows three general circuit topologies for low-side HDPlus products.

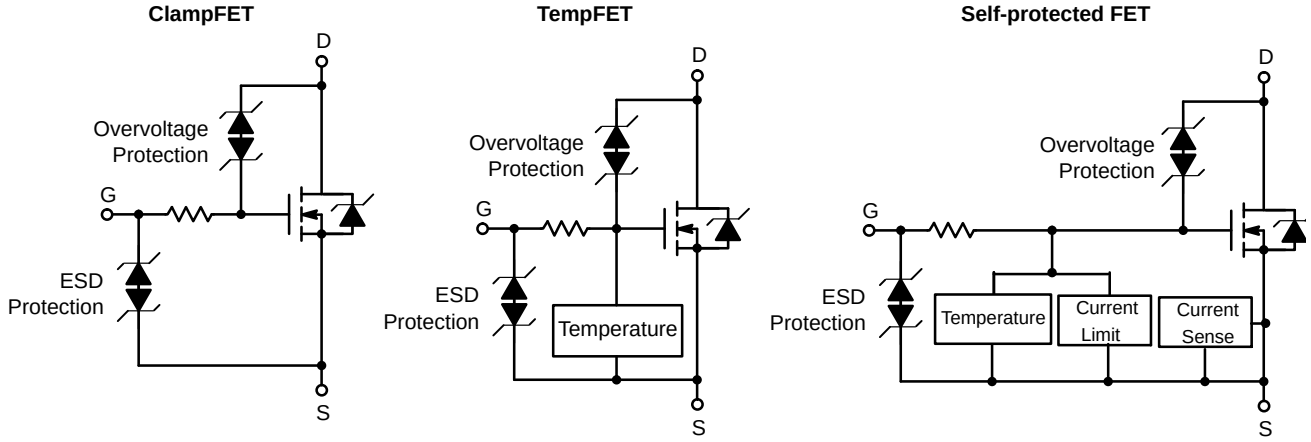


**Figure 1. Block Diagrams of ClampFET, TempFET, and Self-Protected Topologies**

ClampFET topologies utilize ESD protection at the gate input and active gate to drain clamping (described later), useful when switching inductive loads. Thermally protected ClampFET topologies add overtemperature shutdown protection and are specially designed to work with the ON Semiconductor NCV7513 low-side MOSFET pre-driver device. Fully protected low-side topologies incorporate all ClampFET features and add current limitation and overtemperature shutdown circuits. All topologies drive any type of resistive or inductive load such as solenoids, heater coils, and filament bulbs limited only by the current and thermal capability of the device. Table 1 lists the HDPlus low-side family of devices and associated circuit topology.

**Table 1. HDPLUS LOW-SIDE PRODUCT FAMILY AND FEATURES**

| Device | Package | Topology | $T_{lim}$ | $I_{lim}$ | Clamp Voltage (V) Typ. |
|---|---|---|---|---|---|
| NCV8401 | DPAK | Self-protected | X | X | 46 |
| NCV8402 | SOT−223 | Self-protected | X | X | 46 |
| NCV8403 | DPAK/SOT−223 | Self-protected | X | X | 46 |
| NCV8405 | SOT−223 | Self-protected | X | X | 46 |
| NCV8406 | SOT−223 | Self-protected | X | X | 65 |
| NCV8440 | SOT−223 | ClampFET | | | 55 |
| NIMD6001 | SO−8 | DiagnosticFET | | | |
| NID9N05CL | DPAK | ClampFET | | | 55 |
| NIF9N05CL | SOT−223 | ClampFET | | | 55 |
| NID5001N | DPAK | Self-protected | X | X | 46 |
| NIF5002N | SOT−223 | Self-protected | X | X | 46 |
| NID5003N | DPAK | Self-protected | X | X | 46 |
| NIF5003N | SOT−223 | Self-protected | X | X | 46 |
| NIF62514 | SOT−223 | Self-protected | X | X | 46 |
| NID6002N | DPAK | Self-protected | X | X | 67 |

### Normal Operation

Under normal operation, the HDPlus low-side product family operates the same as any standard power MOSFET device. Many of the HDPlus low-side data sheet parameters and data sheet curves are identical to those found on standard MOSFET data sheets. Since numerous application notes cover standard power MOSFET operations topics including gate drive control, gate charge, switching characteristics, thermal management, etc., this paper focuses only on fault condition operation and modes of normal operation affected by fault protection circuitry.

### Fault Types

Perhaps the most common and worrisome fault is a short circuit. This type of fault can take several forms, as detailed below:

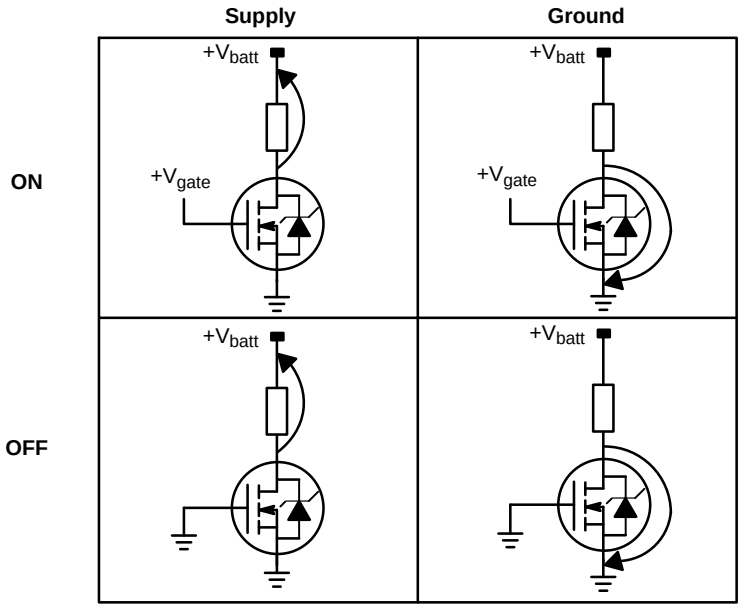


**Figure 2. Short Circuit Modes**

Such short conditions are further exacerbated since often the short circuits are intermittent and thus can take many forms during even very brief periods. For example, in the case of a short to ground with the MOSFET off, one normally would not worry about the FET since current is diverted thru the short. However, if the short is intermittent and the load is inductive, the interruption of the current flow results in a fly-back voltage appearing at the drain node of the FET. The peak current in the load inductance could be higher than normal operation due to the duration of the short and when the resistance of the short is less than the operating resistance of the MOSFET. Thus the device may absorb more energy than expected, and numerous intermittent short events occurring in quick succession could result in elevated peak junction temperature, leading to potential device destruction.

Other faults include electro static discharge (ESD) at the device pins, overvoltage due to line transients or inductive load switching, and overheating. Overtemperature failure typically results from another failure such as short circuit which vastly increases device power dissipation, but can also result from extreme ambient conditions or a thermal path anomaly such as a solder void between the device heatsink and circuit board. The control circuitry of the low-side HDPlus products can detect and control device operation during many of these failure modes by operating in a safe mode so the device can return to normal function once the fault is remedied.

### Gate Input Operation

The gate input pin on the HDPlus low-side family of product behaves very much like the gate pin of a standard MOSFET. So much so, in fact, that data sheets for this family of products list the input pin as the gate input pin. The voltage at the gate input pin has a direct path to the gate of the power MOSFET output transistor and as such, the magnitude of this voltage determines the operation mode of the MOSFET switch. At voltages below the device threshold, the device remains off and blocks the load supply voltage. As the gate voltage increases above threshold, the device channel becomes progressively enhanced, putting the MOSFET into the on state. Exceeding the rated voltage on the gate input pin can result in rupture of the device gate oxide, rendering the device useless. This behavior is the same as for standard MOSFET devices. Thus, any drive circuit used to drive standard MOSFETs can be used to drive HDPlus low-side MOSFET devices. However, given that the gate input pin also drives the control circuitry and series gate resistance for HDPlus low-side devices, special consideration must be made for the source and sink current capability of the input drive circuit.

A simplified input circuit is shown in Figure 3. Since active components other than the MOSFET gate oxide interface are connected to the gate input pin, the current leakage at this pin with the drain shorted to the source ($I_{gssf}$) is typically three orders of magnitude greater than the same leakage measurement on standard MOSFET (50−100 μA versus < 50 nA). Under normal operation, the voltage supply at the gate input must be capable of driving the $T_{lim}$ reference voltage and control circuitry on devices with overtemperature protection or both current limit and overtemperature protection. More importantly, the gate voltage supply must be capable of driving enough current during a current limit or thermal shutdown fault condition.

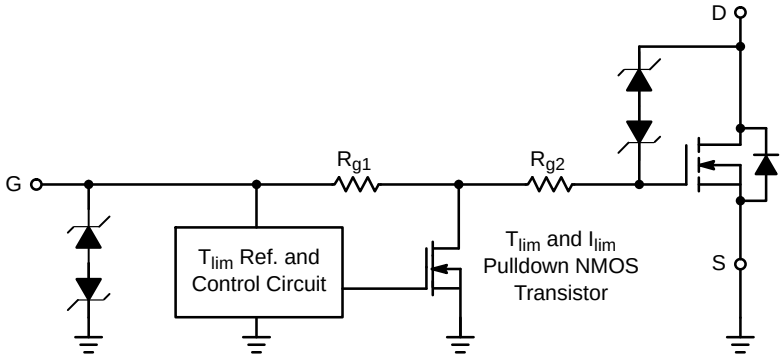


**Figure 3. Simplified Input Circuit**

When the device is in a current limit operation mode, a feedback loop to the gate of the current limit pulldown transistor will drive the gate of the main power MOSFET to near threshold voltage, approximately 2−3 volts above ground. Thus in this mode, the gate input supply must be able to source a current equal to $(V_{in} - V_{gate}) / R_{g1}$ plus additional bias current, where $V_{gate}$ is near threshold voltage. During thermal shutdown, the $T_{lim}$ pulldown transistor pulls the gate voltage down to ground potential. Thus, the gate input supply must source current equal to approximately $V_{in}/R_{g1}$ plus some additional bias current. In addition, $R_{g1}$ (and $R_{g2}$) are negative temperature coefficient devices, thus temperature shutdown operation mode is the worst case condition for determining minimum gate drive current source and sink requirements. This minimum source current must be available during an overtemperature fault. If not, the pulldown transistor may not keep the power FET off, possibly allowing the junction temperature of the power FET to reach the destructive level. The following table lists nominal room temperature values of $R_{g1}$, $R_{g2}$, and typical gate input current for normal and $T_{lim}$ fault conditions at elevated temperature by device. Figure 4 shows how gate

input current during $T_{lim}$ fault varies with gate voltage for the NIF62514 device. The non-linearity of the curve in Figure 4 indicates the non-linear behavior of the additional bias current required for the control circuitry as a function of gate voltage.

**Table 2. TYPICAL GATE INPUT PARAMETERS**

| Device | $R_{g1}$ (kΩ) | $R_{g2}$ (kΩ) | $I_g$ @ 5.0 V (μA), $T_j$ = 125°C | $I_g$ @ 5.0 V (μA), $T_j > T_{lim}$ |
|---|---|---|---|---|
| NCV8401 | 9.9 | 5.0 | 38 | 600 |
| NCV8402 | 60 | 40 | 37 | 150 |
| NCV8403 | 13.5 | 9.0 | 43 | 450 |
| NCV8405 | 30 | 20 | 38 | 220 |
| NCV8406 | 1.0 | 0.5 | 41 | 5900 |
| NIF62514 | 30 | 20 | 59 | 242 |
| NIF5002N | 60 | 40 | 53 | 146 |
| NID5001N | 10 | 5.0 | 58 | 634 |
| NIF5003N | 14 | 5.0 | 66 | 507 |
| NID5003N | 14 | 5.0 | 66 | 507 |
| NID6002N | 1.0 | 0.5 | 70 | 5170 |

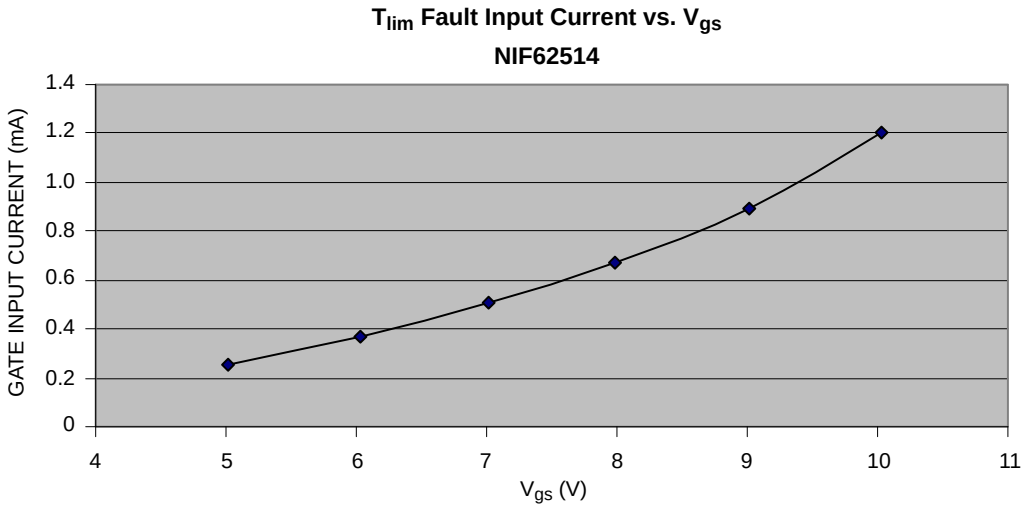


**Figure 4. Gate Input Current as a Function of $V_{in}$ During $T_{lim}$ Fault for the NIF62514 Device**

The resistances, $R_{g1}$ and $R_{g2}$, in series from the gate input to the power MOSFET gate, in addition to affecting minimum input source current requirements, also affect switching speed and EMI/RFI requirements for the gate drive design. The gate of the power MOSFET essentially is a capacitive load to the gate drive output, so any resistance in series with the gate input will slow down the rising and falling switching transitions of load current and voltage. Many MOSFET circuit designs add 1.0 kΩ or more of external series gate resistance in order to slow the normally nanosecond rise and fall times, especially in applications with strict EMI/RFI limitations. Since all HDPlus low-side MOSFET devices have integrated series gate resistance, addition of external series gate resistance may not be necessary.

Lastly, the gate input pin of a MOSFET device may be subjected to ESD during the assembly, test, installation, and service of the circuit board. All HDPlus low-side design incorporate back to back ESD diodes (Figure 3) at the gate input pin. These diodes, typically set to an approximate 13 V Zener voltage, coupled with the internal series gate resistance, allow a minimum of 4,000 V Human Body Model ESD capability and at least 400 V Machine Model ESD capability.

### Current Limit Operation

Figure 5 shows a simplified current limit circuit topology used in HDPlus low-side devices. The current limit function is based on a load current sensing technique that utilizes SENSEFET® technology. Vertical DMOS power MOSFET

technology, whether trench or planar gate structure based and whether striped or cell active area based, the total active area of the device can be modeled as a number of smaller transistors connected in parallel. SENSEFET technology takes advantage of this principle by isolating a portion of the source metallization and making a separate connection to this isolated area. This essentially creates two power transistors connected in parallel that share current in proportion to their respective active areas. The source connection of the smaller transistor is known as the mirror connection and the ratio of current thru the larger device to the current thru the smaller device is known as the current mirror ratio and is symbolized by the letter n. The current mirror ratio usually ranges between n = 200 and n = 1000, but can be higher. This means a sense current equal to only 1/200 to 1/1000 of the load current flows thru the current mirror MOSFET. This affords integration of a sense resistor in the control circuit because the sense resistor will dissipate power on the order of milliwatts or less with amperes of current flowing thru the load. More detailed information regarding SENSEFET technology is found in ON Semiconductor application note AND8093/D.

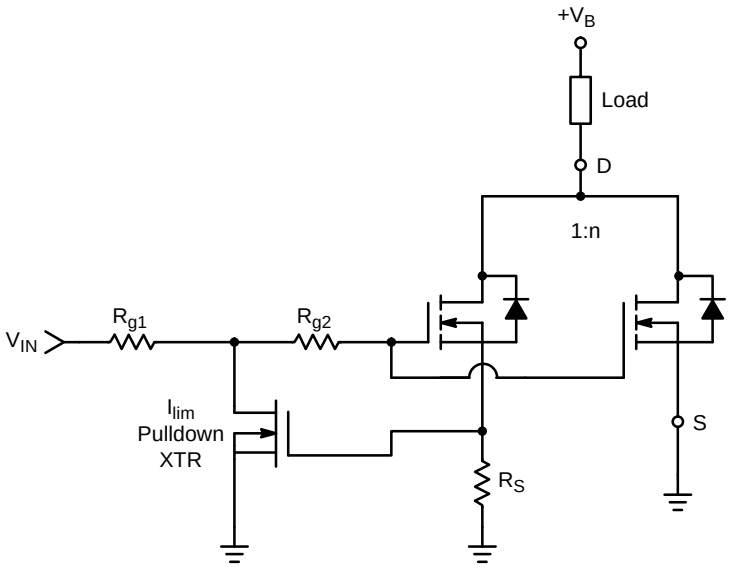


**Figure 5. Simplified Current Limit Circuit**

The voltage developed across $R_{sense}$ is fed to the gate of a NMOS pull down transistor. The drain of the NMOS transistor is connected to the gate of the output power MOSFET thru the series resistance $R_{g2}$. As the load current increases, the voltage at the gate of the pulldown transistor increases until the pulldown transistor threshold is reached; this is the point of the load current limit setpoint. The pulldown transistor begins to reduce the voltage at the power MOSFET gate and a feedback loop is established where the pulldown transistor maintains enough gate voltage to maintain the load current at the setpoint value.

In this mode of operation, the power MOSFET is operating in a saturation region, meaning the device is biased near threshold voltage so the channel of the device is not fully enhanced to the on-state. Not only is the device conducting high current, but it is conducting this current at high drain to source voltage. In the case of a near perfect short across the load, nearly all of the load supply voltage is across the drain to source of the power MOSFET. Thus in the current limit operation mode the power MOSFET dissipates significant power. Such high power dissipation could quickly lead to device destruction if not for the overtemperature shutdown feature. This will be discussed in the next section.

However, as the output power MOSFET heats up during current limit operation, the control section of the die containing the pulldown NMOS transistor also heats up. The NMOS transistor threshold varies negatively with increasing temperature, so less sense voltage is required to activate the pulldown transistor. Thus as the power MOSFET continues to heat up, the current limit setpoint decreases.

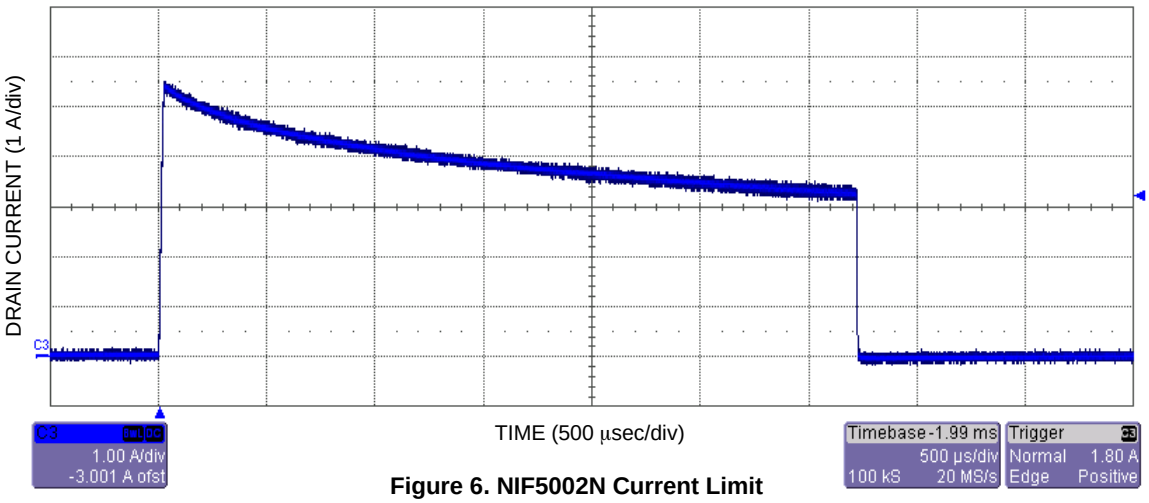


**Figure 6. NIF5002N Current Limit**

In the scope capture above, the NIF5002N device under test was turned on into a direct short and the current is limited initially to approximately 5.5 A. As the device heats the current limit value progressively decreases to approximately 3.3 A until it reaches the overtemperature setpoint and shuts off.

The current limit value not only varies with temperature, as discussed above, but also with applied gate voltage. Figure 7 plots the current limit value versus gate voltage at two different junction temperatures (below the $T_{lim}$ threshold) for the NIF62514 device. As more gate voltage is applied to the device, effectively more voltage is applied to the drain of the gate pull down transistor. More drain current is thus required in the pulldown transistor to limit the current which requires more gate drive to the pulldown transistor. This means more sense current is required through the sense resistor, which requires more drain current through the main power MOSFET.

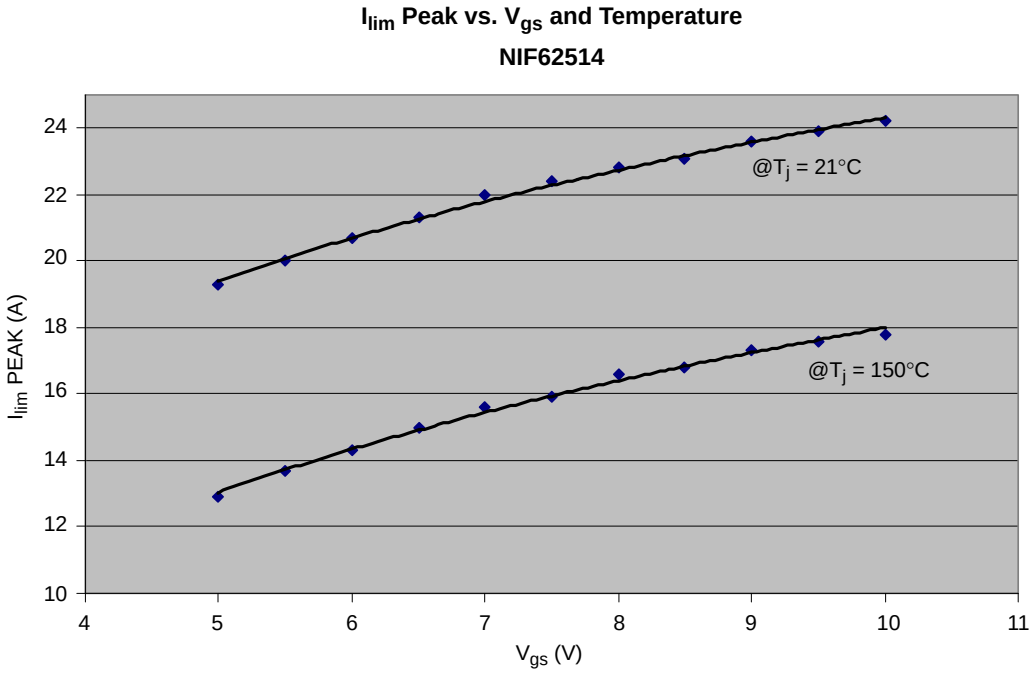


**Figure 7. Peak Current Limit as a Function of Temperature and Gate Voltage**

The series resistance $R_{g2}$ limits how fast the current limit circuit reacts to load current exceeding the current limit setpoint. Discharging the main power MOSFET capacitance thru $R_{g2}$ limits the current in the pulldown transistor. This results in limiting the dv/dt seen at the power MOSFET drain as the drain voltage transitions from low on-state magnitude to a higher magnitude in linear operation. This is important because a high magnitude dv/dt, especially coupled with higher supply voltages, may result in latchup of one or more NMOS control transistors. Latchup can occur when enough current is injected into the NMOS structure so that a normally shunted parasitic P−N junction is forward biased. The injected current comes from the capacitance formed by the depletion region between the drain and P-tub source region, from the relation i = CdV/dt. In the HDPlus process, each NMOS transistor layout is optimized to reduce susceptibility to injected currents and $R_{g2}$ is added as an additional structure to eliminate device latchup.

### Overtemperature Shutdown Operation

Figure 8 diagrams a simplified overtemperature detection and shutdown circuit.

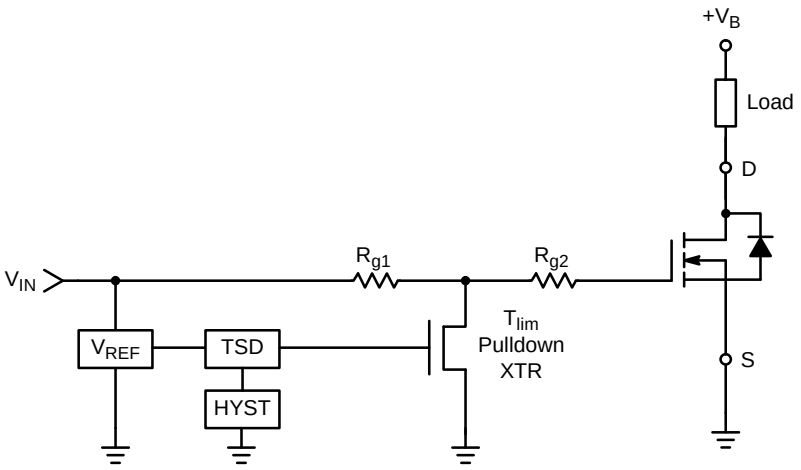


**Figure 8. Simplified Temperature Limit Shutdown Circuit**

A reference voltage biased by the gate input supply voltage, provides a reference for the temperature sensitive device (TSD) elements. These elements (diode structures) are located near the center of the active area of the main power MOSFET, which is the area on the die most likely to heat the quickest during a thermal transient event. If the TSD elements indicate a die junction temperature greater than the overtemperature setpoint, the $T_{lim}$ pulldown NMOS transistor pulls the main power MOSFET gate to ground, turning off the device. A hysteresis circuit allows the device to turn back on after the die junction temperature cools by approximately 15°C. As seen in the scope trace below (a time extension of Figure 6), the device will oscillate on and off at frequency determined by the thermal management of the application.

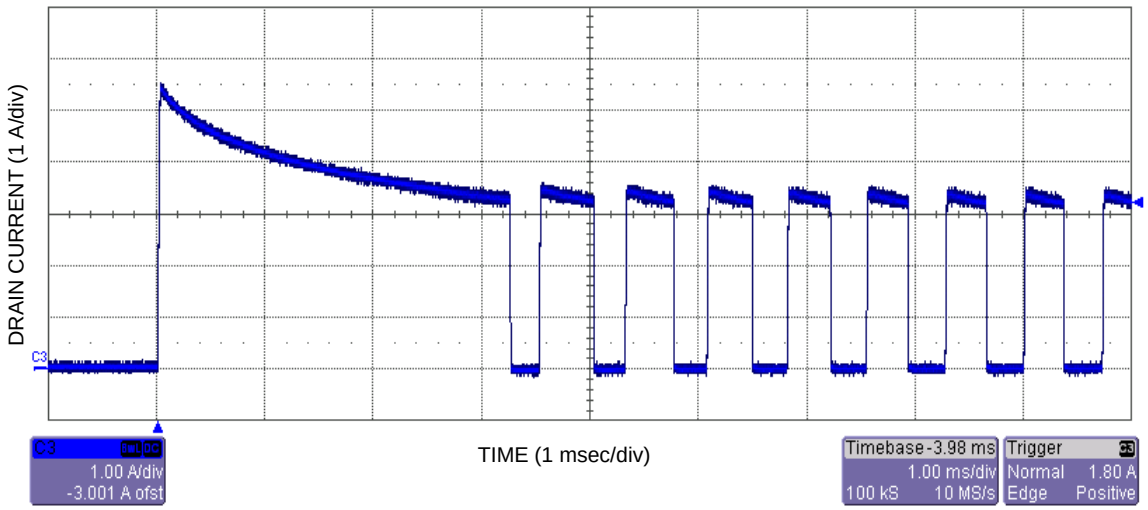


**Figure 9. NIF5002N Current Limit Expanded, Showing Thermal Cycling**

Although current HDPlus TempFET and self-protected MOSFET products are designed with hysteretic auto restart capability during $T_{lim}$ fault conditions, proven HDPlus test circuits are designed that latch-off the power MOSFET during a $T_{lim}$ fault and allow restart only when the gate input pin is toggled.

Since the reference voltage for the TSD elements is affected slightly by the magnitude of the gate input supply voltage, especially at lower gate voltages, the overtemperature setpoint decreases as the gate input voltage increases up to approximately 5.0 V. As the applied gate voltage increases above 5.0 V, the temperature shutdown limit increases slightly with increasing gate voltage. This is illustrated in Figure 10. The slight increase in the temperature shutdown limit for gate voltage above 5.0 V is due to the increased gate drive required by the NMOS pulldown transistor as the NMOS drain voltage increases.

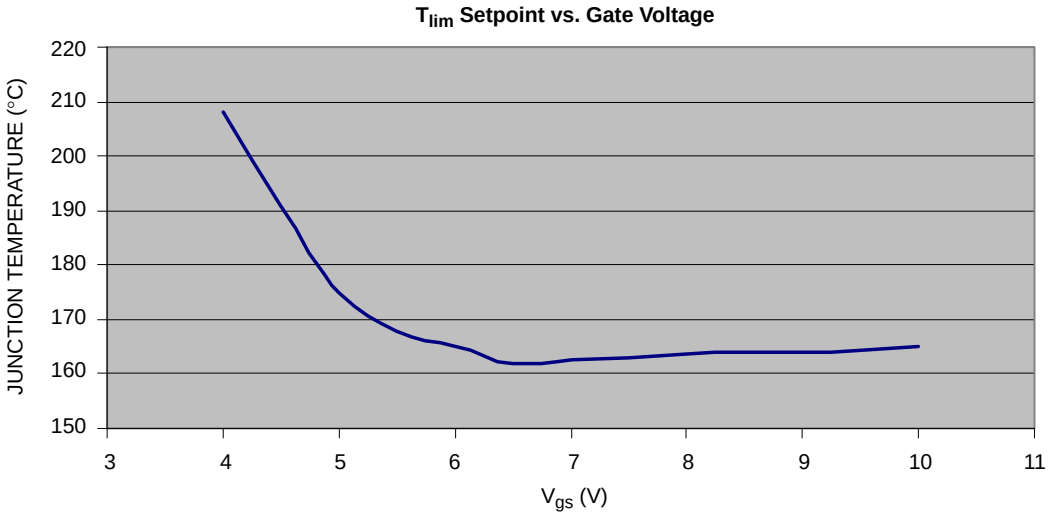


**Figure 10. Typical Temperature Limit Shutdown as a Function of Gate Voltage**

The HDPlus overtemperature protection circuitry allows the device to survive fault conditions, such as a short circuit. As part of the HDPlus family reliability study, devices were subjected to 1,000 hours of continuous operation with a shorted load. This resulted in excess of 36 million thermal on-off cycles, without device failure or degradation of electrical parameters. In this case, the range of junction temperature was approximately the 15°C thermal hysteresis, from 160°C, to 175°C. Further tests were performed to increase the delta junction temperature to 100°C, by turning off the part long enough after each thermal cycle to allow the junction temperature to cool by 100°C before turning the part back on into a shorted load. In this case the test was terminated after 360,000 thermal cycles, without any device failure or degradation of electrical parameters. However, device lifetime is a function of the delta junction temperature and applied power and thus protected devices can not survive indefinitely. In cases with high applied voltage, high current limit magnitude, and operation conditions that allow for large delta junction temperature, device lifetime can be limited to a few thousand short circuit cycles. It is recommended that system designs minimize the delta junction temperature during fault conditions or limit the number of fault cycles or both to ensure expected device lifetime.

There is a non fault operation mode where the overtemperature protection is not active and device failure is possible. When switching off an inductive load, the device must absorb the energy stored in the load inductor, equal to 1/2 ($Li^2$). For standard MOSFETs, this operation mode is known as Unclamped Inductive Switching (UIS). During a UIS event, the device drain to source silicon junction is in avalanche and significant power must be dissipated by the device, dependent on the avalanche voltage and peak current value. The normal failure mode for an UIS event is when the energy absorbed by the MOSFET raises the junction temperature above the intrinsic temperature of the silicon structure, typically greater than 300°C. When the junction temperature exceeds the intrinsic temperature, the device stops behaving like a semiconductor, gate control is lost, and device destruction quickly occurs unless drain supply power is immediately removed.

This failure mode is the same for the HDPlus low-side family of products, except these products use an active self-clamping technique from gate to drain to clamp the drain voltage below the avalanche breakdown voltage of the device. Active clamping will be explained in the next section, but essentially this technique, when used while turning off an inductive load, is known as self-clamped inductive switching (SCIS). The SCIS technique allows more energy to be absorbed by a device than a comparable device without active gate to drain clamping. However, there is a limit to how much energy the part can absorb, again limited by when the junction temperature exceeds the intrinsic temperature of the silicon. The point to realize is that during the SCIS event, the gate voltage is by definition at ground potential. Thus the control circuitry for the device is not biased and therefore the overtemperature limit circuit is not functional. The maximum energy rating for each device must be observed when switching inductive loads or

it is possible to experience device failure due to the die junction temperature exceeding the intrinsic temperature. In addition, even if the maximum energy rating is observed, sufficient time between SCIS pulses must be allowed so that the junction temperature can cool down back to the initial starting junction temperature. Otherwise, the junction temperature can ratchet up after each SCIS cycle, eventually reaching the intrinsic failure temperature.

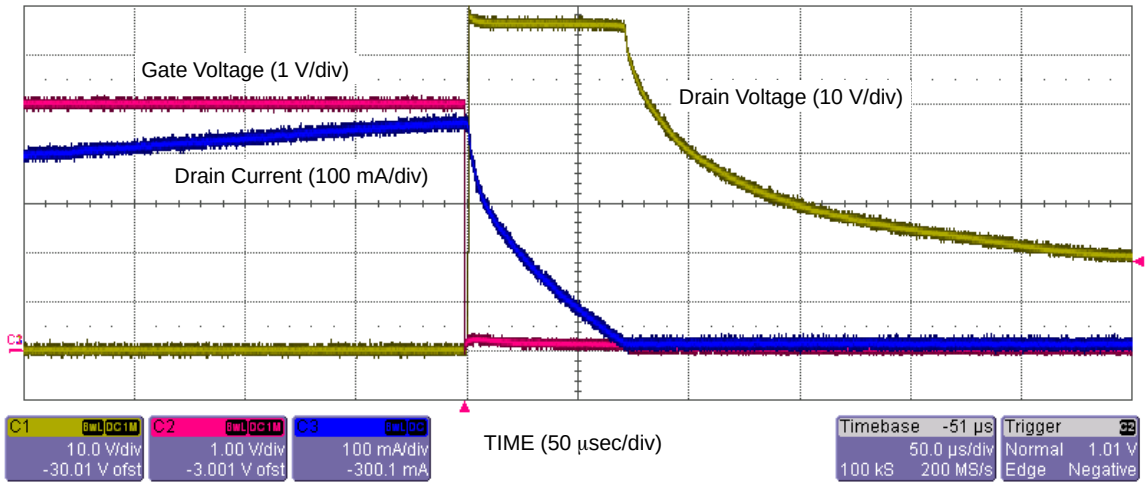


**Figure 11. NID6002 Driving 30 mH Fuel Injector, $V_{supply}$ = 12 V, Showing 67 V Active Clamp of Drain Voltage**

### Inductive Load Active Clamping

Figure 12 shows a simplified model of the HDPlus low-side active clamping components. The key component is the back-to-back Zener diode string located between the main power MOSFET gate and drain connections. The Zener voltage of this stack is designed to be less than the avalanche voltage of the main power MOSFET drain to source junction. When the drain voltage rises above the gate to drain Zener stack voltage, current will flow through the stack and thru $R_{g1}$ to ground, since the gate is switched off. Thus a voltage at the main power MOSFET gate is developed. The Zener current will be approximately equal to the power MOSFET gate voltage divided by $R_{g1}$.When this voltage nears threshold, the MOSFET begins to conduct load current in a forward, linear operation mode. The inductive energy is dissipated with a more uniform current density in the active region, since the device is turned on, as compared to dissipating the energy in an avalanche operation mode. Moreover, since the clamp voltage is lower than the avalanche voltage, the device dissipates less instantaneous power in an active clamp mode than in an avalanche mode. These behaviors afford the device greater energy handling capability when switching inductive loads in active clamp operation mode.

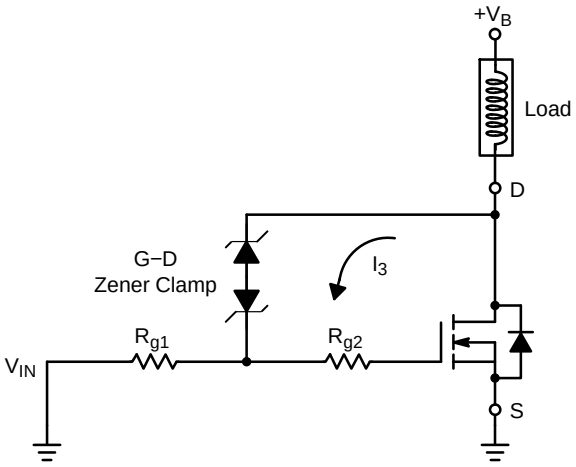


**Figure 12. Simplified Active Clamp Circuit**

### Switching Operation

As discussed earlier in the application note, resistive switching performance for HDPlus low-side MOSFETs is different from standard MOSFETs only in how much the internal series gate resistance affects transition times. The scope captures below show a fully protected HDPlus low-side MOSFET turn-on waveform compared to a comparable standard MOSFET with and without external series gate resistance. In these traces, gate voltage is turned

on to 5.0 V, switching a 3.4 Ω load from a 12 V supply. How series gate resistance affects switching transition is apparent by noting the time scales in the traces below.

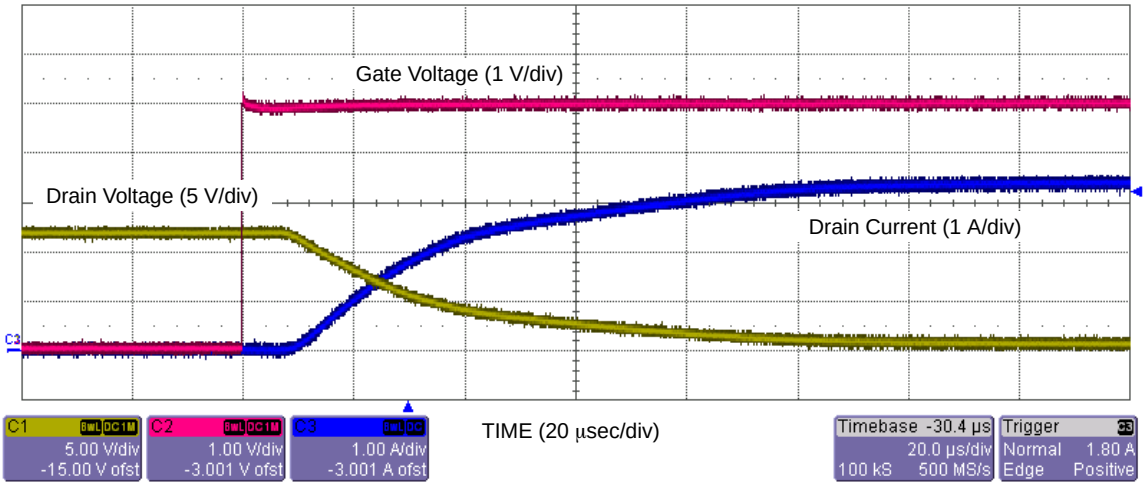


**Figure 13. NIF5002N Rise Time, Zero Ω External Gate Resistance**

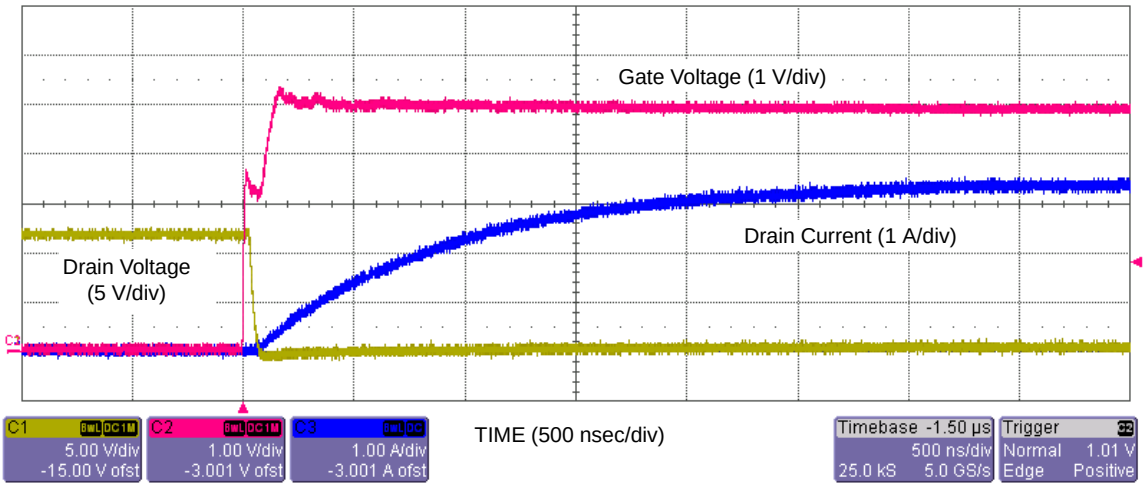


**Figure 14. NTD3055L170 Standard MOSFET Rise Time, Zero Ω Ext. Gate Resistance**

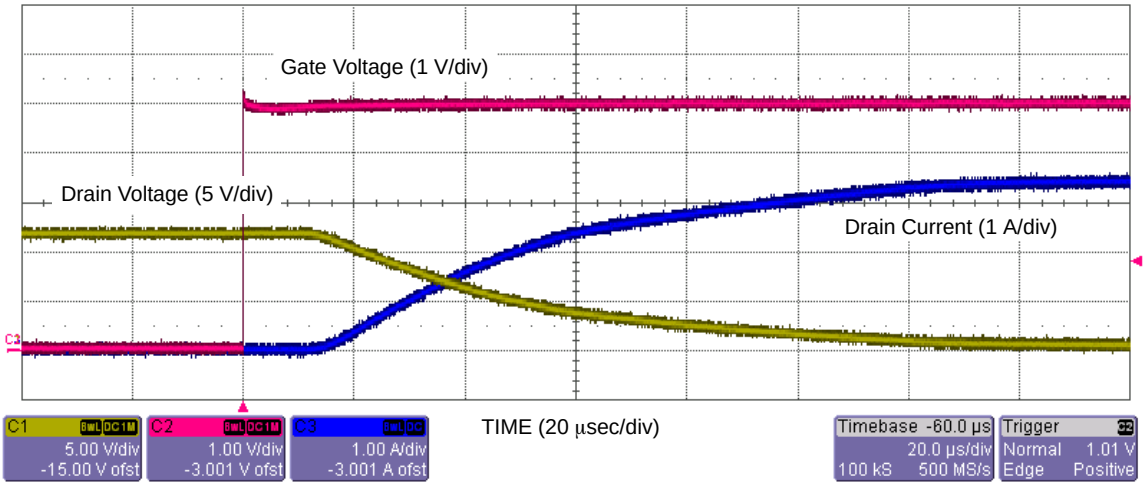


**Figure 15. NTD3055L170 Standard MOSFET Rise Time, 100 kΩ Ext. Gate Resistance**

### Voltage Transients

As with standard MOSFETs, the HDPlus low-side device family is designed to be compliant with the ISO7637 automotive transient specification. The worst case condition to consider is when the drain supply voltage line exceeds the clamp voltage when the device is turned off. This can result in a peak current flow approximately equal to $(V_{pk(transient)} - V_{clamp}) / R_{load}$. Since the gate is off in this situation, the protection control circuitry is inactive. Thus application circuit designs must consider expected peak transients, especially those of relatively long duration, and ensure the device is thermally capable of dissipating the power generated by transient pulse or pulses.

Figures 17, 18, and 19 were generated using the test circuit shown in Figure 15. The capacitor is charged to the desired peak transient and discharged at the drain of the test device through $R_i$ via a relay switch. In Figure 17, an NIF5002N survives a 52 V peak voltage, with $R_i$ = 3.4 Ω. The peak drain current is equal to (52 V − 47 V) / 3.4 Ω = 1.5 A, as seen in the picture. When the peak voltage is increased to 53 V, the same device fails, as seen in Figure 18. In this case, the power dissipated by the device, equal to $((V_{transient}(t) - V_{clamp}(t)) / R_i) * V_{clamp}(t)$, was sufficient to raise the junction temperature to $T_{intrinsic}$ after approximately 14 msec of pulse duration. Note that the failure point is where the current waveform becomes discontinuous. This example shows how surviving a load dump or other voltage transient on the supply line is a function of the application thermal design and depends on the load resistance and transient thermal resistance of the device. Figure 19 shows a NID5001N device surviving a 100 V peak transient pulse. In this case the load resistance, $R_{i,}$ is increased to 15.1 Ω, thereby decreasing the drain current and reducing power dissipation. Moreover, the NID5001N die active area is approximately eight times larger than the NIF5002N device so transient thermal response is greatly improved. In general, the higher the clamp voltage, the greater the load resistance, and the larger the die active area, the greater the peak transient drain voltage the device can survive.

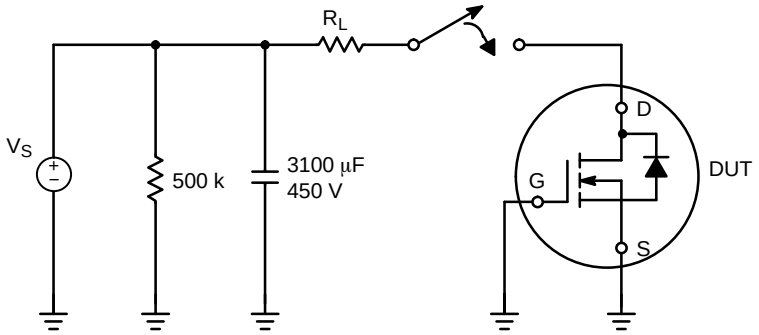


**Figure 16. Load Dump Test Circuit**

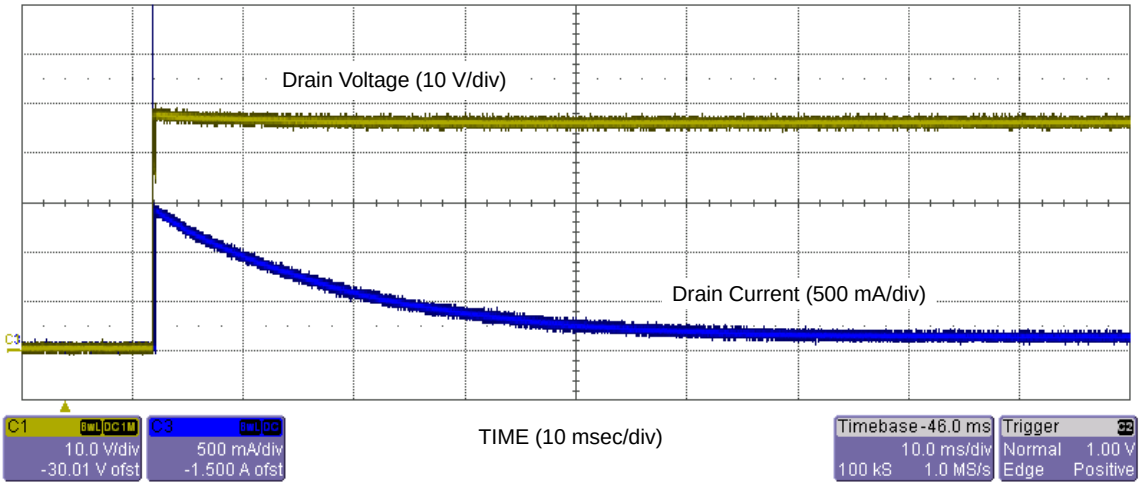


**Figure 17. NIF5002N Load Dump Transient, $V_{pk}$ = 52 V, Pass, $R_i$ = 3.4 Ω**

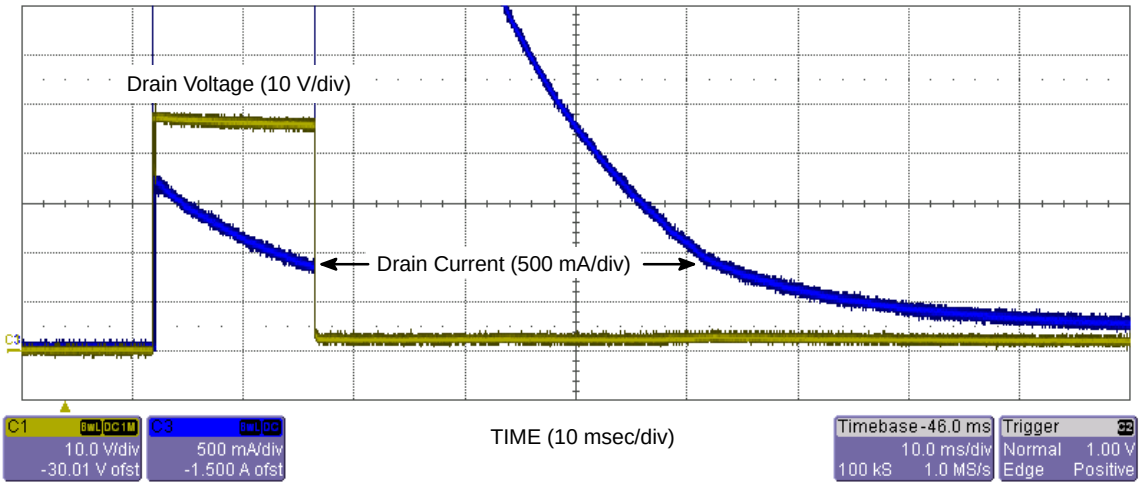


**Figure 18. NIF5002N Load Dump Transient, $V_{pk}$ = 53 V, Fail, $R_i$ = 3.4 Ω**

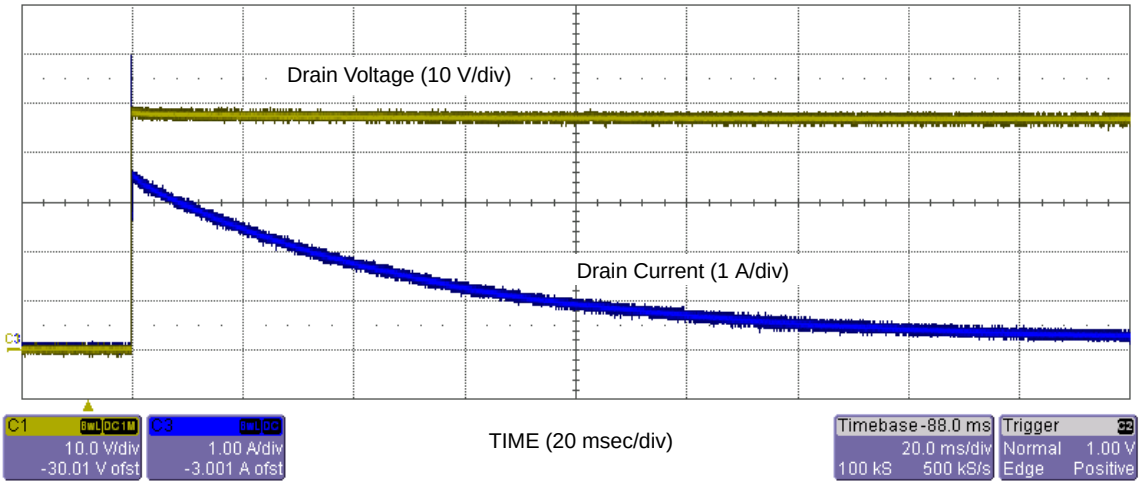


**Figure 19. NID5001N Load Dump, $V_{pk}$ = 100 V, Pass, $R_i$ = 15.1 Ω**

## Summary of Failure Modes

Although some of the HDPlus low-side devices are categorized as “fully-protected MOSFETs”, it is important to realize certain operation conditions can exist where the protection circuitry can not save the device from destruction. A summary table of potential device failure modes and mitigation strategies is shown below.

**Table 3. POTENTIAL DEVICE FAILURE MODES AND MITIGATION STRATEGIES**

| Potential Failure Mode | Mitigation |
|---|---|
| Insufficient gate drive during fault condition | − Increase current source/sink capability of gate drive circuit<br>− Increase gate drive voltage |
| Excessive dV/dt at drain | − Increase series gate resistance<br>− Filter or snubber circuits to eliminate fast edge transients<br>− Reduce supply voltage |
| Excessive die temperature during SCIS operation | − Reduce load inductance<br>− Reduce circuit parasitic inductance<br>− Use lower clamp voltage device<br>− Use device with proper energy rating<br>− Decrease device duty cycle or frequency or both<br>− Use parallel devices |
| Excessive die temperature during load dump or other transient event | − Increase load resistance<br>− Improve transient thermal response via better thermal pathway or larger silicon active area<br>− Use parallel devices |

## Summary

The HDPlus low-side device family offers an efficient monolithic solution to integrating protection features with vertical power MOSFET technology. The operation and application of these devices is the same as standard MOSFETs, assuming the gate drive circuit design allows for fault operation modes as described in this application note. Moreover it is important to note that the integrated protection features of the low-side devices can not protect against all failures modes. Careful design of the application circuit and environment can mitigate this issue.



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