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AND8173/D

Termination and Interface of ON Semiconductor ECL Devices With CML (Current Mode Logic) OUTPUT Structure

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APPLICATION NOTE

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Contents

Introduction

This document will discuss general termination and interface interconnection of On Semiconductor ECL devices with Current Mode Logic (CML) OUTPUT Structures. ECL has a long history of using a coupled emitter differential pair output structure with an Emitter Follower (EF) as shown in Figure 2. This classic EF output displays about 6 Ω – 8 Ω internal impedance in both LOW and HIGH output states. A constant internal current, I_{CS}, is steered through one side or the other by the two switching transistors. Now, some devices are available using CML outputs structures with internal impedance of 50 Ω as shown in Figures 1. On Semiconductor ECL CML devices offer back source termination to 50 Ω impedance and a potential reduction in external components.

Information regarding the Termination of ECL Devices with Emitter Follower (EF) OUTPUT Structure may be found in AND8020.

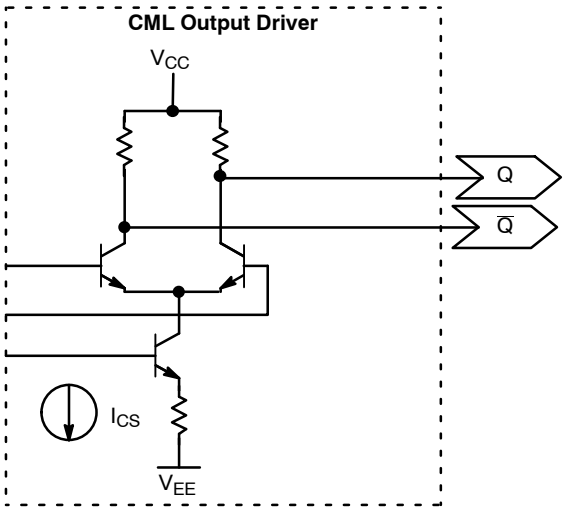

Figure 1. ECL with CML, Current Mode Logic Output Structures

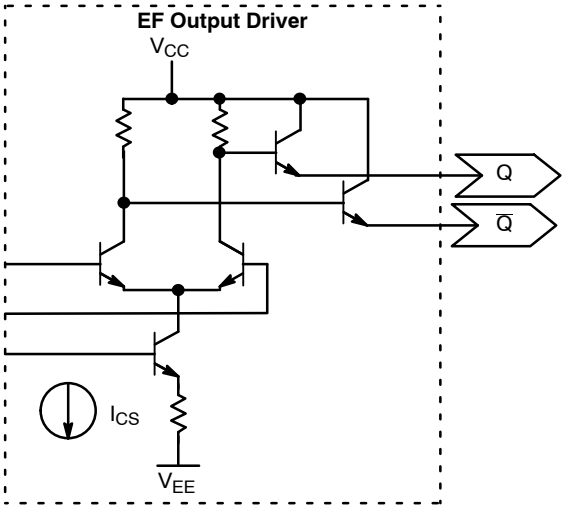

Figure 2. ECL with Emitter Follower Output, Output Structures

SECTION 1. UNLOADED CML DRIVER OUTPUT VOLTAGE LEVELS (DC OPEN)

This coupled emitter differential pair output structure incorporates an internal 16 mA constant source bias, I_{CS}, as "tail current". The unloaded open output voltages, V_{OPEN}, result from the internal current, I_{CS}, steered through each 50 Ω, R_C, collector resistor by the output transistors per Figures 3 and 4. The two output states, $Vout_{OPEN}$ HIGH and $Vout_{OPEN}$ LOW, are complementary. One output side of the differential pair will present an output voltage of V_{CC} − 800 mV, or $Vout_{OPEN}$ LOW due to the 16 mA I_{CS}, drawn through its R_C.

The complementary output side, $Vout_{OPEN}$ HIGH has essentially no current flow, I_{OFF}, and so will drop essentially 0 V across its R_C, thus remaining near V_{CC}. Switching is accomplished by steering the constant 16 mA I_{CS} tail current from one side to the other.

$$Vout_{OPEN}\ HIGH = V_{CC} - (I_{OFF} \cdot R_C) = V_{CC} - 0 \quad \text{(eq. 1)}$$

$$Vout_{OPEN}\ LOW = V_{CC} - (I_{CS} \cdot R_C) = V_{CC} - 800 \quad \text{(eq. 2)}$$

Where:

I_{CS} = Constant Current Source Bias

R_C = Output Transistor Collector Resistor

Unloaded (open) CML Outputs Q and $\overline{Q}$ will present either a $Vout_{OPEN}$ HIGH voltage level near V_{CC} or a $Vout_{OPEN}$ LOW voltage level of V_{CC} − 800 mV. An active complementary signal pair will produce characteristic parameters per Table 1.

Table 1. CML DRIVER LEVELS (with Open, Unloaded Outputs)

Parameter	Level	Unit
$Vout_{OPEN\ HIGH}$	V_{CC}	
$Vout_{OPEN\ CM}$	V_{CC} − 400	mV
$Vout_{OPEN\ LOW}$	V_{CC} − 800	mV
$Vout_{OPEN\ SE}$ (Note 1)	800	mVpp
$Vout_{OPEN\ DIFF}$	1600	mVpp

1. Each line measured single−ended.

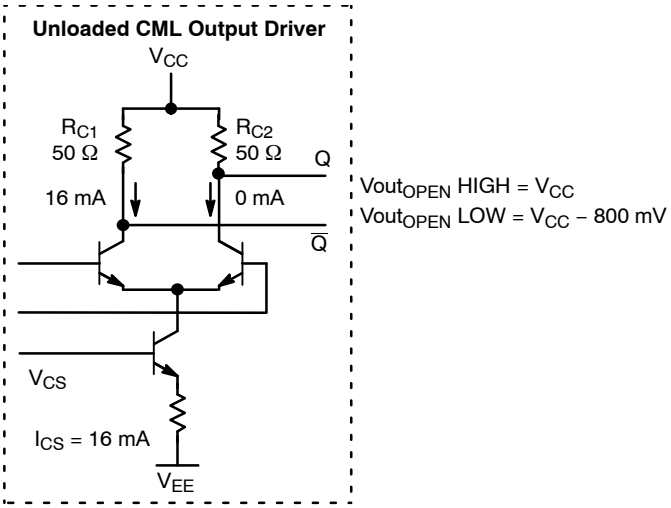

Figure 3. CML Open Output Driver Currents and Levels (Q HIGH, $\overline{Q}$ LOW)

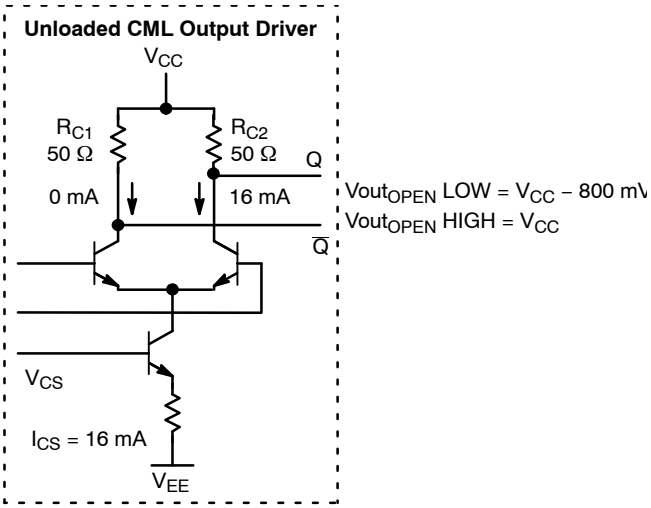

Figure 4. CML Open Output Driver Currents and Levels (Q LOW, $\overline{Q}$ HIGH)

SECTION 2. DIRECT CONNECT (DC) CML LOAD TERMINATED 50 Ω PER LINE TO V_{CC}

When the output is connected to a current source (loaded), the driver's internal constant 16 mA tail current, I_{CS}, now draws from the active side transistor through the internal 50 Ω, R_C (collector resistor), and also through the receiver's 50 Ω (R_T) termination to a current source. A typical receiver termination (internal or external termination resistor) is 50 Ω to V_{CC} as shown in Figures 5 and 6. Both output lines in a differential pair should have equal loads to maintain balanced dynamic signal loading to the driver. The complementary side draws essentially zero current, I_{off} and remains near V_{CC}.

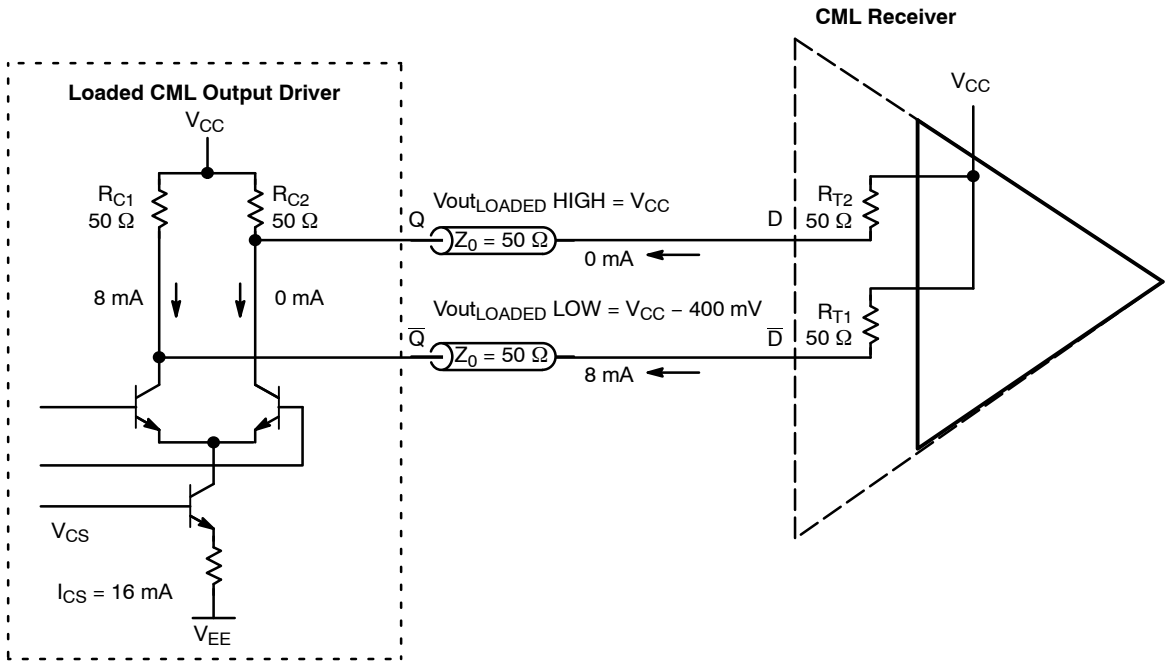

Figure 5. CML Output (with Direct Connect Load Termination of 50 Ω per line to V_{CC}), Currents and Levels (Q HIGH, $\overline{Q}$ LOW)

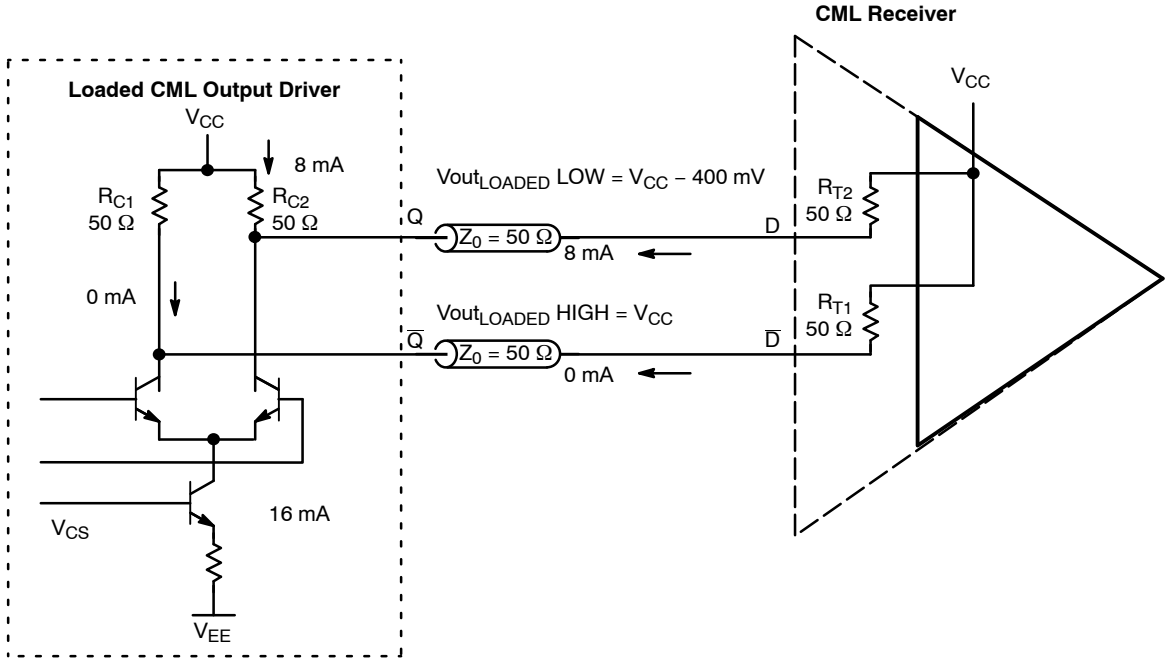

Figure 6. CML Output (with Direct Connect Load Termination of 50 Ω per line to V_{CC}), Currents and Levels (Q LOW, $\overline{Q}$ HIGH)

The driver 50 Ω R_C is in parallel to the receiver 50 Ω (R_T) to V_{CC}, presenting a $R_{(EQ)}$ of 25 Ω to the active side's constant 16 mA tail current, and will drop a total of about 400 mV below V_{CC} as the $Vout_{LOADED}$ LOW. The complementary output side, $Vout_{LOADED}$ HIGH, has essentially no current flow, I_{OFF}, remains near V_{CC}.

$$Vout_{LOADED}\ HIGH = V_{CC} - (I_{OFF} \cdot R_{(EQ)}) = V_{CC} - 0 \quad \text{(eq. 3)}$$

$$Vout_{LOADED}\ LOW = V_{CC} - (I_{CS} \cdot R_{(EQ)}) = V_{CC} - 400 \quad \text{(eq. 4)}$$

Where:

I_{CS} = Constant Source Bias

I_{OFF} = Zero Current Side

R_C = Output Transistor Collector Resistor

With differential CML Output lines loaded and each terminated 50 Ω (R_T) to V_{CC} at the driver, the voltage levels present either a $Vout_{LOADED}$ HIGH level of V_{CC} or $Vout_{LOADED}$ LOW of V_{CC} − 800 mV at the receiver. An active complementary signal pair produces the characteristic parameters per Table 2.

Table 2. CML DRIVER LEVELS (with Direct Connect Load Termination of 50 Ω to V_{CC})

Parameter	Level	Unit
$Vout_{LOADED}$ HIGH	V_{CC}	
$Vout_{LOADED}$ CM	V_{CC} − 200	mV
$Vout_{LOADED}$ LOW	V_{CC} − 400	mV
$Vout_{LOADED}$ SE (Note 2)	400	mVpp
$Vout_{LOADED}$ DIFF	800	mVpp

2. Each line measured single−ended.

SECTION 3. Cap Coupled (AC) CML LOAD TERMINATED 50 Ω PER LINE TO V_{term}

A driver and receiver using a cap, Cx, coupled (AC) differential interconnect and receiver side 50 Ω termination (R_T) requires a DC receiver side rebiasing, V_{term}, to the signal lines as shown in Figure 7. The coupling cap, Cx, value and the load impedance constitute an RC network affecting the signal edges. Cap coupling (AC) restricts low frequency response and may require coding to maintain a sufficient crossing density.

This AC coupled pair in Figure 7 will produce characteristic signal levels per Table 3.

Table 3. CML DRIVER LEVELS (with Cap Coupled Termination of 50 Ω per line to V_{CC})

Parameter	Receiver Level	Unit
$Vout_{AC}$ LOADED HIGH	V_{term} + 200	mV
$Vout_{AC}$ LOADED CM	V_{term}	mV
$Vout_{AC}$ LOADED LOW	V_{term} − 200	mV
$Vout_{AC}$ LOADED SE (Note 3)	400	mVpp
$Vout_{AC}$ LOADED DIFF	800	mVpp

3. Each line measured single−ended.

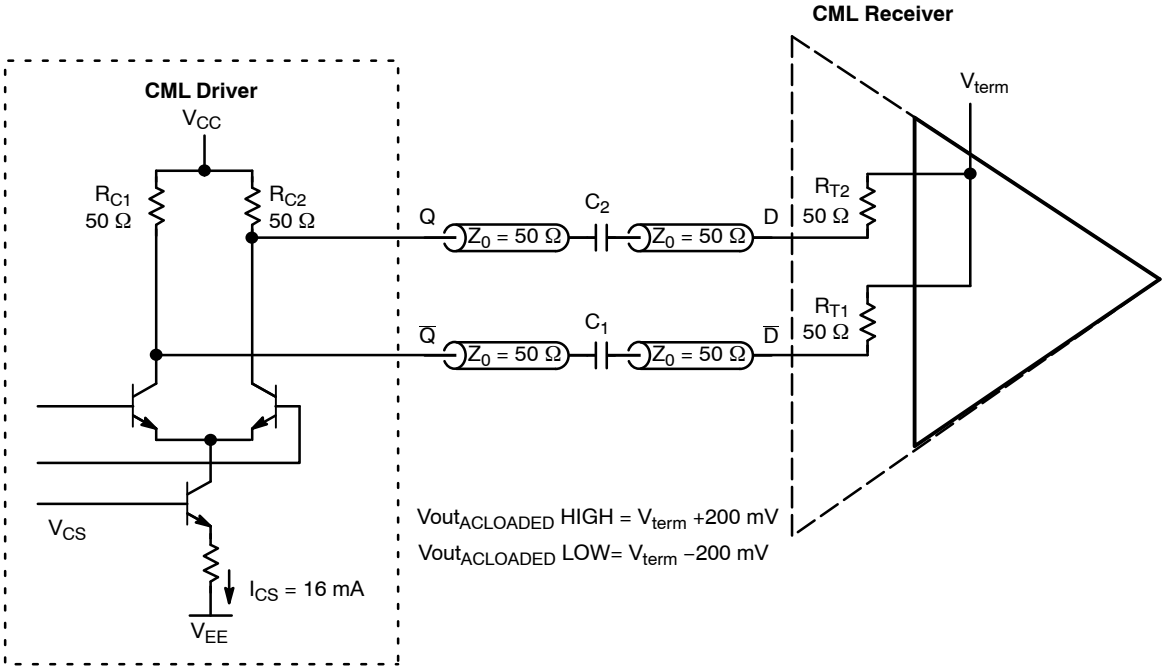

Figure 7. CML Output with Cap Coupling (AC) and Load Termination of 50 Ω to V_{term}

V_{term} SUPPLY

The V_{term} DC bias supply associated with the CML receiver in Figure 7 needs to accommodate the receiver common mode range and bypassed to enhance rejection of common mode noise. Typically, the V_{term} bias supply may be connected directly from the receiver R_T pins whether internal or external to the driver. When internal, the pin connect to the fixed value 50 Ω (R_T) resistors may be singulated or combined. If external, the termination resistor (R_T) value may be changed to accommodate the specific transmission line impedance.

An external DC reference supply, V_{term}, may be generated by a resistor divider network spanning from the V_{CC} to V_{EE} supplies, with appropriate bypass capacitance, C_{BP}, as shown in Figure 8. Typically bypass capacitor value may range from 0.01 μF to 0.001 μF. Resistors R1 and R2 should generate an appropriate common mode voltage for the receiver. Current through R2 should be at least 10X the receiver typical input current for both lines.

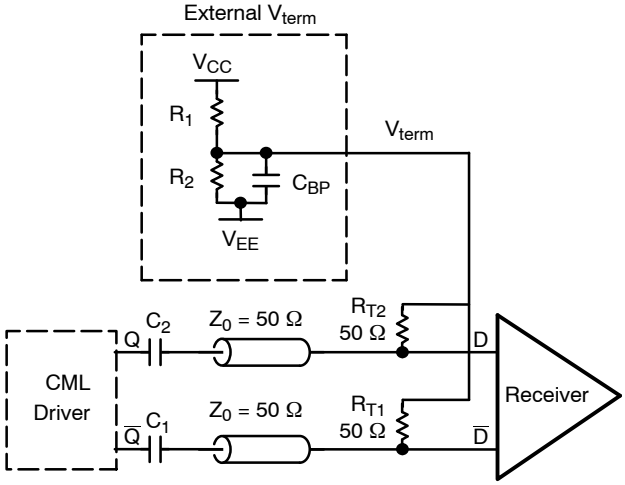

Figure 8. Typical V_{term} Supply Divider Network

Alternatively, a receiver without internal 50 Ω (R_T) resistors may be terminated and DC biased by using a Thevenin parallel equivalent network. Both impedance matching and DC rebias are simultaneously accomplished by a solution of a R1 resistor to V_{CC} and a R2 resistor to V_{EE} as shown in Figure 9, on each of the complementary lines. See AND8020, Section 3 Thevenin Equivalent Parallel Termination for equations generating the values of R1 and R2.

LVPECL receivers offer a wide range of accepted common mode value solutions for inputs operating in a differential interconnect. Selecting a common mode value of V_{CC} − 1.3 V would satisfy any standard ECL receiver. Table 4 gives values for the typical pullup resistor to V_{CC} (R1 or R1'), the pulldown resistor to V_{EE} (R2 or R2'), and the resulting V_{rebias} voltage when using V_{CC} − 1.3 common mode voltage and impedance matching to transmission media with Z_0 = 50 Ω.

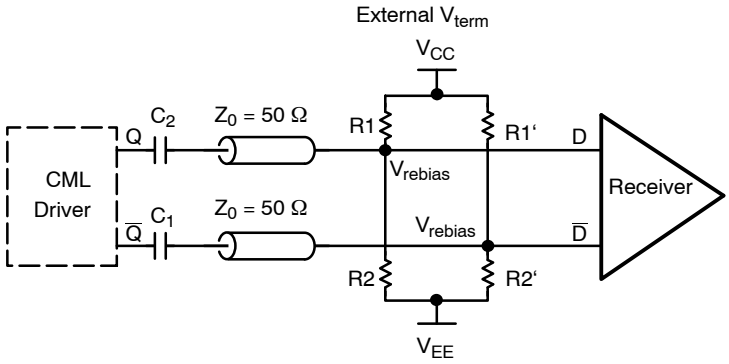

Figure 9. Thevenin Parallel Termination Scheme

Table 4. Typical V_{CC} − 1.3 REBIAS AND IMPEDANCE MATCHING RESISTOR NETWORK VALUES @ Z_0 = 50 Ω

Resistor	$\lvert V_{CC} - V_{EE} \rvert$ = 5.0 V	$\lvert V_{CC} - V_{EE} \rvert$ = 3.3 V	$\lvert V_{CC} - V_{EE} \rvert$ = 2.5 V	Unit
R1 (R1')	68	83	96.15	Ω
R2 (R2')	192	127	104.16	Ω
V_{rebias}	3.7	2.0	1.2	V

SECTION 4. CML INTERFACE INTERCONNECTS

CML Driver Direct Connect (DC) to LVPECL

The ON Semiconductor ECL Logic Devices with CML OUTPUT Structures easily interconnects directly (DC) to a typical LVPECL receiver input on similar power supplies. A direct (DC) interface interconnect is shown in Figure 10.

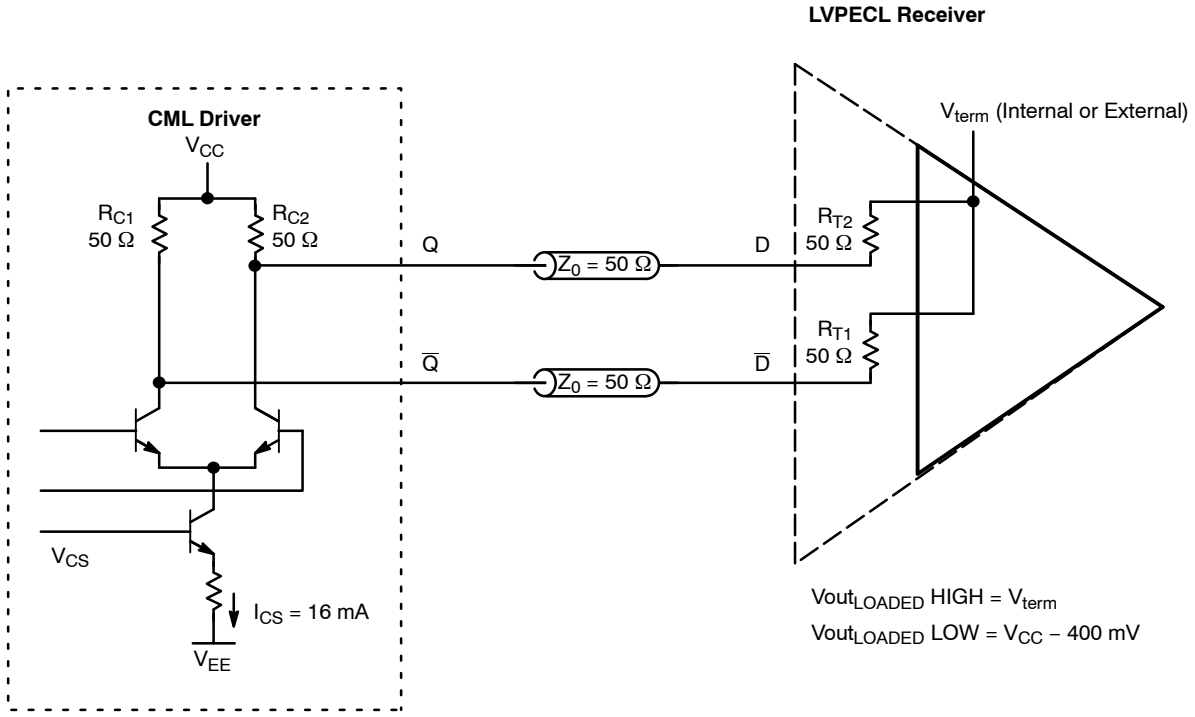

Figure 10. CML Output with Direct (DC) Interconnect and Termination of 50 Ω to V_{term}

A receiver may have either internal or external 50 Ω (R_T) termination resistors, and these resistors may be singulated or combined for pinout. If external, the termination resistors (R_T) value may be changed to accommodate the transmission line impedance.

The V_{term} supply (Figure 8) connects to the 50 Ω (R_T) termination resistors and determines the receiver DC bias level. A proper V_{term} DC bias must be selected for the receiver to comply with common mode specifications, such as VIHCMR or VCMR. Most devices will tolerate V_{term} at V_{CC} while others may spec a signal HIGH level, VIHmax (consult device data sheet) requiring an appropriately lower V_{term} supply. A lower V_{term} supply affects the receiver $Vout_{HIGH}$ and $Vout_{LOW}$ levels. A typical On Semiconductor ECL Device with CML OUTPUT Structure, directly (DC) driving an internally terminated LVPECL input with various V_{term} values, produces a characteristic swing amplitude, $Vout_{PP}$ (each line is measured single ended), and a common mode voltage, $Vout_{CM}$, presented in Table 5. Both CML driver and LVPECL receiver were supplied V_{CC} @ 3.3 V. Note the insensitivity of the output swing to changes in the V_{term} supply as it ranges from V_{CC} to V_{CC} – 2.0 V, the typical V_{TT} termination voltage for Emitter Follower ECL structures.

Table 5. CML DRIVER LEVELS (WITH DIRECT CONNECT TERMINATION OF 50 Ω PER LINE TO V_{term})

V_{term}	$Vout_{CM}$	$Vout_{HIGH}$	$Vout_{LOW}$	$Vout_{PP}$ (Note 4)	Unit
3.3	3.1	3.25	2.95	0.300	V
3.0	2.95	3.10	2.85	0.300	V
2.5	2.75	2.85	2.55	0.295	V
2.0	2.45	2.60	2.30	0.280	V

4. Each line measured single−ended

CML Driver Cap Coupled (AC) to Various Supplied ECL: PECL, LVPECL, LVNECL, NECL

The On Semiconductor ECL Devices with CML OUTPUT Structures easily interconnect with cap coupling (AC) to ECL type receiver inputs operating with different supply modes such as shown in Figures 11, 12, and 13.

A V_{term} supply is used to DC bias the receiver input lines. See also V_{term} Supply**,** Figure 8 and Table 4.

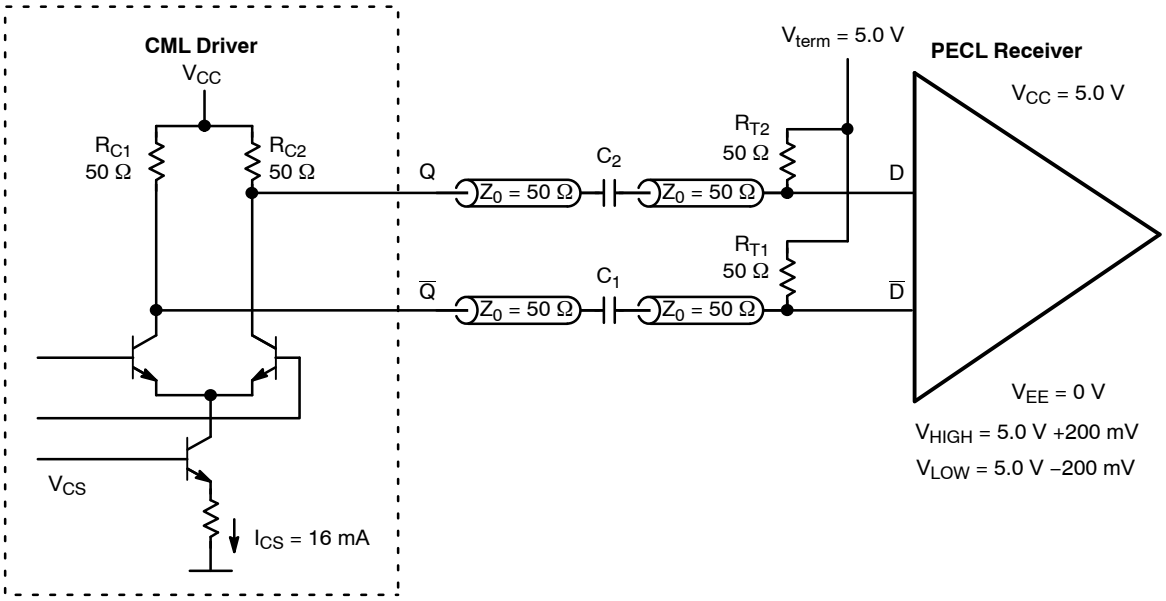

Figure 11. CML to PECL (V_{CC} = V_{term} = 5.0 V, V_{EE} = 0 V)

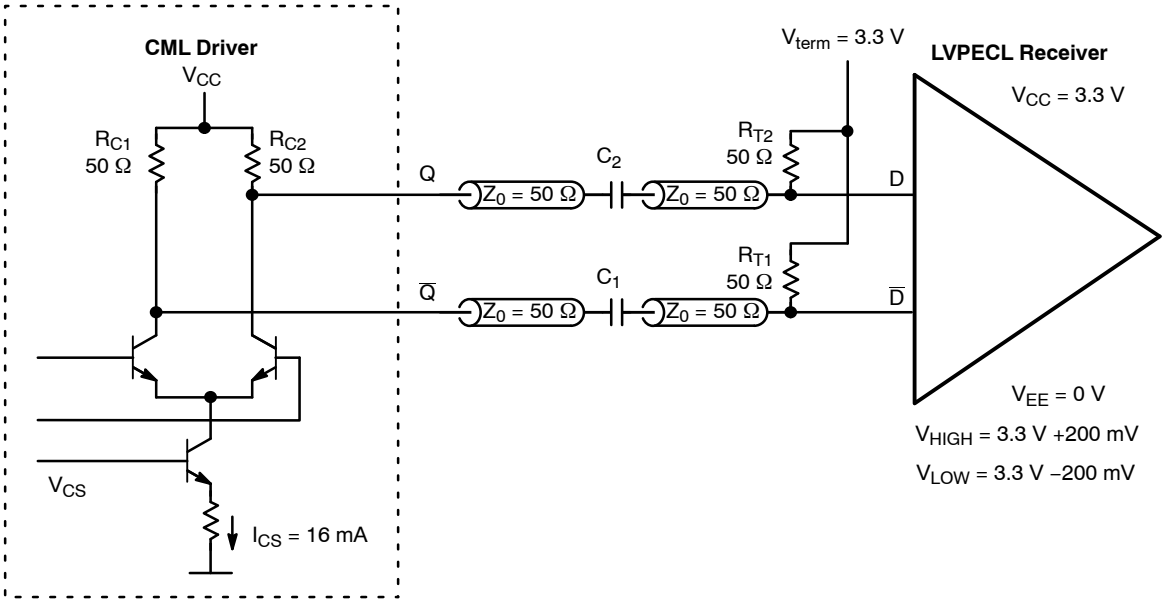

Figure 12. CML to LVPECL (V_{CC} = V_{term} = 3.3 V, V_{EE} = 0 V)

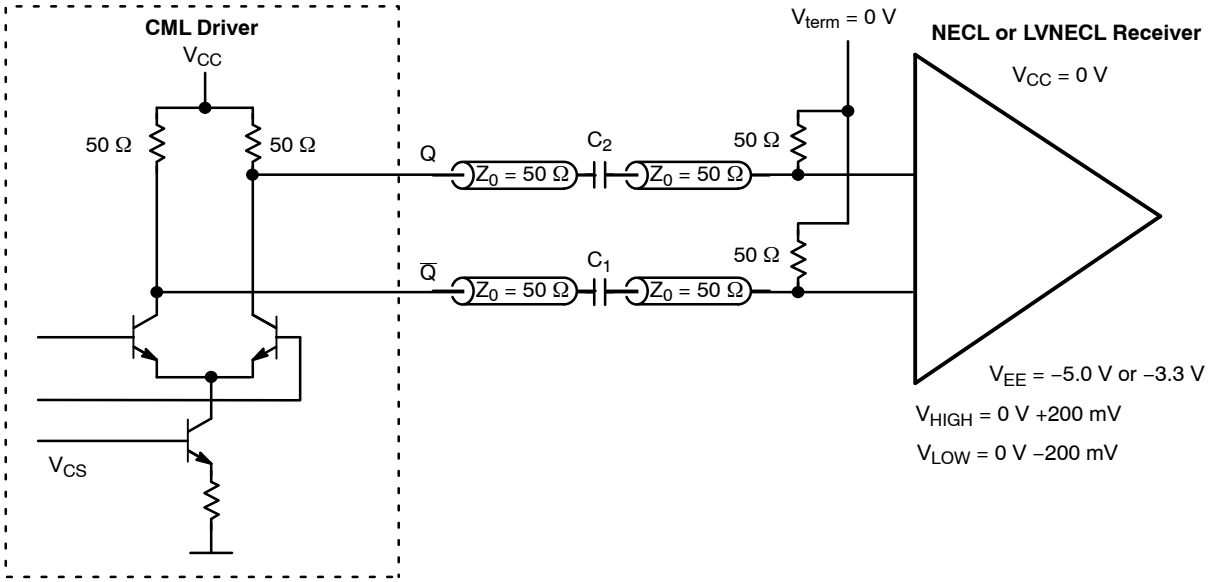

Figure 13. CML to NECL (V_{term} = 0 V, V_{EE} = −5.0 V or −3.3 V)

CML Driver Cap Coupled (AC) to LVDS

A CML Driver interconnect to an LVDS (LVDS, BLVDS, M−LVDS, GLVDS, or LVDM) compliant receiver requires a cap coupled (AC) interface. Typically, a 50 Ω (R_T) per line impedance matching termination to V_{term} is used as shown in Figure 14, and will produce a V_{HIGH} of about 1.33 V, a V_{LOW} of 1.0 V, with an amplitude of 330 mVpp (each line measured single−ended). The V_{CM} is set to 1.2 V by the V_{term} reference.

If the two 50 Ω (R_T) per line impedance matching termination resistors are external, the termination resistor scheme may be modified by using a Thevenin parallel scheme as shown in Figure 9. The Thevenin parallel impedance matching resistor network values and rebias voltage for an LVDS cap coupled receiver with Z_0 = 50 Ω are given in Table 6.

Table 6. LVDS IMPEDANCE MATCHING RESISTOR NETWORK VALUES AND REBIAS VOLTAGE

Resistor	$\|V_{CC} - V_{EE}\|$ = 5.0 V	$\|V_{CC} - V_{EE}\|$ = 3.3 V	$\|V_{CC} - V_{EE}\|$ = 2.5 V	Unit
R1 (R1')	210	138	104	Ω
R2 (R2')	66	79	96	Ω
V_{rebias}	1.2	1.2	1.2	V

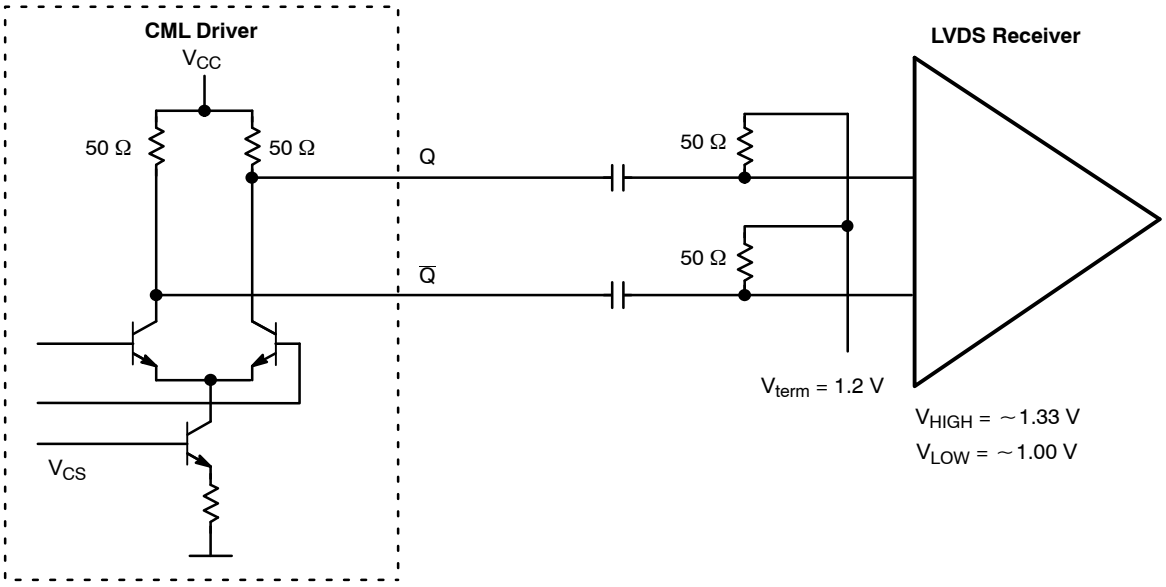

Figure 14. CML to LVDS (V_{term} = 1.2 V)

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