

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

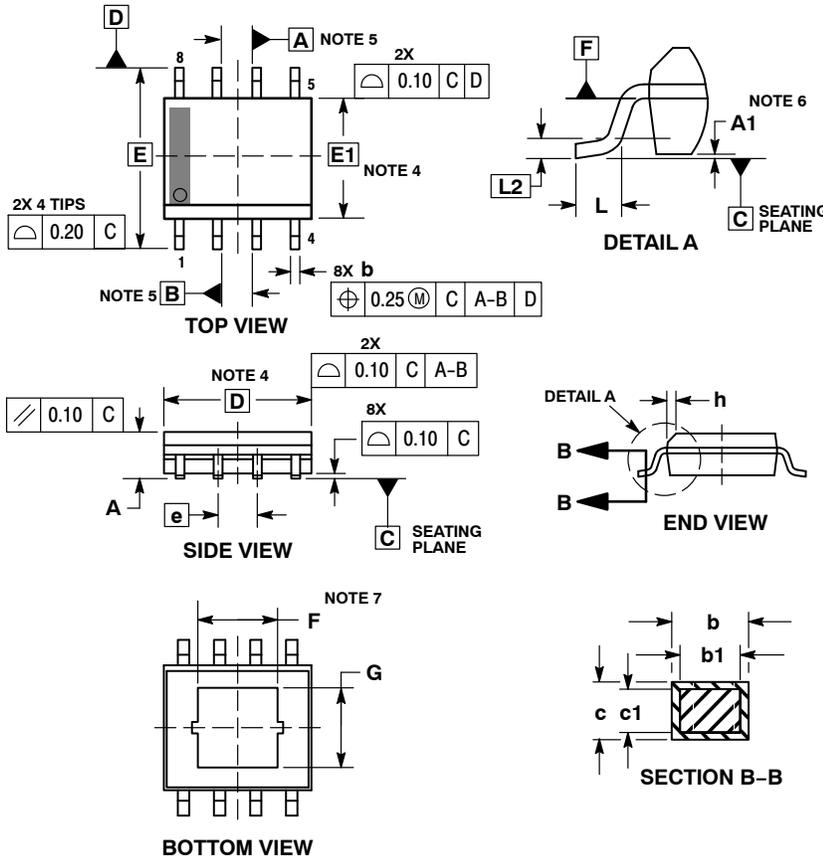
ON Semiconductor®



SCALE 1:1

SOIC8-NB EP CASE 751BU ISSUE E

DATE 01 APR 2015

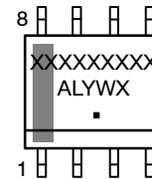


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION *D* DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSION *E* DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE. DIMENSIONS *D* AND *E* ARE DETERMINED AT DATUM *F*.
5. DIMENSIONS *A* AND *B* ARE TO BE DETERMINED AT DATUM *F*.
6. *A1* IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. TAB CONTOUR MAY VARY MINIMALLY TO INCLUDE TOOLING FEATURES.

MILLIMETERS		
DIM	MIN	MAX
A	1.35	1.75
A1	0.00	0.10
<i>b</i>	0.31	0.51
<i>b1</i>	0.28	0.48
<i>c</i>	0.17	0.25
<i>c1</i>	0.17	0.23
<i>D</i>	4.90	BSC
<i>E</i>	6.00	BSC
<i>E1</i>	3.90	BSC
<i>e</i>	1.27	BSC
<i>F</i>	1.55	2.39
<i>G</i>	1.55	2.39
<i>h</i>	0.25	0.50
<i>L</i>	0.40	1.27
<i>L2</i>	0.25	BSC

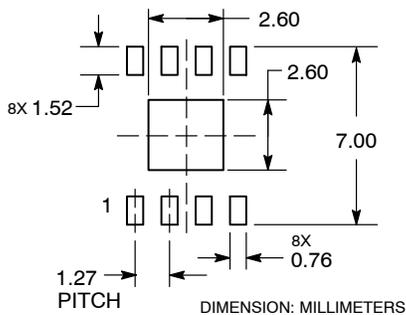
GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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