

# Quad 2:1 Multiplexer/ Demultiplexer Bus Switch

## 74FST3257

The onsemi 74FST3257 is a quad 2:1, high performance multiplexer/demultiplexer bus switch. The device is CMOS TTL compatible when operating between 4 and 5.5 Volts. The device exhibits extremely low  $R_{ON}$  and adds nearly zero propagation delay. The device adds no noise or ground bounce to the system.

### Features

- $R_{ON} < 4 \Omega$  Typical
- Less Than 0.25 ns–Max Delay Through Switch
- Nearly Zero Standby Current
- No Circuit Bounce
- Control Inputs are TTL/CMOS Compatible
- Pin-For-Pin Compatible With QS3257, FST3257, CBT3257
- All Popular Packages: SOIC-16, TSSOP-16, QFN16
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

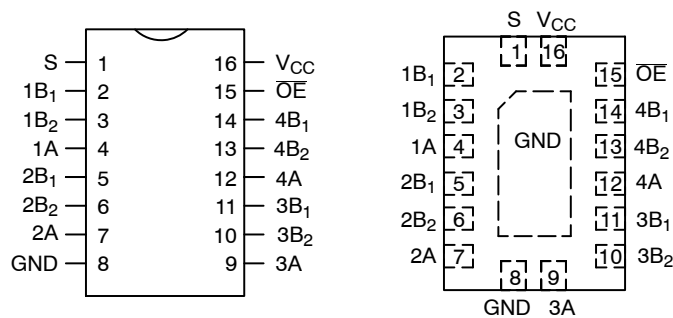
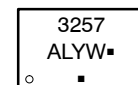
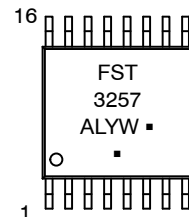
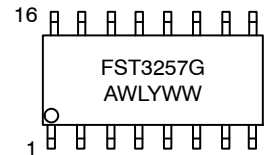


Figure 1. 16-Lead Pinout Diagrams

S	OE	Function
X	H	Disconnect
L	L	A = B <sub>1</sub>
H	L	A = B <sub>2</sub>

Figure 2. Truth Table

### MARKING DIAGRAMS



A = Assembly Location  
WL, L = Wafer Lot  
Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

### PIN NAMES

Pin	Description
$\overline{OE}_1, \overline{OE}_2$	Bus Switch Enables
S <sub>0</sub> , S <sub>1</sub>	Select Inputs
A	Bus A
B <sub>1</sub> , B <sub>2</sub> , B <sub>3</sub> , B <sub>4</sub>	Bus B

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# 74FST3257

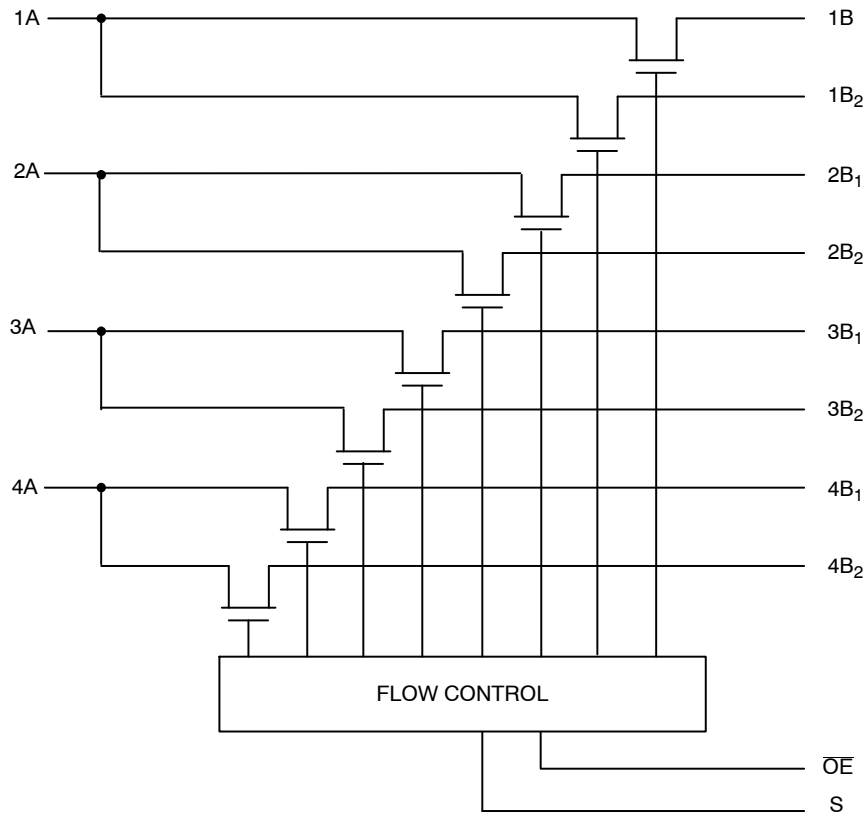


Figure 3. Logic Diagram

## ORDERING INFORMATION

Device Order Number	Package	Shipping <sup>†</sup>
74FST3257DR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
NLV74FST3257DR2G*		
74FST3257DTR2G	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel
74FST3257MNTWG	QFN16 (Pb-Free)	3000 Units / Tape & Reel
74FST3257MN2TWG	QFN16 (Pb-Free)	3000 Units / Tape & Reel (4mm pitch carrier tape)

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

**MAXIMUM RATINGS**

Symbol	Parameter	Value	Units
$V_{CC}$	DC Supply Voltage	-0.5 to +7.0	V
$V_I$	DC Input Voltage	-0.5 to +7.0	V
$V_O$	DC Output Voltage	-0.5 to +7.0	V
$I_{IK}$	DC Input Diode Current $V_I < GND$	-50	mA
$I_{OK}$	DC Output Diode Current $V_O < GND$	-50	mA
$I_O$	DC Output Sink Current	128	mA
$I_{CC}$	DC Supply Current per Supply Pin	$\pm 100$	mA
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 100$	mA
$T_{STG}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds	260	$^{\circ}C$
$T_J$	Junction Temperature Under Bias	+150	$^{\circ}C$
$\theta_{JA}$	Thermal Resistance SOIC TSSOP QFN	125 170 N/A	$^{\circ}C/W$
MSL	Moisture Sensitivity	Level 1	
$F_R$	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
$V_{ESD}$	ESD Withstand Voltage Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	> 2000 > 200 N/A	V
$I_{Latchup}$	Latchup Performance Above $V_{CC}$ and Below GND at 85 $^{\circ}C$ (Note 4)	$\pm 500$	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22-A114-A.
2. Tested to EIA/JESD22-A115-A.
3. Tested to JESD22-C101-A.
4. Tested to EIA/JESD78.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Units
$V_{CC}$	Supply Voltage Operating, Data Retention Only	4.0	5.5	V
$V_I$	Input Voltage (Note 5)	0	5.5	V
$V_O$	Output Voltage (HIGH or LOW State)	0	5.5	V
$T_A$	Operating Free-Air Temperature	-40	+85	$^{\circ}C$
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate Switch I/O		DC 5	ns/V
	Switch Control Input $V_{CC} = 5.0 V \pm 0.5 V$	0		

5. Unused control inputs may not be left open. All control inputs must be tied to a high or low logic input voltage level.

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C			Units
				Min	Typ*	Max	
V <sub>IK</sub>	Clamp Diode Voltage	I <sub>IN</sub> = -18 mA	4.5			-1.2	V
V <sub>IH</sub>	High-Level Input Voltage		4.0 to 5.5	2.0			V
V <sub>IL</sub>	Low-Level Input Voltage		4.0 to 5.5			0.8	V
I <sub>I</sub>	Input Leakage Current	0 ≤ V <sub>IN</sub> ≤ 5.5 V	5.5			±1.0	μA
I <sub>OZ</sub>	Off-State Leakage Current	0 ≤ A, B ≤ V <sub>CC</sub>	5.5			±1.0	μA
R <sub>ON</sub>	Switch On Resistance (Note 6)	V <sub>IN</sub> = 0 V, I <sub>IN</sub> = 64 mA	4.5		4	7	Ω
		V <sub>IN</sub> = 0 V, I <sub>IN</sub> = 30 mA	4.5		4	7	
		V <sub>IN</sub> = 2.4 V, I <sub>IN</sub> = 15 mA	4.5		8	15	
		V <sub>IN</sub> = 2.4 V, I <sub>IN</sub> = 15 mA	4.0		11	20	
I <sub>CC</sub>	Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND, I <sub>OUT</sub> = 0	5.5			3	μA
ΔI <sub>CC</sub>	Increase In I <sub>CC</sub> per Input	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5			2.5	mA

\*Typical values are at V<sub>CC</sub> = 5.0 V and T<sub>A</sub> = 25°C.

6. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF, R <sub>U</sub> = R <sub>D</sub> = 500 Ω				Units
			V <sub>CC</sub> = 4.5-5.5 V		V <sub>CC</sub> = 4.0 V		
			Min	Max	Min	Max	
t <sub>PHL</sub> , t <sub>PLH</sub>	Prop Delay Bus to Bus (Note 7)	V <sub>I</sub> = OPEN		0.25		0.25	ns
	Prop Delay, Select to Bus A		1.0	4.7		5.2	
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time, Select to Bus B	V <sub>I</sub> = 7 V for t <sub>PZL</sub>	1.0	5.2		5.7	ns
	Output Enable Time, I <sub>OE</sub> to Bus A, B	V <sub>I</sub> = OPEN for t <sub>PZH</sub>	1.0	5.1		5.6	
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time, Select to Bus B	V <sub>I</sub> = 7 V for t <sub>PLZ</sub>	1.0	5.2		5.5	ns
	Output Disable Time, I <sub>OE</sub> to Bus A, B	V <sub>I</sub> = OPEN for t <sub>PHZ</sub>	1.0	5.5		5.5	

7. This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

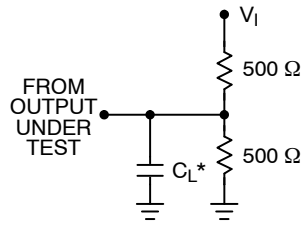
## CAPACITANCE (Note 8)

Symbol	Parameter	Conditions	Typ	Max	Units
C <sub>IN</sub>	Control Pin Input Capacitance	V <sub>CC</sub> = 5.0 V	3		pF
C <sub>I/O</sub>	A Port Input/Output Capacitance	V <sub>CC</sub> , $\overline{OE}$ = 5.0 V	7		pF
C <sub>I/O</sub>	B Port Input/Output Capacitance	V <sub>CC</sub> , $\overline{OE}$ = 5.0 V	5		pF

8. T<sub>A</sub> = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

# 74FST3257

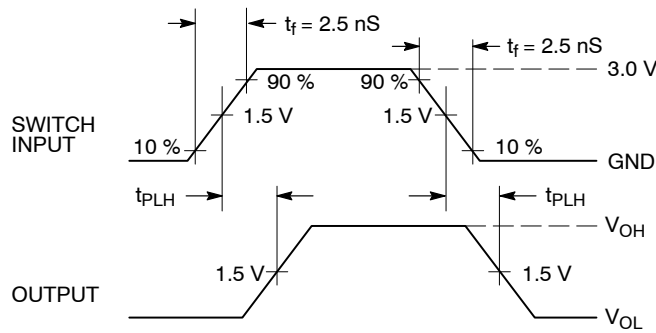
## AC Loading and Waveforms



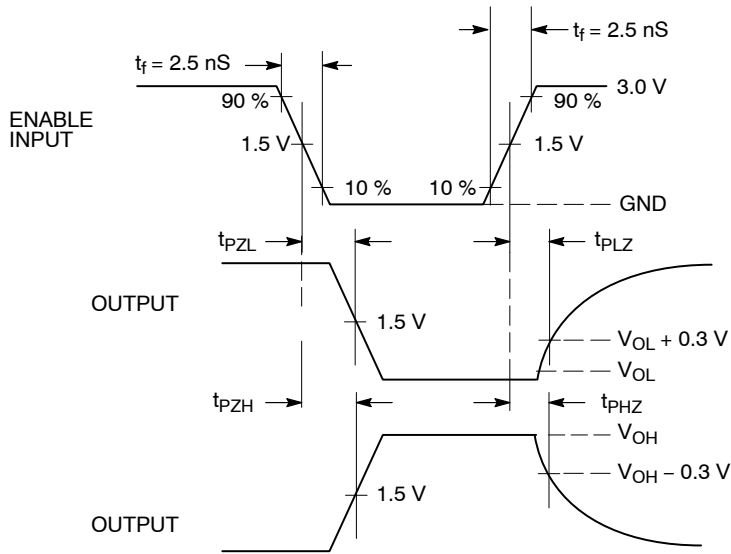
**NOTES:**

1. Input driven by 50 Ω source terminated in 50 Ω.
  2. CL includes load and stray capacitance.
- \*C<sub>L</sub> = 50 pF

**Figure 4. AC Test Circuit**



**Figure 5. Propagation Delays**



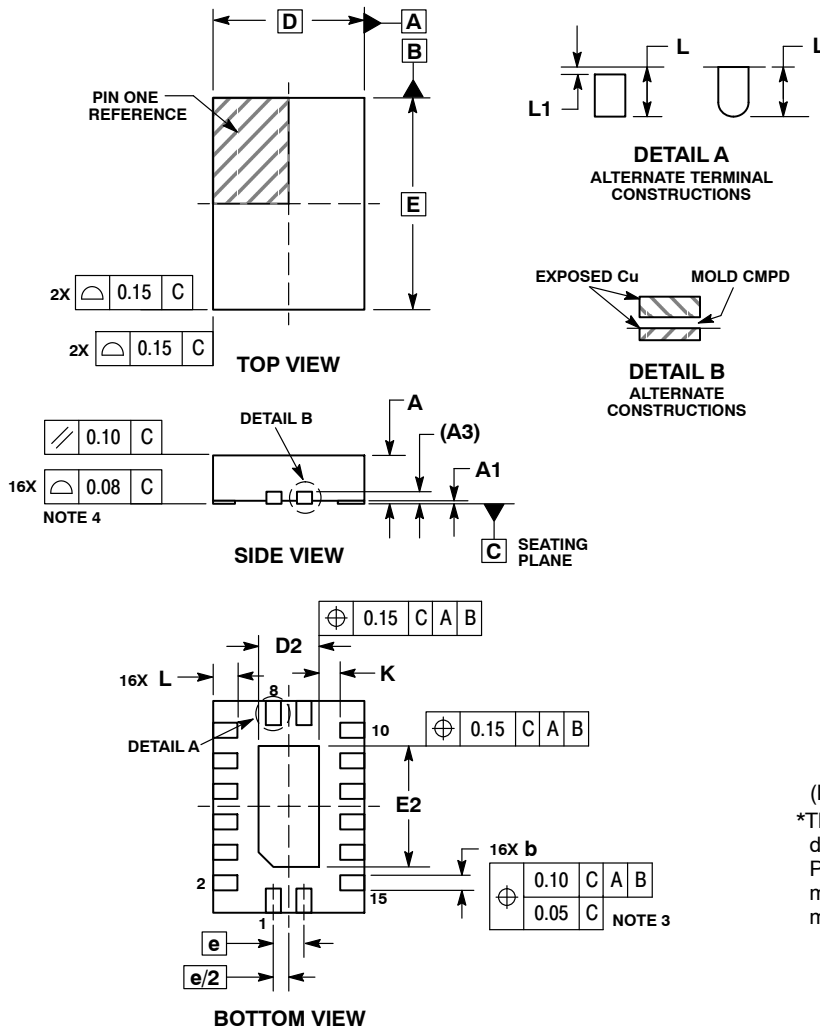
**Figure 6. Enable/Disable Delays**



SCALE 2:1

QFN16, 2.5x3.5, 0.5P  
CASE 485AW  
ISSUE O

DATE 11 DEC 2008

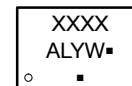


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.50 BSC	
D2	0.85	1.15
E	3.50 BSC	
E2	1.85	2.15
e	0.50 BSC	
K	0.20	---
L	0.35	0.45
L1	---	0.15

GENERIC MARKING  
DIAGRAM\*

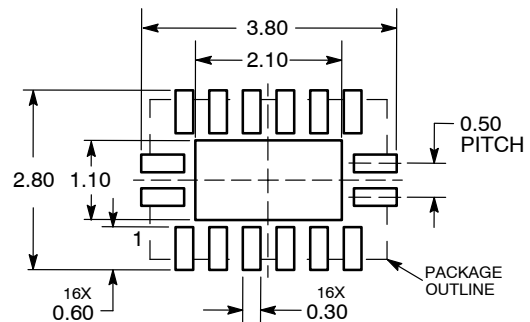


- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED  
SOLDERING FOOTPRINT\*

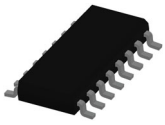


DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	QFN16, 2.5X3.5, 0.5P	PAGE 1 OF 1

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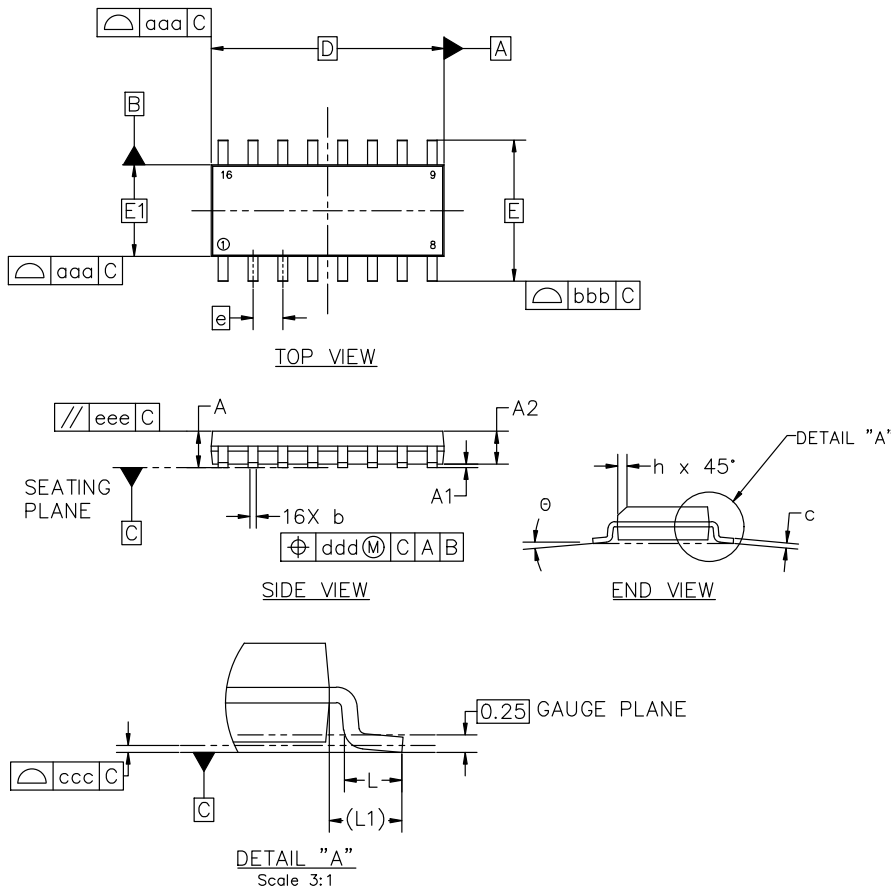


**SOIC-16 9.90x3.90x1.50 1.27P**  
CASE 751B  
ISSUE L

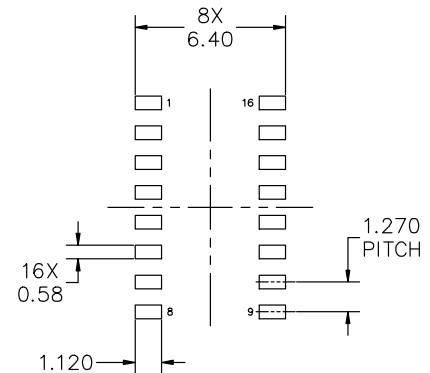
DATE 29 MAY 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

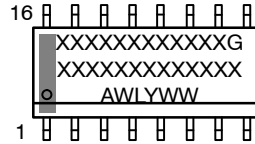
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<b>DESCRIPTION:</b>	<b>SOIC-16 9.90X3.90X1.50 1.27P</b>	<b>PAGE 1 OF 2</b>

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**SOIC-16 9.90x3.90x1.50 1.27P**  
**CASE 751B**  
**ISSUE L**

DATE 29 MAY 2024

**GENERIC  
MARKING DIAGRAM\***



XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

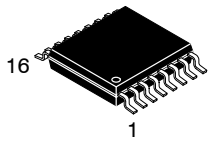
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

<p><b>STYLE 1:</b></p> <p>PIN 1. COLLECTOR  2. BASE  3. EMITTER  4. NO CONNECTION  5. EMITTER  6. BASE  7. COLLECTOR  8. COLLECTOR  9. BASE  10. EMITTER  11. NO CONNECTION  12. EMITTER  13. BASE  14. COLLECTOR  15. EMITTER  16. COLLECTOR</p>	<p><b>STYLE 2:</b></p> <p>PIN 1. CATHODE  2. ANODE  3. NO CONNECTION  4. CATHODE  5. CATHODE  6. NO CONNECTION  7. ANODE  8. CATHODE  9. CATHODE  10. ANODE  11. NO CONNECTION  12. CATHODE  13. CATHODE  14. NO CONNECTION  15. ANODE  16. CATHODE</p>	<p><b>STYLE 3:</b></p> <p>PIN 1. COLLECTOR, DYE #1  2. BASE, #1  3. EMITTER, #1  4. COLLECTOR, #1  5. COLLECTOR, #2  6. BASE, #2  7. EMITTER, #2  8. COLLECTOR, #2  9. COLLECTOR, #3  10. BASE, #3  11. EMITTER, #3  12. COLLECTOR, #3  13. COLLECTOR, #4  14. BASE, #4  15. EMITTER, #4  16. COLLECTOR, #4</p>	<p><b>STYLE 4:</b></p> <p>PIN 1. COLLECTOR, DYE #1  2. COLLECTOR, #1  3. COLLECTOR, #2  4. COLLECTOR, #2  5. COLLECTOR, #3  6. COLLECTOR, #3  7. COLLECTOR, #4  8. COLLECTOR, #4  9. BASE, #4  10. EMITTER, #4  11. BASE, #3  12. EMITTER, #3  13. BASE, #2  14. EMITTER, #2  15. BASE, #1  16. EMITTER, #1</p>
<p><b>STYLE 5:</b></p> <p>PIN 1. DRAIN, DYE #1  2. DRAIN, #1  3. DRAIN, #2  4. DRAIN, #2  5. DRAIN, #3  6. DRAIN, #3  7. DRAIN, #4  8. DRAIN, #4  9. GATE, #4  10. SOURCE, #4  11. GATE, #3  12. SOURCE, #3  13. GATE, #2  14. SOURCE, #2  15. GATE, #1  16. SOURCE, #1</p>	<p><b>STYLE 6:</b></p> <p>PIN 1. CATHODE  2. CATHODE  3. CATHODE  4. CATHODE  5. CATHODE  6. CATHODE  7. CATHODE  8. CATHODE  9. ANODE  10. ANODE  11. ANODE  12. ANODE  13. ANODE  14. ANODE  15. ANODE  16. ANODE</p>	<p><b>STYLE 7:</b></p> <p>PIN 1. SOURCE N-CH  2. COMMON DRAIN (OUTPUT)  3. COMMON DRAIN (OUTPUT)  4. GATE P-CH  5. COMMON DRAIN (OUTPUT)  6. COMMON DRAIN (OUTPUT)  7. COMMON DRAIN (OUTPUT)  8. SOURCE P-CH  9. SOURCE P-CH  10. COMMON DRAIN (OUTPUT)  11. COMMON DRAIN (OUTPUT)  12. COMMON DRAIN (OUTPUT)  13. GATE N-CH  14. COMMON DRAIN (OUTPUT)  15. COMMON DRAIN (OUTPUT)  16. SOURCE N-CH</p>	

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<b>DESCRIPTION:</b>	SOIC-16 9.90X3.90X1.50 1.27P	<b>PAGE 2 OF 2</b>

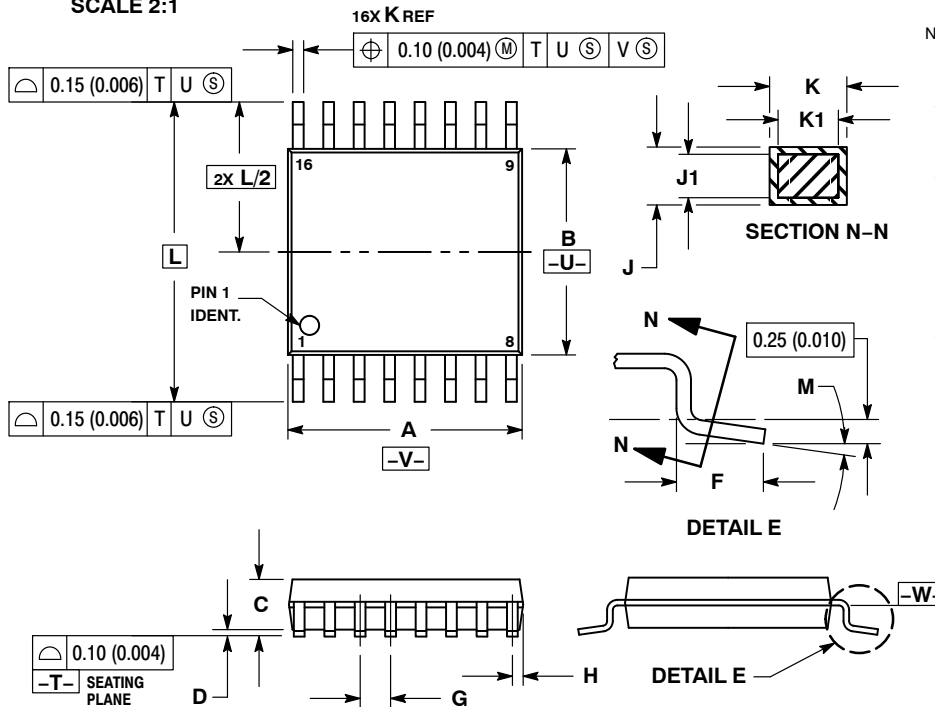
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TSSOP-16 WB  
CASE 948F  
ISSUE B

DATE 19 OCT 2006

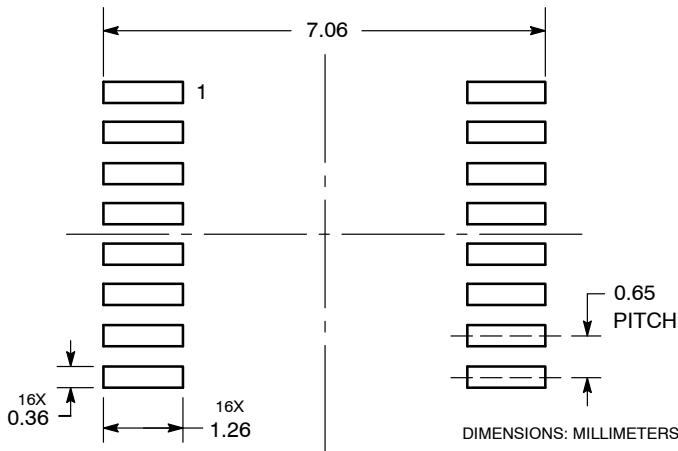


NOTES:

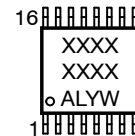
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

RECOMMENDED  
SOLDERING FOOTPRINT\*



GENERIC  
MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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