

General Announcement

Title: Pb (lead) Free Lead Finish/Plating Conversion

First Anticipated Date Code Conversion: June 1st, 2003

Last Anticipated Date Code Conversion: March 1st, 2004

Description and Purpose: Pb Free Lead Finish Conversion

This is a General Announcement that ON Semiconductor is converting the External Lead Finish/Plating to a Pb (lead) Free Finish/Plating process. ON Semiconductor recognizes the increasing demand for environmentally friendly products. ON Semiconductor will convert the existing SnPb (Tin Lead) lead finish/plating to a Pb Free solution on a package by package basis. This conversion will take place from June 2003 to March 2004, with approximately four conversion phases. This General Announcement will be followed by Process Change Notifications (PCNs) prior to each package being converted. The PCNs will include the complete list of affected devices.

Plating Compositions – The Pb containing lead finish composition and the new Pb Free lead finish compositions will be noted on the PCN for each package type.

Moisture Sensitivity Level (MSL) – Surface Mount Packages are qualified to 260 degrees C, which is a higher temperature profile than the JEDEC standard J-STD-020B. The majority of the MSL ratings will remain unchanged from the current MSL 1 classification. The MSL rating will be noted on the PCN for each package type. If there is a change in the MSL rating of a package, appropriate packing precautions will be taken before any product is shipped by ON Semiconductor.

Compatibility – ON Semiconductor has tested the forward and backward compatibility of both Through Hole Devices (THD) and Surface Mount Devices (SMD). Forward compatibility refers to the ability of current Pb containing lead finishes to be used with Pb Free solder pastes. Backward compatibility refers to the ability of the new Pb Free lead finishes to be used with Pb containing solder pastes. All of ON Semiconductor's Pb containing lead finishes are forward compatible. A change in the MSL rating @ 260 degrees C must be taken into account for handling product outside the packing. Virtually all of ON Semiconductor's new Pb Free lead finishes are Backward compatible with a few exceptions, for example, BGA/Bumped processes. Special notes will be placed on the PCN if a device is not backward compatible.

Device Identification – Part numbers and marking will remain unchanged, however, the bar code label on the reel, tube or rail, and the intermediate boxes will have the statement "PB FREE PLTG" printed on those labels. Pb Free product will also be traceable to the Date Code of the product.

Conversion Date and Date Codes – The noted Anticipated Conversion Date refers to the date the Production Process will be converted to the Pb Free Process. Products with Date Codes from that date forward will have the Pb Free lead Finish. Actual receipt of Pb Free Products is based upon the depletion of inventories.

Phase 1			
Anticipated Conversion Date: June 1st 2003			
Samples and Reliability, Available Now			
ChipFET	Micro 8	PowerMite	SC-59
SC-70	SC-74	SC-75	SC-82AB
SC-88	SC-88A	SMA	SMB
SMC	SOD-123	SOD-323	SOT-23-L
SOT-23LC ¹	TSOP-5 ²	TSOP-6 ³	US8
PLCC	LQFP 32	SO-8	TSSOP 8
Notes:			
1. SOT-23LC denotes only Large Collector (drain) parts in SOT-23. Remainder of SOT-23 will convert in Phase 3.			
2. TSOP5 is for Analog and Logic devices only at this time.			
3. TSOP6 is for Discrete and TMOS devices only at this time.			
The Final Process Change Notification for each package will contain the complete list of affected devices.			

Phase 2			
Anticipated Conversion Date: Sept. 1st 2003			
Samples and Reliability Data no later than June 1st, 2003			
Case 77	CDIP	D2PAK	D2PAK 3Ld
D2PAK 5Ld	DPAK	QFN	SC-70-5
SC-88 Epoxy	SON	SOT-223	SOT-23 5 Pin
SOT-23 Epoxy			
Notes:			
The Final Process Change Notification for each package will contain the complete list of affected devices.			

Phase 3			
Anticipated Conversion Date: Dec. 1st 2003			
Samples and Reliability Data no later than August 1st, 2003			
D2PAK 7Ld	Micro 10	PQFN	QSOP
SOIC	SOIC Wide	SO-16	SOT-143
SOT-23	TSOP6 ¹	SOT-23 5 Pin	SOT-23 6 Pin
TSSOP 24/28/48	LQFP 48/52/64		
Notes:			
1. TSOP6 is for Analog and Logic devices.			
The Final Process Change Notification for each package will contain the complete list of affected devices.			

Phase 4			
Anticipated Conversion Date: March 1st 2004			
Samples and Reliability Data no later than November 1st, 2003			
BGA	FCBGA	SOT-89	SSOP
SSOP Wide	PDIP	TO-247	TO-220
TO-3	TO-264	TO-92	Axial Lead Button
Surge Special	TO-218	Bumped Die/FlipChip	
TO-220 FullPAK MicroBump			
Notes:			
The Final Process Change Notification for each package will contain the complete list of affected devices.			

Qualification Plan:

The qualification requirements for Pb-Free external lead finish differ for surface-mount device (SMD) or through-hole devices (THD).

For the THDs the primary qualification requirement is to demonstrate forward compatibility with new Pb-Free solder pastes (based on SnCuAg), and backward compatibility with existing solder pastes (based on SnPb). The tests to be performed typically include:

Solderability with SnCuAg solder
Solderability with SnPb solder
Resistance to Solder Heat

For the SMDs reclassification of the moisture sensitivity level (MSL) at a peak reflow temperature of 260 deg. C is required in addition to solderability validation. The MSL reclassification is performed on the largest die size that is used in the package. The tests to be performed typically include:

Preconditioned Highly Accelerated Stress Testing (PC-HAST)
Preconditioned Autoclave (PC-AC)
Preconditioned Temperature Cycling (PC-TC)
(Preconditioning is performed at the target MSL for 260 deg. C)

Solderability with SnCuAg solder
Solderability with SnPb solder
Resistance to Solder Heat (RSH – Solder Immersion)

Points of Contact:

Your Local ON Semiconductor Sales Representative

ON Semiconductor Technical Information Center 1-800-282-9855 (US & Canada) or <http://www.onsemi.com/tech-support>

<http://www.onsemi.com/pb-free>