Ħ

TOP VIEW

□ 0.20 C

8X b-

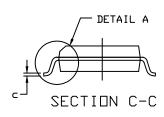
⊕ 0.12 **(** C A − B D

SOIC8 WB CASE 751EW ISSUE A

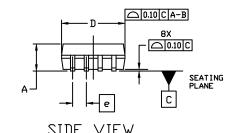
DATE 31 MAY 2019

NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- DIMENSION 6 DOES NOT INCLUDE DAMBAR PROTRUSION.
 ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
- 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH,
 PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS,
 OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE.
 DIMENSIONS D AND E ARE DETERMINED AT DATUM H.
- 5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
- 6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
- 7. NO JEDEC STANDARD AT TIME OF SETUP.



DIM MIN. NDM. MAX. A 2.35 2.50 2.65 A1 0.10 0.20 0.30 b 0.31 0.41 0.51 c 0.20 0.27 0.33 D 5.65 5.85 6.05 E 10.11 10.31 10.51 E1 7.40 7.50 7.60 e 1.27 BSC L 0.40 0.58 0.75 L2 0.25 BSC θ 0° 8°		MILLIMETERS		
A1 0.10 0.20 0.30 b 0.31 0.41 0.51 c 0.20 0.27 0.33 D 5.65 5.85 6.05 E 10.11 10.31 10.51 E1 7.40 7.50 7.60 e 1.27 BSC L 0.40 0.58 0.75 L2 0.25 BSC	DIM	MIN.	N□M.	MAX.
b 0.31 0.41 0.51 c 0.20 0.27 0.33 D 5.65 5.85 6.05 E 10.11 10.31 10.51 E1 7.40 7.50 7.60 e 1.27 BSC L 0.40 0.58 0.75 L2 0.25 BSC	Α	2.35	2.50	2.65
C 0.20 0.27 0.33 D 5.65 5.85 6.05 E 10.11 10.31 10.51 E1 7.40 7.50 7.60 e 1.27 BSC L 0.40 0.58 0.75 L2 0.25 BSC	A1	0.10	0.20	0.30
D 5.65 5.85 6.05 E 10.11 10.31 10.51 E1 7.40 7.50 7.60 e 1.27 BSC L 0.40 0.58 0.75 L2 0.25 BSC	b	0.31	0.41	0.51
E 10.11 10.31 10.51 E1 7.40 7.50 7.60 e 1.27 BSC L 0.40 0.58 0.75 L2 0.25 BSC	c	0.20	0.27	0.33
E1 7.40 7.50 7.60 e 1.27 BSC L 0.40 0.58 0.75 L2 0.25 BSC	D	5.65	5.85	6.05
e 1.27 BSC L 0.40 0.58 0.75 L2 0.25 BSC	Ε	10.11	10.31	10.51
L 0.40 0.58 0.75 L2 0.25 BSC	E1	7.40	7.50	7.60
L2 0.25 BSC	e	1.27 BSC		
	L	0.40	0.58	0.75
θ 0° 8°	L2	0.25 BSC		
	θ	0*		8*

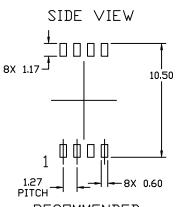


A NOTE 5

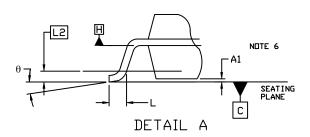
B NOTE 5

△ 0.10 C

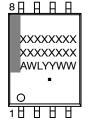
5







GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code A = Assembly Location

WL = Wafer Lot
YY = Year
WW = Work Week
Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " •", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	SOIC8 WB		PAGE 1 OF 1	

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