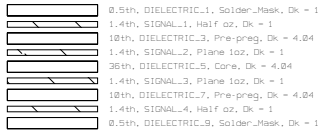
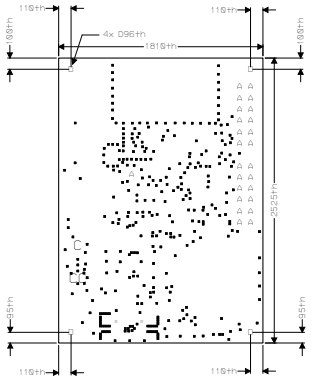
Layer Stackup
Design: RSL15 EVB V1.1
Board thickness: 62





NOTES:

1. Board material, Isola 370HR or equivalent, RoHS Compliant with nominal thickness of 0.062 INCH, 1/2 OZ. base copper on outer layers (SIGNAL_1 & SIGNAL_4), 1 OZ. copper on inner layers (SIGNAL_2, SIGNAL_3).
2. Order of layers is SIGNAL_1, SIGNAL_2, SIGNAL_3, SIGNAL_4
3. All dimension +/- 5 MIL unless specified otherwise.
4. L.D.I. mask on both sides. Mask must be between all lands.
5. Silkscreen to be white ink on both sides of the board. Soldermask color is light green. No ink to be on surface mount land pads. Vendor marking on bottom side.
6. Board to use ENIG (Electroless Nickel Immersion Gold) finish.
7. Boards to be 100% tested to Gerber extracted netlist or using ipc356 netlist.
8. Controlled impedance board - layer SIGNAL_1
   16.5 mil traces on SIGNAL_1 layer shall be 50 ohms +/- 10%
   11 mil traces on SIGNAL_4 layer shall be 90 ohms differential +/- 10%
9. Panel should include at least 2 fiducials.
10. Board to be manufactured to IPC-6012 Class 2

Through Holes

Symbol	Diameter	Tolerance	Plated	Punched	HoleName	Quantity
✥	Ø.0080	+\- Ø.003	Yes	No	Rnd 8	342
A	Ø.0400	+\- Ø.003	Yes	No	Rnd 40	25
B	Ø.0256	+\- Ø.004	No	No	Rnd Ø.65mm Non-Plated	2
C	Ø.0394	+\- Ø.004	No	No	Rnd 1 Non-Plated	3
D	Ø.0960	+/- Ø.0030	No	No	Rnd 96 +/-Tol 3 Non-Plated	4

REVISION HISTORY	DATE
V1.0 Initial Design	Dec. 10, 2020
V1.1 Updated RF section	Feb. 15, 2021

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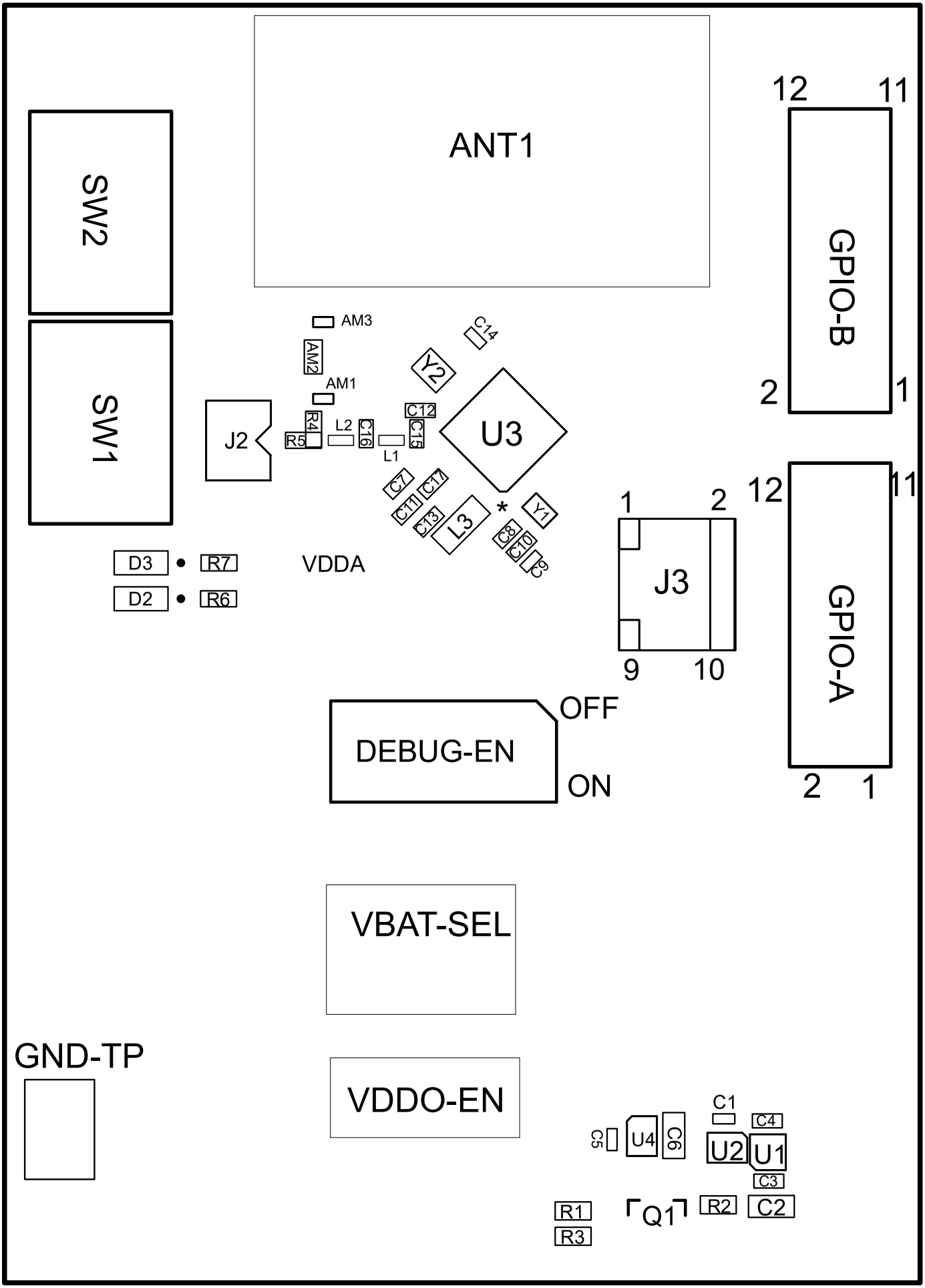
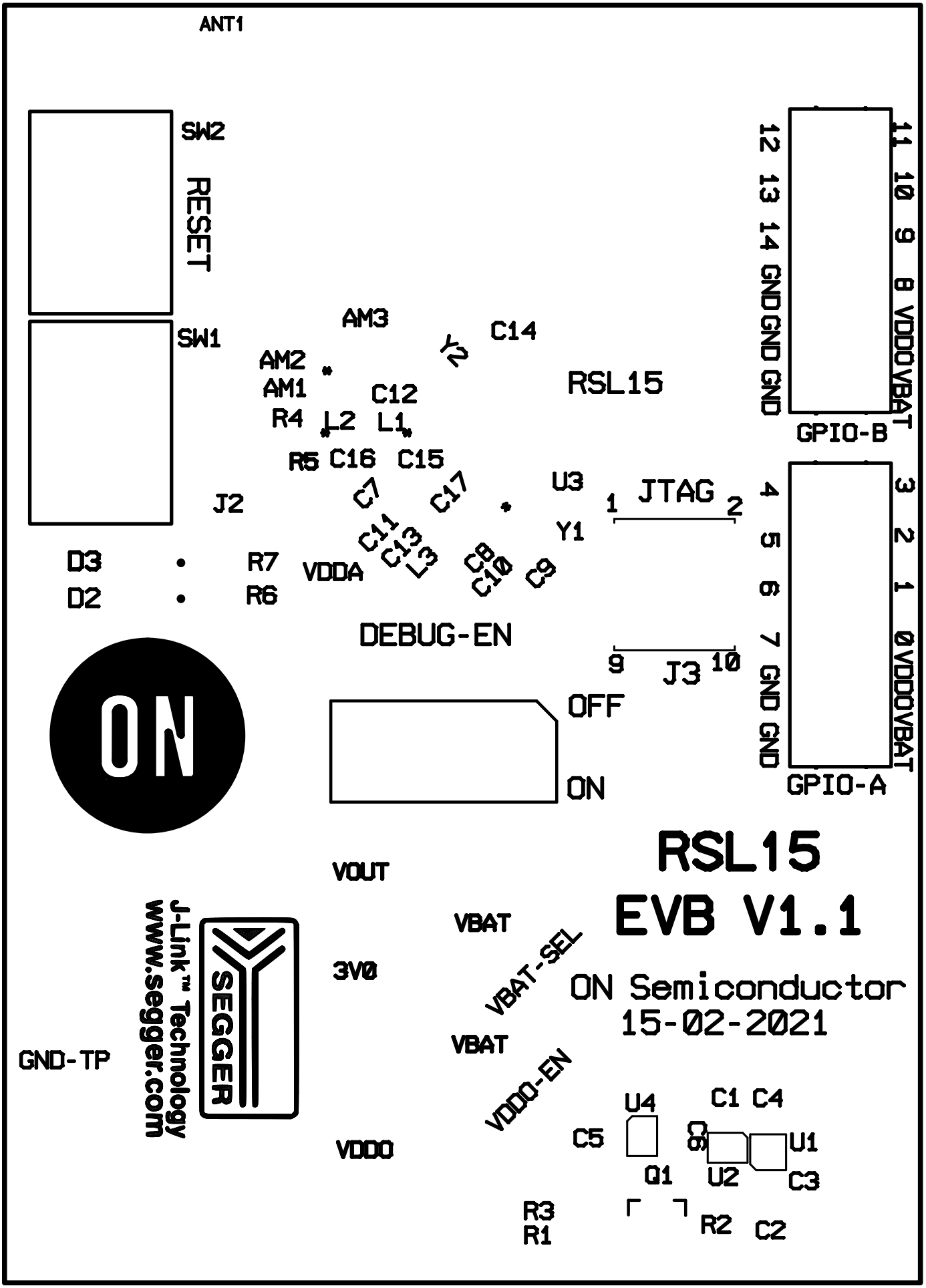
Waterloo, Ont.
Canada, N2V 1K8

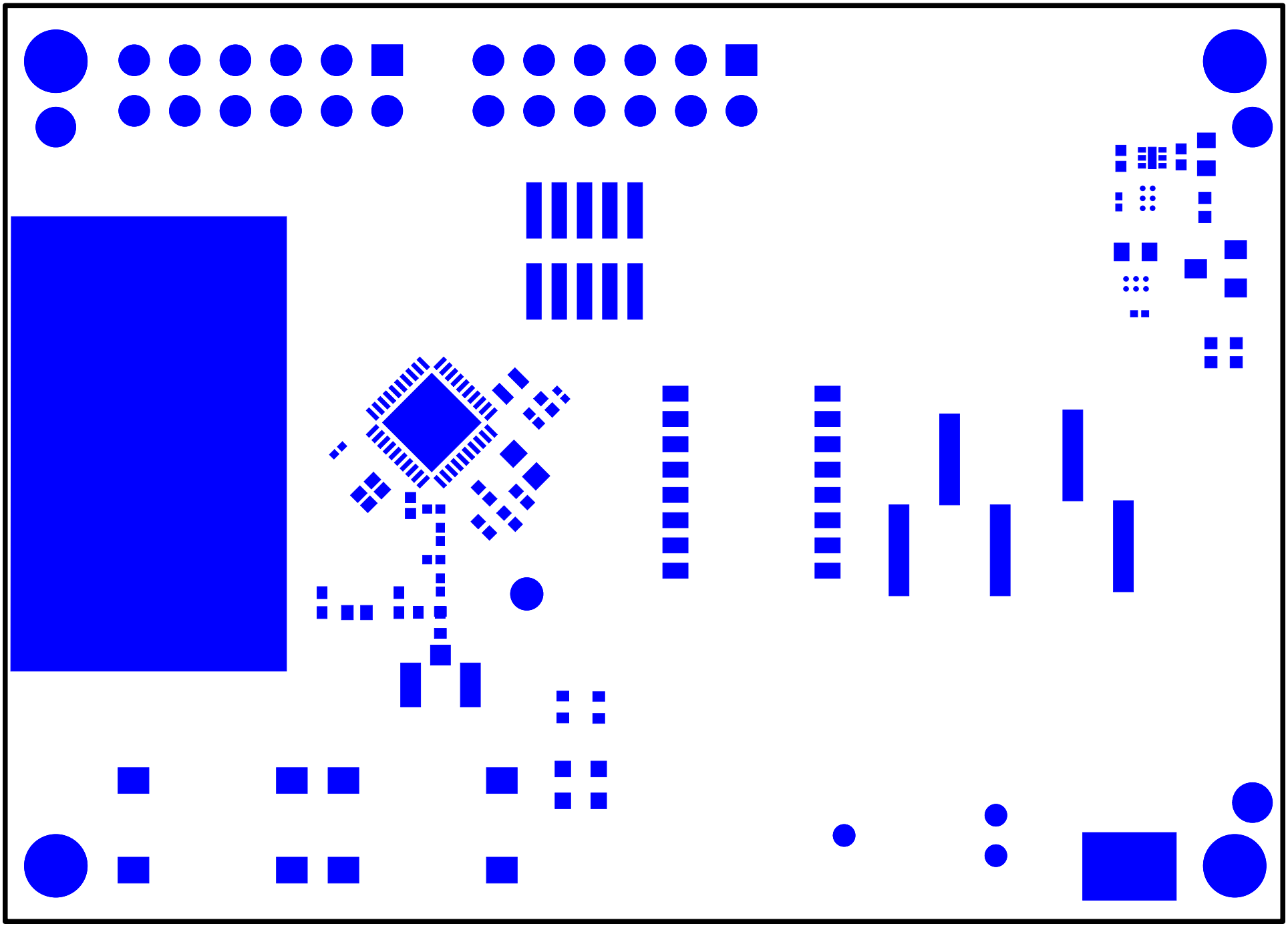
TITLE
RSL15 EVB

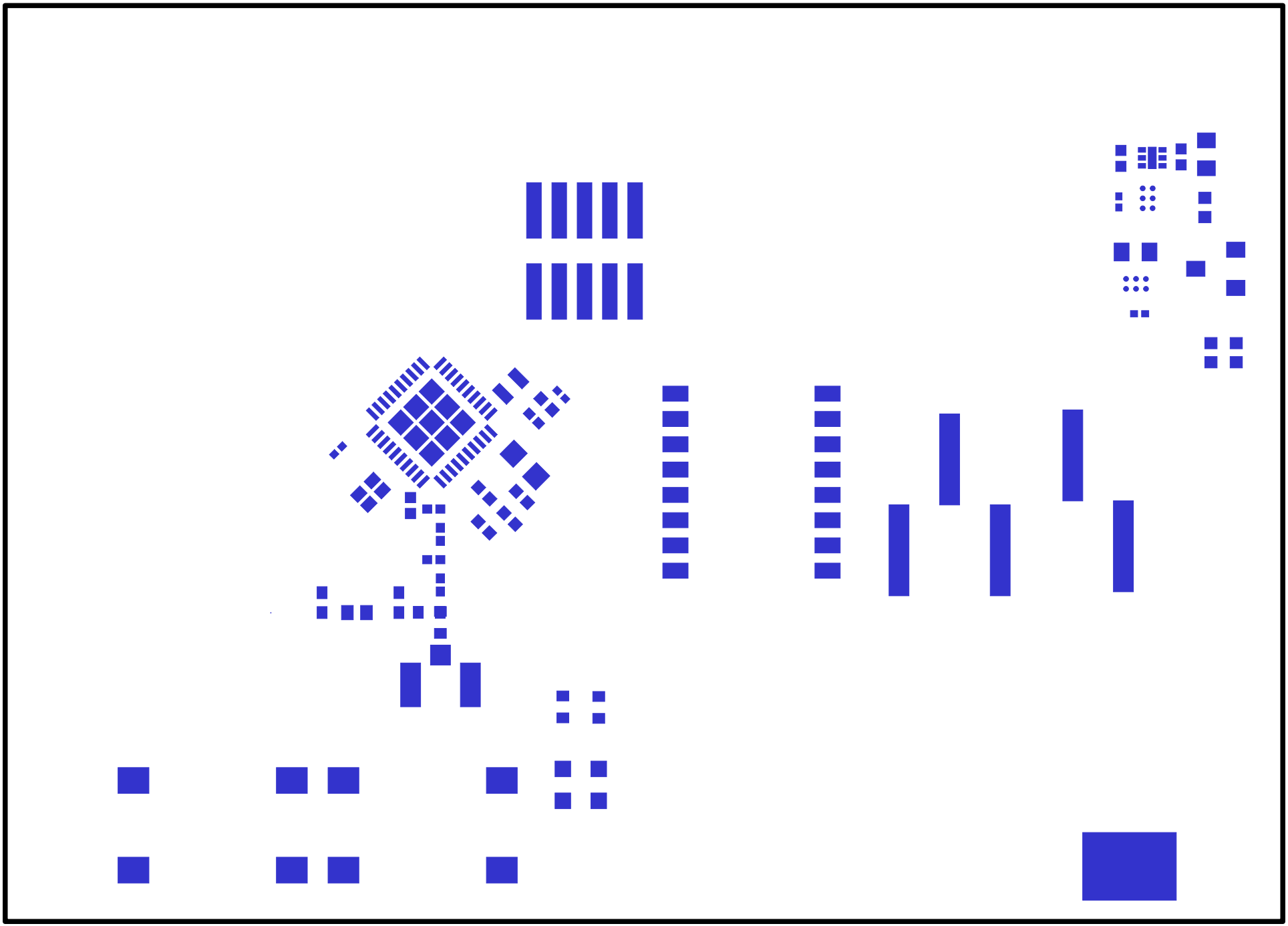
SIZE	NUMBER	REV
B		V1.1

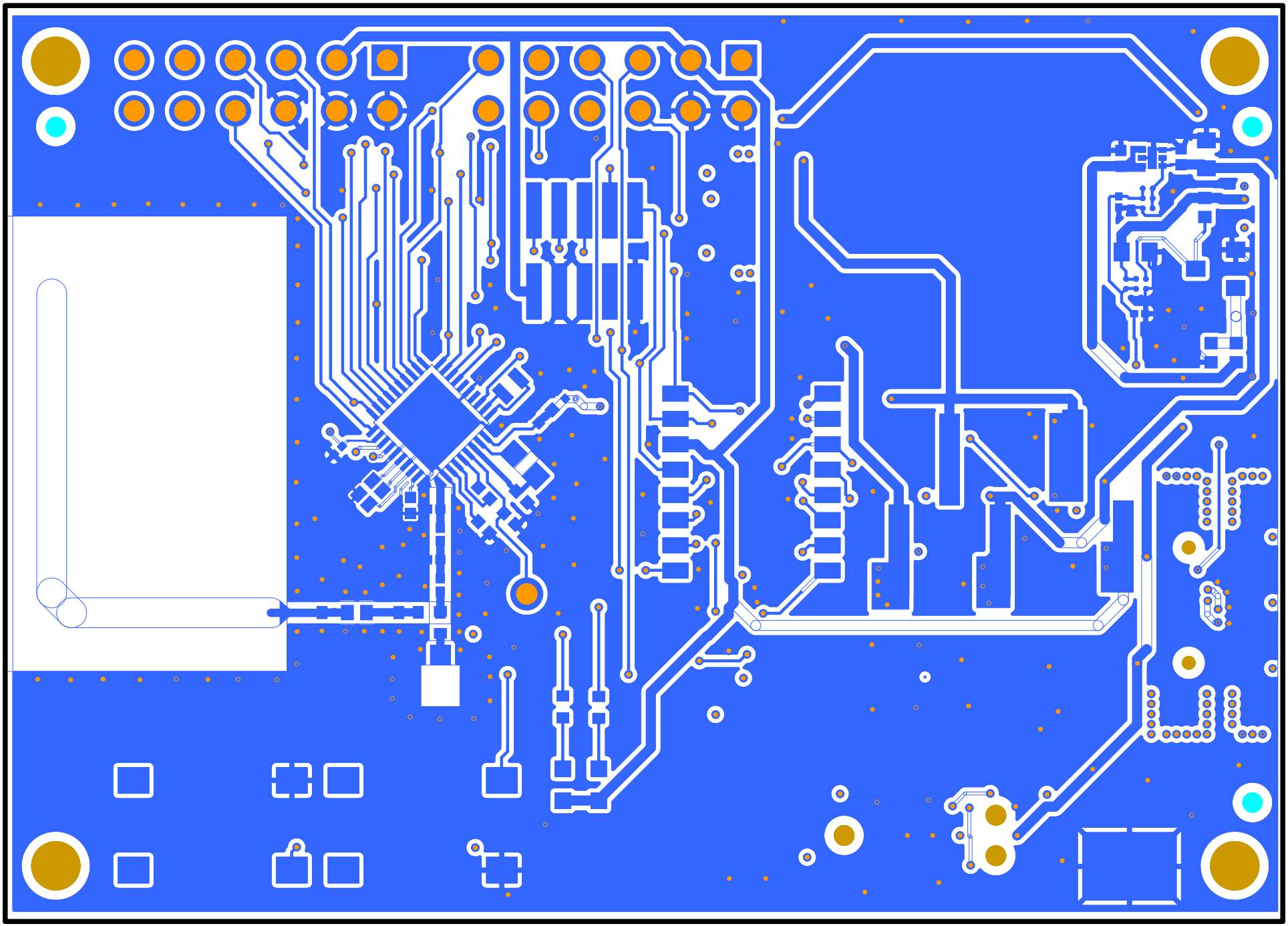
Drawn By	M.C.	Fabrication Drawing	DATE	15-02-21	SHEET	1 of 1

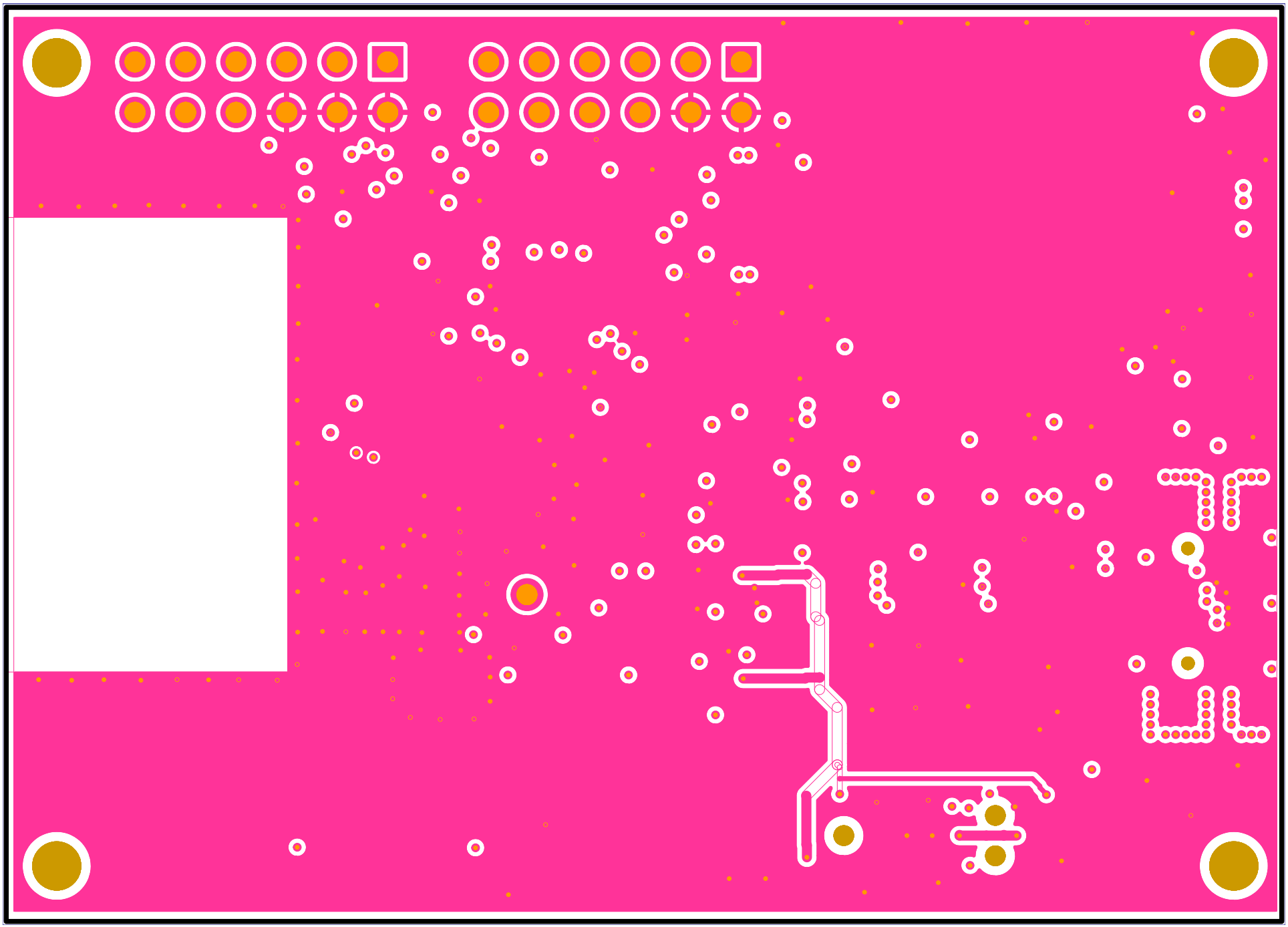

ANT1
SW2
SW1
GPIO-B
12
11
2
1
AM3
AM2
AM1
C14
Y2
C12
C15
C16
L2
L1
R4
R5
J2
U3
C7
C17
C11
C13
L3
C8
C10
C9
Y1
*
D3
R7
D2
R6
VDDA
1
2
J3
9
10
GPIO-A
12
11
2
1
OFF
DEBUG-EN
ON
VBAT-SEL
GND-TP
VDDO-EN
C1
C4
C5
U4
C6
U2
U1
C3
R1
R3
Q1
R2
C2

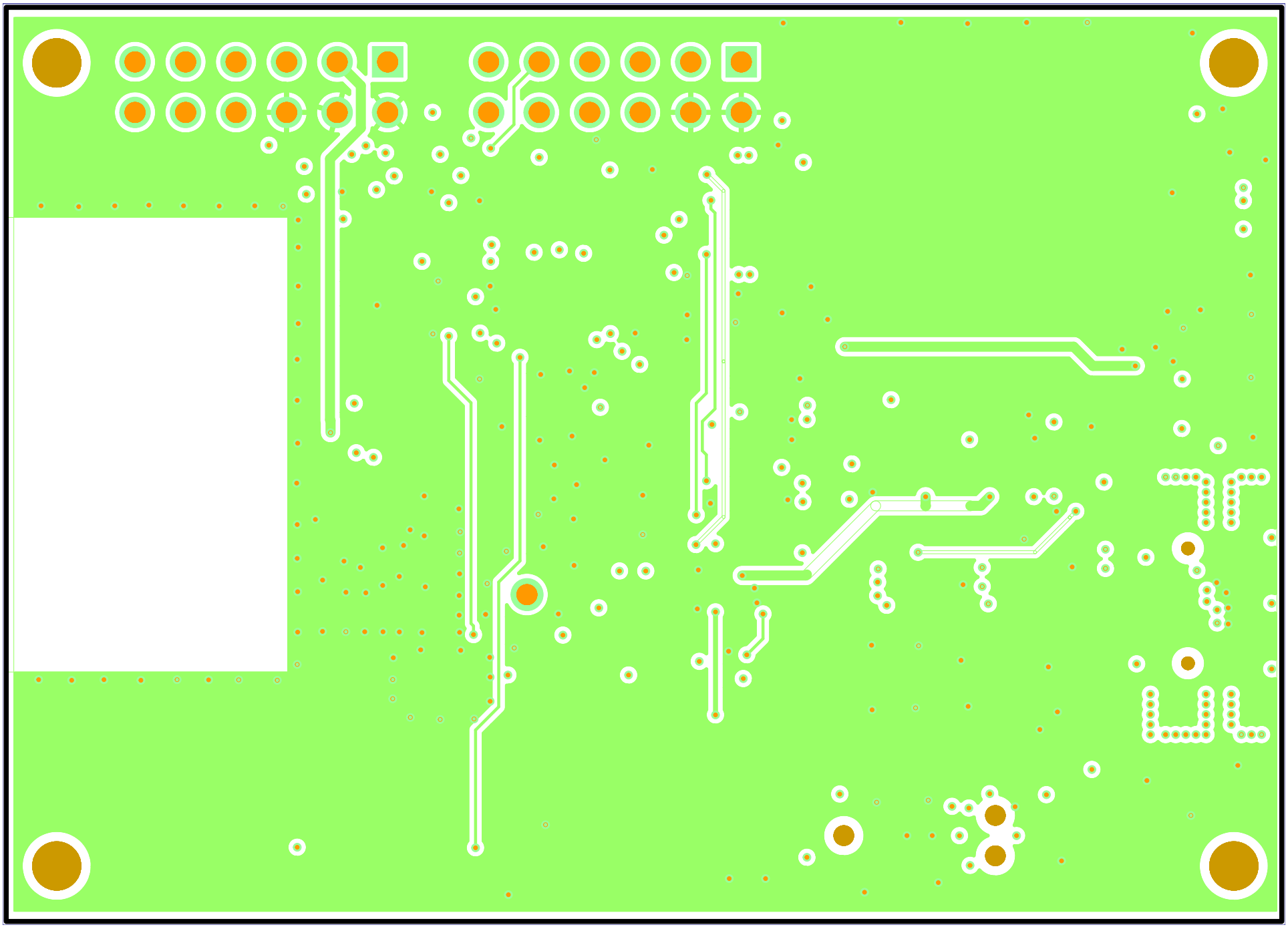

ANT1
SW2
RESET
SW1
AM3
AM2
AM1
R4
L2
L1
C12
C14
Y2
RSL15
R5
C16
C15
C7
C17
U3
J2
C11
C13
L3
C8
C10
C9
Y1
JTAG
1
2
D3
D2
R7
R6
VDDA
DEBUG-EN
9
J3
10
OFF
ON
VOUT
VBAT
3V0
VBAT-SEL
VBAT
VDDO-EN
VDDO
GND-TP
J-Link™ Technology
www.segger.com
SEGGER
RSL15
EVB V1.1
ON Semiconductor
15-02-2021
U4
C1
C4
C5
C6
U1
Q1
U2
C3
R3
R1
R2
C2
11 10 9 8 VDDO VBAT
12 13 14 GND GND GND
GPIO-B
4 5 6 7 GND GND
3 2 1 0 VDDO VBAT
GPIO-A

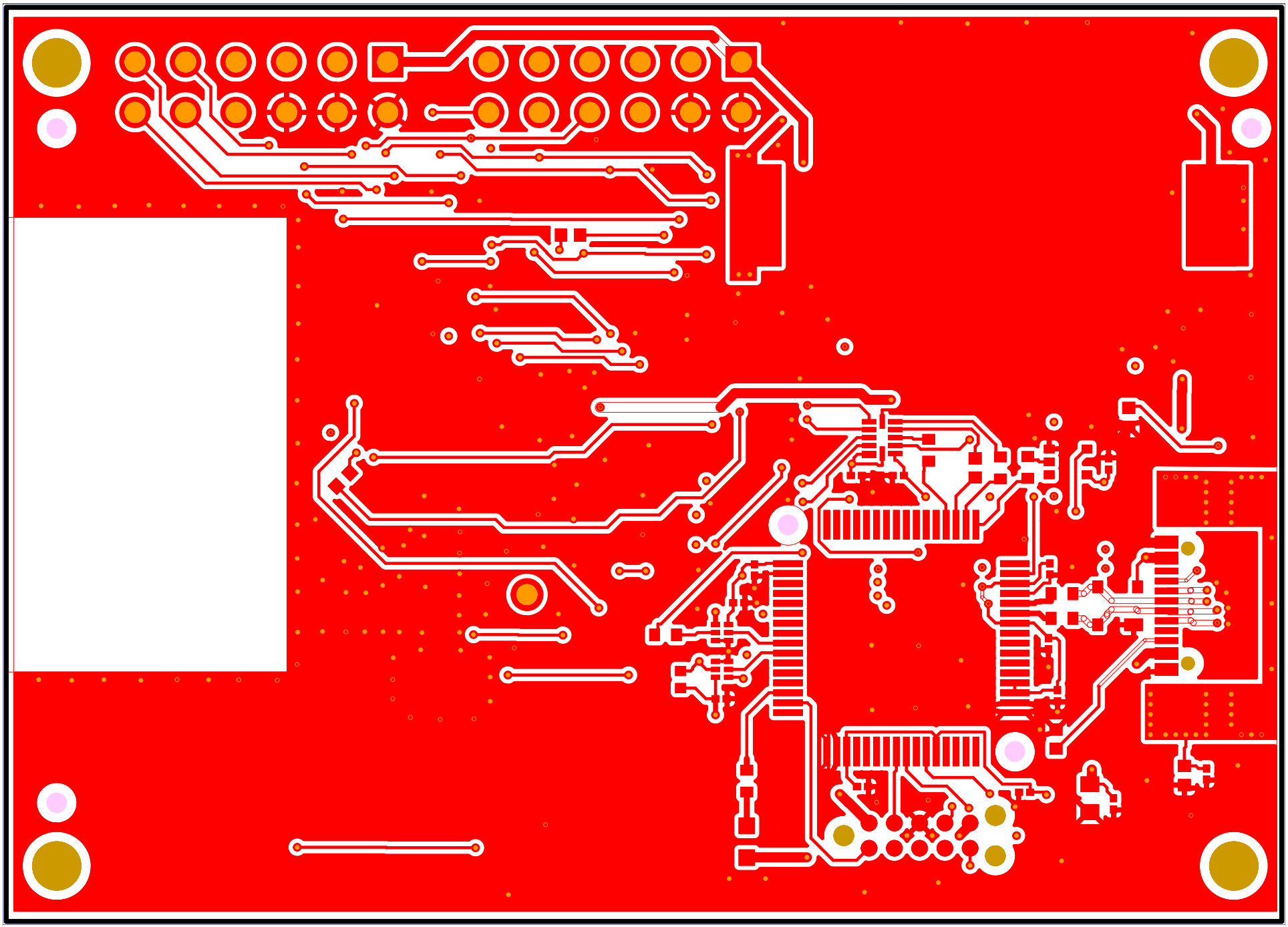


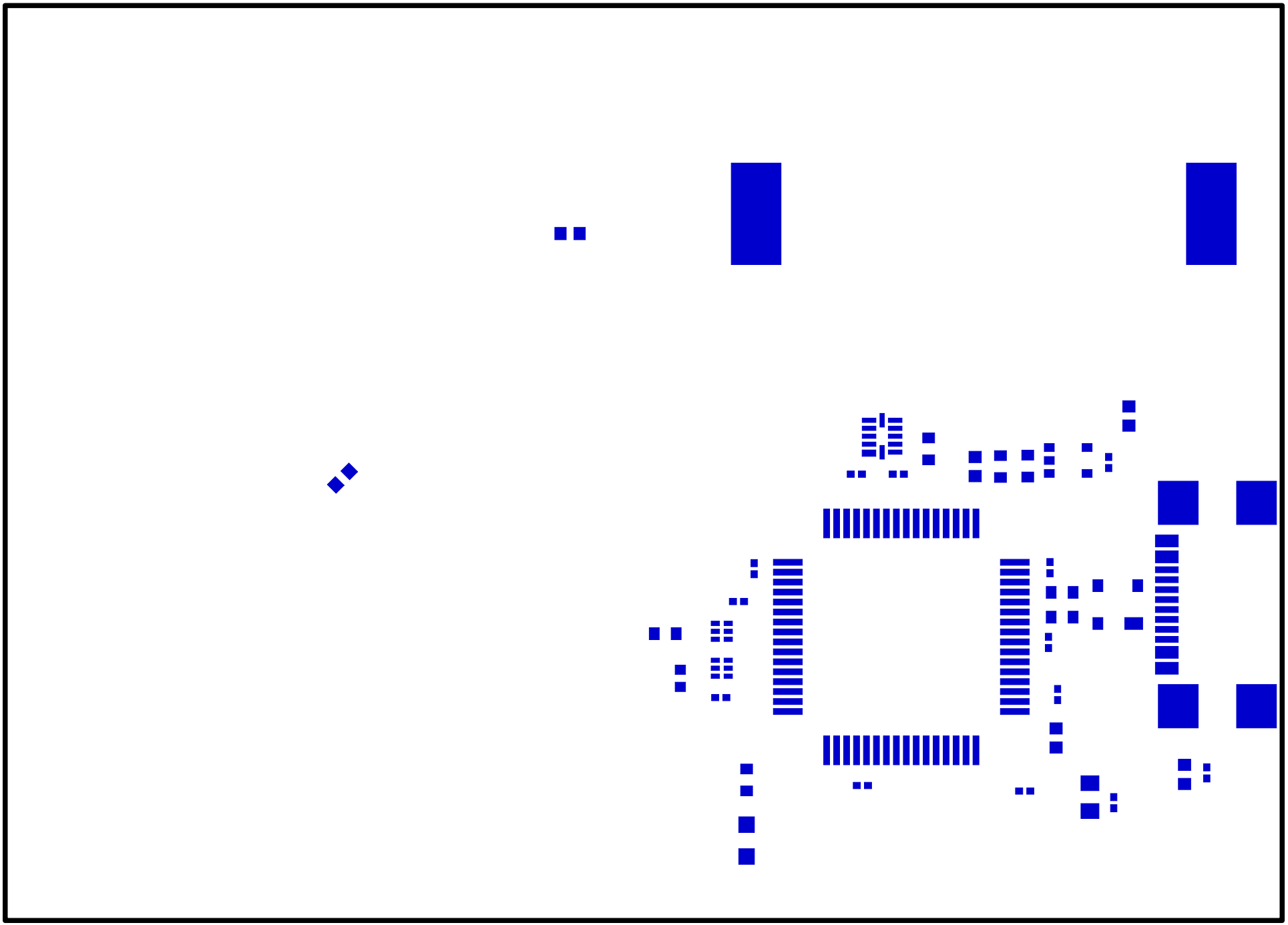


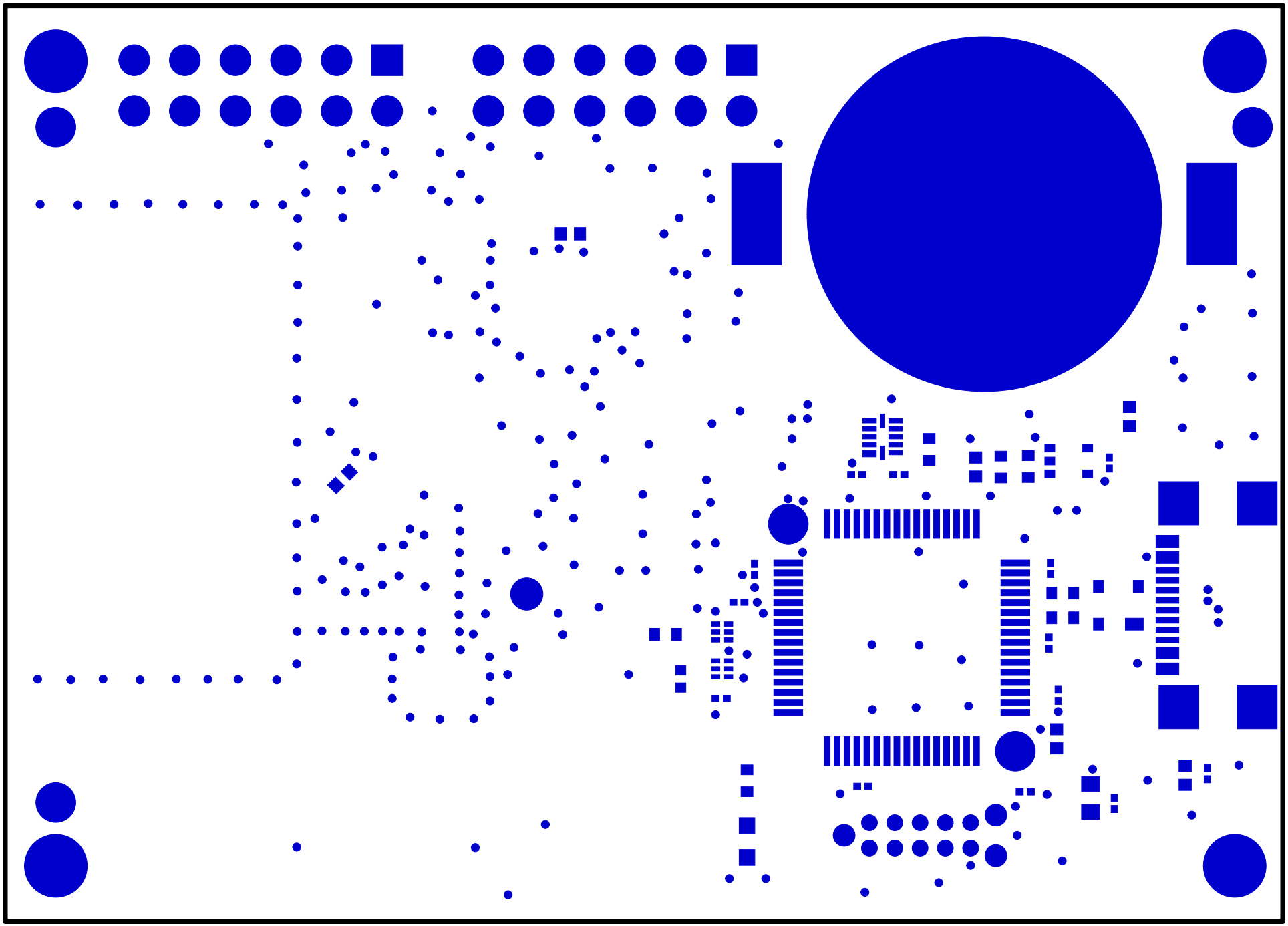


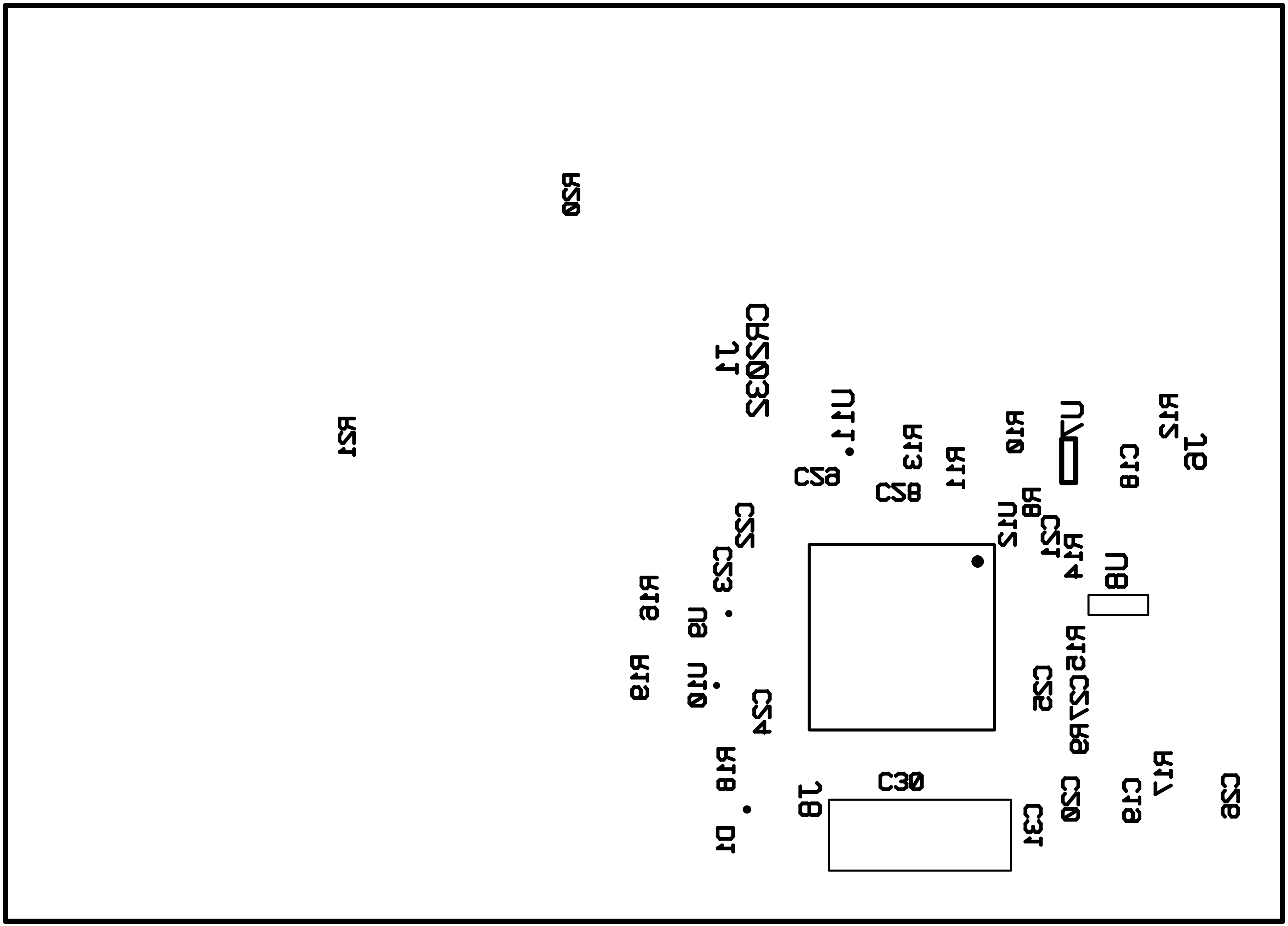


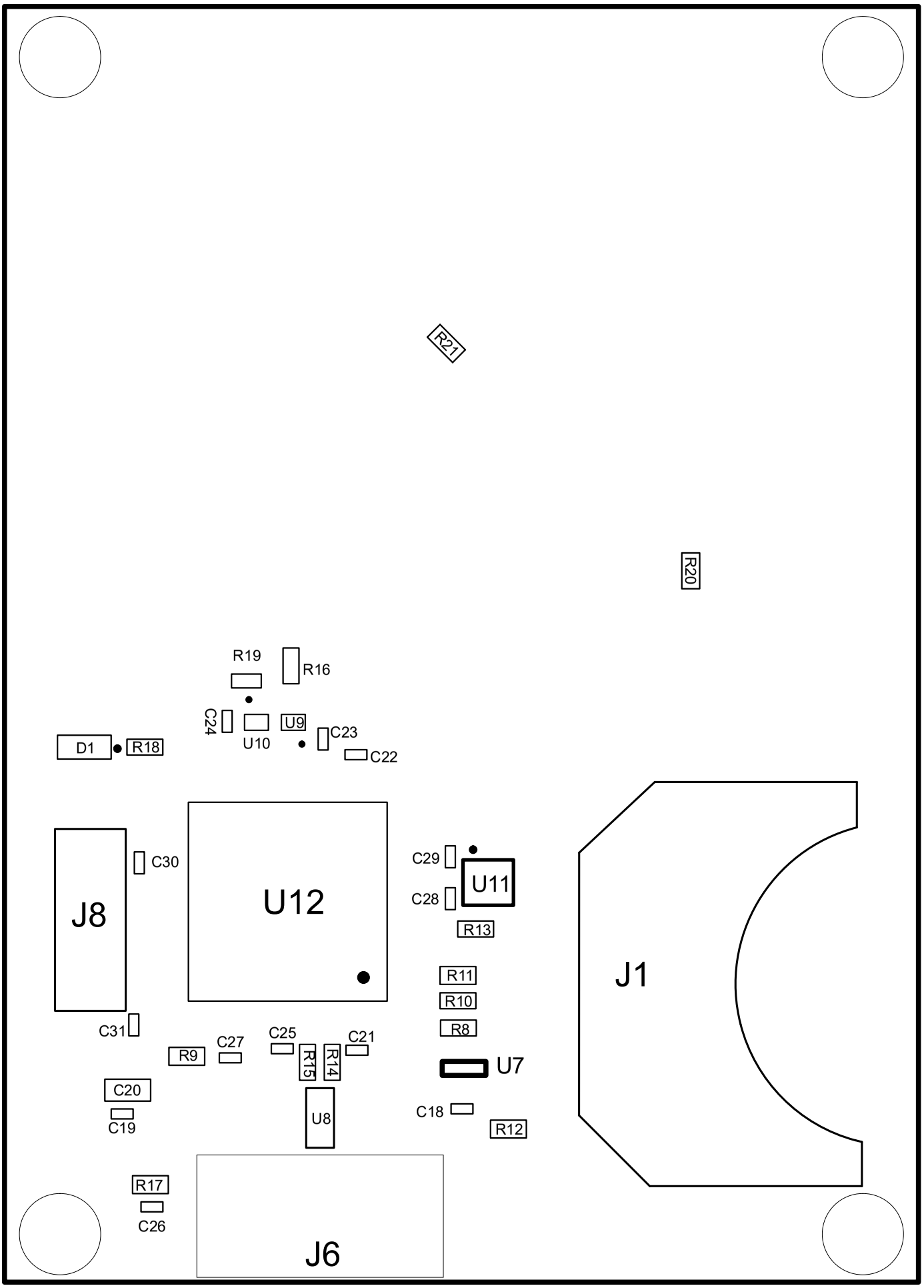









R20
R21
CR2033
1.1
U11
R13
R11
R10
U7
R12
C16
C18
C29
C28
R8
U12
C21
R14
U8
C22
C23
R16
U9
R19
U10
R15
C27
R9
C25
C24
R18
C30
J1
C20
C19
R17
C26
C31
D1


R21
R20
R19
R16
C24
U9
U10
C23
C22
D1
R18
J8
C30
U12
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U11
C28
R13
J1
R11
R10
R8
C31
R9
C27
C25
R15
R14
C21
U7
C20
C19
U8
C18
R12
R17
C26
J6