

# NPN High-Power Transistors

## TIP33C

Designed for general-purpose power amplifier and switching applications.

### Features

- ESD Ratings: Machine Model, C; > 400 V  
Human Body Model, 3B; > 8000 V
- Epoxy Meets UL 94 V-0 @ 0.125 in
- These Devices is Pb-Free\*

### MAXIMUM RATINGS

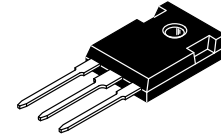
Rating	Symbol	Value	Unit
Collector – Emitter Voltage	$V_{CEO}$	60	Vdc
Collector – Base Voltage	$V_{CBO}$	60	Vdc
Emitter – Base Voltage	$V_{EBO}$	5.0	Vdc
Collector Current – Continuous – Peak (Note 1)	$I_C$	10 15	Adc Apk
Base Current – Continuous	$I_B$	3.0	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	80 0.64	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.56	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	35.7	$^\circ\text{C}/\text{W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

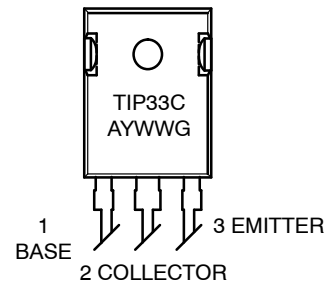
1. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .



TO-247  
CASE 340L  
STYLE 3

## 10 AMPERE NPN SILICON POWER TRANSISTORS 60 & 100 VOLT, 80 WATTS

### MARKING DIAGRAM



TIP33C = Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
TIP33CG	TO-247 (Pb-Free)	30 Units / Rail

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# TIP33C

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (Note 2) (I <sub>C</sub> = 30 mA, I <sub>B</sub> = 0)	V <sub>CEO(sus)</sub>	60	– –	Vdc
Collector–Emitter Cutoff Current (V <sub>CE</sub> = 30 V, I <sub>B</sub> = 0) (V <sub>CE</sub> = 60 V, I <sub>B</sub> = 0)	I <sub>CEO</sub>	–	0.7	mA
Collector–Emitter Cutoff Current (V <sub>CE</sub> = Rated V <sub>CEO</sub> , V <sub>EB</sub> = 0)	I <sub>CES</sub>	–	0.4	mA
Emitter–Base Cutoff Current (V <sub>EB</sub> = 5.0 V, I <sub>C</sub> = 0)	I <sub>EBO</sub>	–	1.0	mA

### ON CHARACTERISTICS (Note 2)

DC Current Gain (I <sub>C</sub> = 1.0 A, V <sub>CE</sub> = 4.0 V) (I <sub>C</sub> = 3.0 A, V <sub>CE</sub> = 4.0 V)	h <sub>FE</sub>	40 20	– 100	–
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 3.0 A, I <sub>B</sub> = 0.3 A) (I <sub>C</sub> = 10 A, I <sub>B</sub> = 2.5 A)	V <sub>CE(sat)</sub>	– –	1.0 4.0	Vdc
Base–Emitter On Voltage (I <sub>C</sub> = 3.0 A, V <sub>CE</sub> = 4.0 V) (I <sub>C</sub> = 10 A, V <sub>CE</sub> = 4.0 V)	V <sub>BE(on)</sub>	– –	1.6 3.0	Vdc

### DYNAMIC CHARACTERISTICS

Small–Signal Current Gain (I <sub>C</sub> = 0.5 A, V <sub>CE</sub> = 10 V, f = 1.0 kHz)	h <sub>fe</sub>	20	–	–
Current–Gain — Bandwidth Product (I <sub>C</sub> = 0.5 A, V <sub>CE</sub> = 10 V, f = 1.0 MHz)	f <sub>T</sub>	3.0	–	MHz

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

# TIP33C

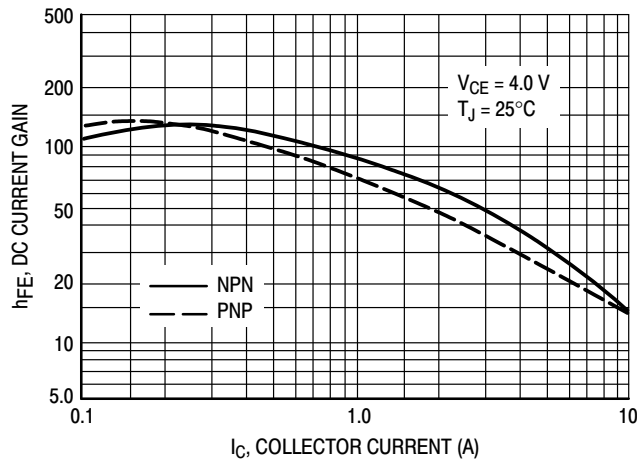


Figure 1. DC Current Gain

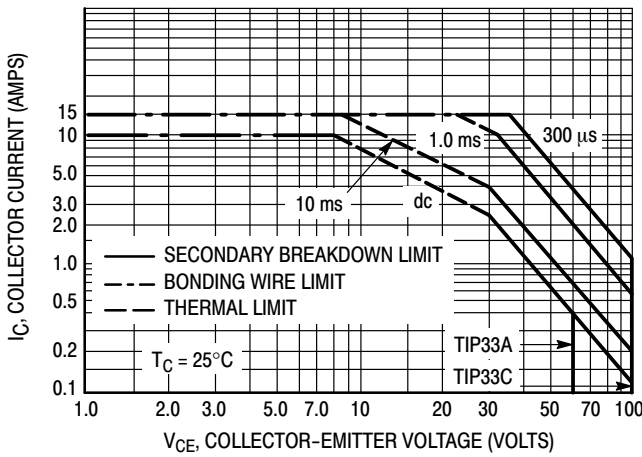


Figure 2. Maximum Rated Forward Bias Safe Operating Area

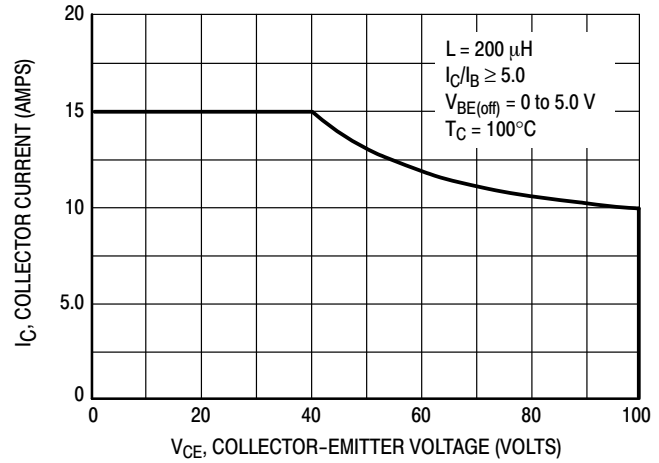


Figure 3. Maximum Rated Forward Bias Safe Operating Area

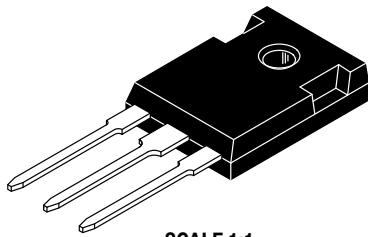
## FORWARD BIAS

The Forward Bias Safe Operating Area represents the voltage and current conditions these devices can withstand during forward bias. The data is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10%, and must be derated thermally for  $T_C > 25^\circ\text{C}$ .

## REVERSE BIAS

The Reverse Bias Safe Operating Area represents the voltage and current conditions these devices can withstand during reverse biased turn-off. This rating is verified under clamped conditions so the device is never subjected to an avalanche mode.

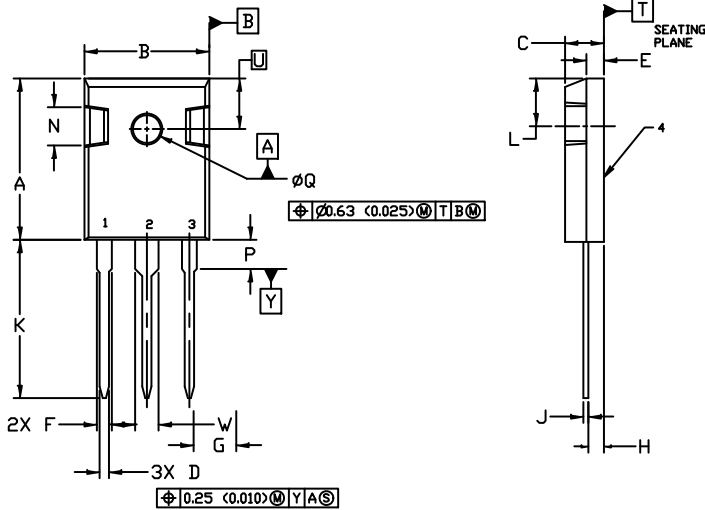
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TO-247  
CASE 340L  
ISSUE G

DATE 06 OCT 2021

SCALE 1:1

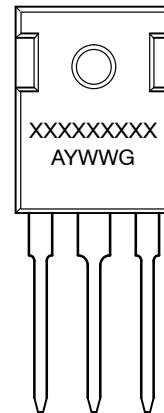


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER

DIM	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	20.32	21.08	0.800	0.830
B	15.75	16.26	0.620	0.640
C	4.70	5.30	0.185	0.209
D	1.00	1.40	0.040	0.055
E	1.90	2.60	0.075	0.102
F	1.65	2.13	0.065	0.084
G	5.45 BSC		0.215 BSC	
H	1.50	2.49	0.059	0.098
J	0.40	0.80	0.016	0.031
K	19.81	20.83	0.780	0.820
L	5.40	6.20	0.212	0.244
N	4.32	5.49	0.170	0.216
P	----	4.50	----	0.177
Q	3.55	3.65	0.140	0.144
U	6.15 BSC		0.242 BSC	
W	2.87	3.12	0.113	0.123

GENERIC  
MARKING DIAGRAM\*



- |  |  |  |  |
|--|--|--|--|
| <p>STYLE 1:<br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p>  | <p>STYLE 2:<br/>PIN 1. ANODE<br/>2. CATHODE (S)<br/>3. ANODE 2<br/>4. CATHODES (S)</p>               | <p>STYLE 3:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 4:<br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> |
| <p>STYLE 5:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p> | <p>STYLE 6:<br/>PIN 1. MAIN TERMINAL 1<br/>2. MAIN TERMINAL 2<br/>3. GATE<br/>4. MAIN TERMINAL 2</p> |  |  |

- XXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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