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SG6859A
Low-Cost, Green-Mode PWM Controller for Flyback Converters

Features

- Green-Mode PWM
- Supports the "Blue Angel" Standard
- Low Startup Current: 9 µA
- Low Operating Current: 3 mA
- 300 mA Driving Capability
- Leading-Edge Blanking
- Constant Output Power Limit
- Universal Input
- Built-in Synchronized Slope Compensation
- Current-Mode Operation
- Cycle-by-cycle Current Limiting
- Under-Voltage Lockout (UVLO)
- Programmable PWM Frequency with Frequency Hopping
- V_{DD} Over-Voltage Protection (Auto Restart)
- Gate Output Voltage Clamped at 17 V
- Low Cost
- Few External Components Required
- Small SOT23-6L Package

Applications

General-purpose switching mode power supplies and flyback power converters, such as:

- Battery chargers for cellular phones, cordless phones, PDAs, digital cameras, and power tools
- Power adapters for ink jet printers, video game consoles, and portable audio players
- Open-frame SMPS for TV/DVD standby and auxiliary supplies, home appliances, and consumer electronics
- Replacements for linear transformers and RCC SMPS
- PC 5 V standby power

Description

This highly integrated PWM controller provides several enhancements designed to meet the low standby-power needs of low-power SMPS. To minimize standby power consumption, the proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency under light-load conditions. This green-mode function enables the power supply to meet even the strictest power conservation requirements.

The BiCMOS fabrication process enables reducing the startup current to 9 µA and the operating current to 3 mA. To further improve power conservation, a large startup resistance can be used. Built-in synchronized slope compensation ensures the stability of peak current mode control. Proprietary internal compensation provides a constant output power limit over a universal AC input range (90 V_{AC} to 264 V_{AC}). Pulse-by-pulse current limiting ensures safe operation during short-circuits.

To protect the external power MOSFET from damage by supply over voltage, the SG6859A's output driver is clamped at 17 V. SG6859A controllers can be used to improve the performance and reduce the production cost of power supplies. The best choice for replacing linear and RCC-mode power adapters, the SG6859A is available in 8-pin DIP and 6-pin SOT23-6L packages.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
SG6859ATZ		SOT23-6L	Tape & Reel
SG6859ATY	-40 to +105°C	SOT23-6L	
SG6859ADZ		DIP-8	Tube
SG6859ADY			

Application Diagram
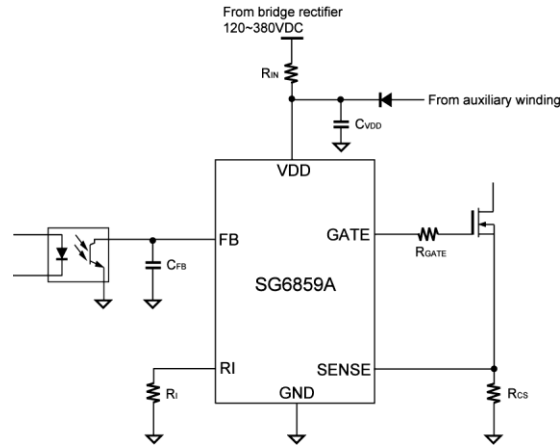
Figure 1.   Typical Application

Internal Block Diagram
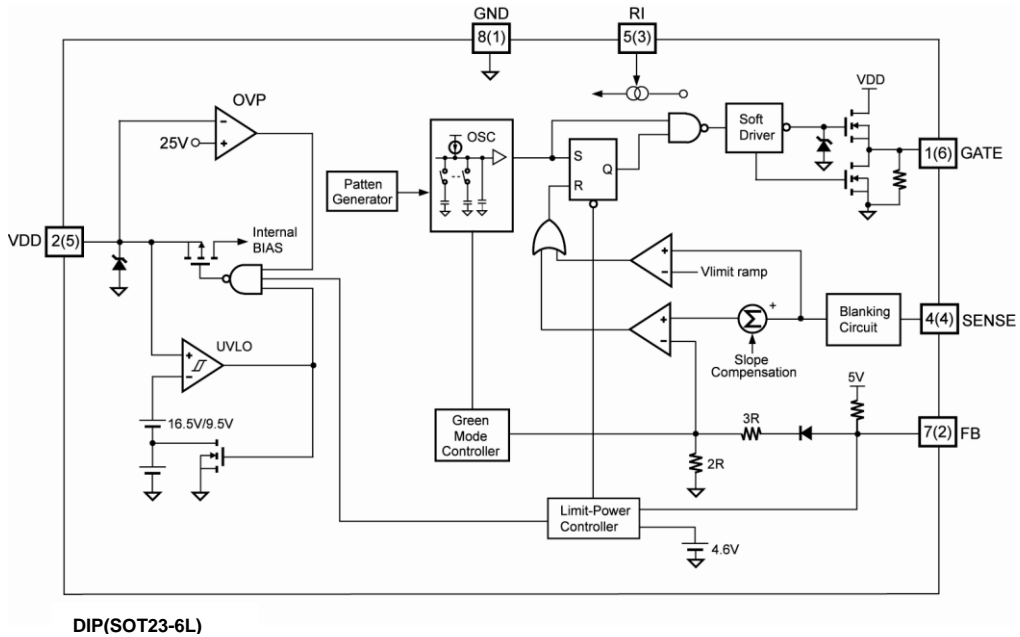
Figure 2.   Functional Block Diagram

Marking Information

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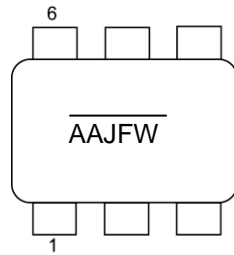
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W: Week Code
A~Z=W1~W26
A~Z=W27~W52
    __ : Lead Free Package

*Marking for SG6859ATZ (Pb-free)

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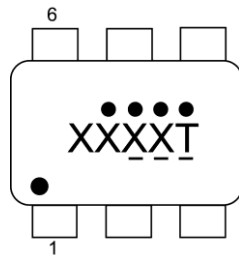
XXXX: AAJF=SG6859A
T : Die Run Code
. . . . : Year Code
- - - : Week Code

*Marking for SG6859ATY (Green Compound)

SG6859ATP
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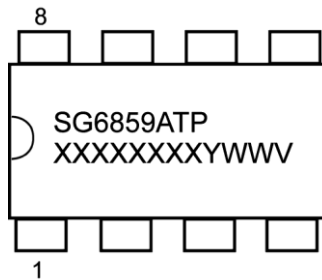
T: D=DIP
P: Z= Lead Free + RoHS Compatible
    Null=Regular Package
XXXXXXXX: Wafer Lot
Y: Year
WW: Week
V: Assembly Location

*Marking for SG6859ADZ (Pb-free)

*F*ZXYTT
6859A
TPM
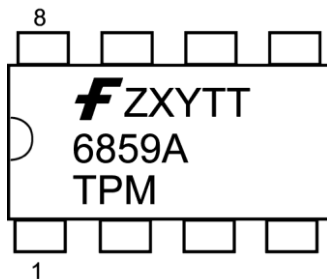
***F*- Fairchild Logo**
Z- Plant Code
X- 1-Digit Year Code
Y- 1-Digit Week Code
TT: 2-Digit Die Run Code
T: Package Type (D=DIP)
P: Y: Green Package
M: Manufacture Flow Code

*Marking for SG6859ADY (Green Compound)

Figure 3. Top Mark

Pin Configurations
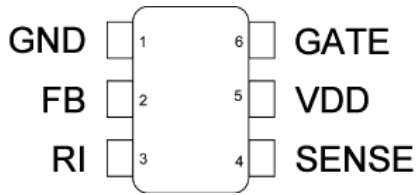
Figure 4. SOT23-6L Pin Configuration
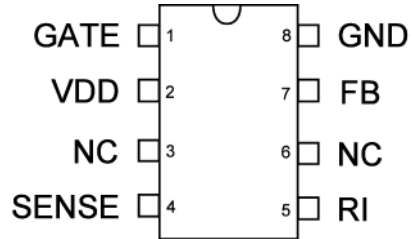
Figure 5. DIP-8 Pin Configuration

Pin Definitions

DIP Pin #	SOT Pin #	Name	Description
1	6	GATE	The totem-pole output driver for driving the power MOSFET.
2	5	VDD	Power supply
3		NC	No connection
4	4	SENSE	Current sense. This pin senses the voltage across a resistor. When the voltage reaches the internal threshold, PWM output is disabled. This activates over-current protection. This pin also provides current amplitude information for current-mode control.
5	3	RI	A resistor connected from the RI pin to ground generates a constant current source used to charge an internal capacitor and determine the switching frequency. Increasing the resistance reduces the amplitude of the current source and the switching frequency. A 95 kΩ resistor R_I results in a 50 µA constant current I_I and a 70 kHz switching frequency.
6		NC	No connection
7	2	FB	Feedback. The FB pin provides the output voltage regulation signal. It provides feedback to the internal PWM comparator, so that the PWM comparator can control the duty cycle.
8	1	GND	Ground

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{VDD}	DC Supply Voltage[1, 2]			30	V
V_{FB}	Input Voltage to FB Pin		-0.3	7.0	V
V_{SENSE}	Input Voltage to Sense Pin		-0.3	7.0	V
T_J	Operating Junction Temperature			150	°C
Θ_{JA}	Thermal Resistance (Junction-to-Air)	SOT23-6L		273	°C/W
		DIP		113	°C/W
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Temperature (Wave Soldering or IR, 10 Seconds)			+260	°C
ESD	Electrostatic Discharge Capability, Human Body Model JESD22-A114			3.5	kV
	Electrostatic Discharge Capability, Charged Device Model JESD22-C101			1.5	kV
	Electrostatic Discharge Capability, Machine Model, JESD22-A115			200	V

Notes:
1. All voltage values, except differential voltages, are given with respect to GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

Electrical Characteristics

Unless otherwise noted, V_{DD}=15 V and T_A=25°C.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
V_{DD} Section							
V_{DD-OP}	Continuously Operation Voltage					22	V
V_{DD-ON}	Turn-on Threshold Voltage			15.5	16.5	17.5	V
V_{DD-OFF}	Turn-off Threshold Voltage			8.5	9.5	10.5	V
I_{DD-ST}	Startup Current		$V_{DD}=V_{DD-ON}$ – 0.1 V		9	15	µA
I_{DD-OP}	Operating Supply Current		V_{DD}=15 V, C_L=1 nF		3.0	3.5	mA
V_{DD-OVP}	V_{DD} Over-Voltage Protection Level		Auto Restart	24	25	26	V
$t_{D-VDDOVP}$	V_{DD} Over-Voltage Protection Debounce		Auto Restart		125		µs
$V_{DD-G\ OFF}$	V_{DD} Low-Threshold Voltage to Exit Green-off Mode				V_{DD-OFF} + 1		V
Feedback Input Section							
Z_{FB}	Input Impedance				5		kΩ
$V_{FB-OPEN}$	FB Output High Voltage			5			V
V_{FB-OL}	FB Open-loop Trigger Level			4.3	4.6	4.9	V
t_{D-OLP}	Delay of FB Pin Open-loop Protection				56		ms
V_{FB-N}	Green-Mode Entry FB Voltage			2.60	2.85	3.10	V
V_{FB-G}	Green-Mode Ending FB Voltage				2.2		V
S_G	Green-Mode Modulation Slope		R_I=95 kΩ	40	75	100	Hz/mV
Current-Sense Section							
Z_{SENSE}	Input Impedance			10			kΩ
t_{PD}	Delay to Output			40	55	100	ns
V_{STHFL}	Flat Threshold Voltage for Current Limit				1		V
V_{STHVA}	Valley Threshold Voltage for Current Limit			0.75	0.80	0.85	V
t_{LEB}	Leading-Edge Blanking Time			270	320	370	ns
DCY_{SAW}	Duty Cycle of SAW Limit				40		%
Oscillator Section							
f_{OSC}	Frequency	Center Frequency	R_I=95 kΩ	65	70	75	kHz
		Hopping Range			±4.9		
T_{HOP}	Hopping Period		R_I=95 kΩ		3.7		ms
f_{OSC-G}	Green-Mode Frequency		R_I=95 kΩ		20		kHz
f_{DV}	Frequency Variation vs. V_{DD} Deviation		V_{DD}=13.5 to 22 V	0	0.02	2.00	%
f_{DT}	Frequency Variation vs. Temp. Deviation		T_A=-20 to 85°C			2	%
Output Section							
DCY_{MAX}	Maximum Duty Cycle			62	67	72	%
V_{GATE-L}	Output Voltage Low		V_{DD}=15 V, I_O=20 mA			1.4	V
V_{GATE-H}	Output Voltage High		V_{DD}=13.5 V, I_O=20 mA	8			V
t_r	Rising Time		V_{DD}=15 V, C_L=1 nF		150		ns
t_f	Falling Time		V_{DD}=15 V, C_L=1 nF		55		ns
$V_{GATE-CLAMP}$	Output Clamp Voltage		V_{DD}=22 V	16	17	18	V

Typical Performance Characteristics
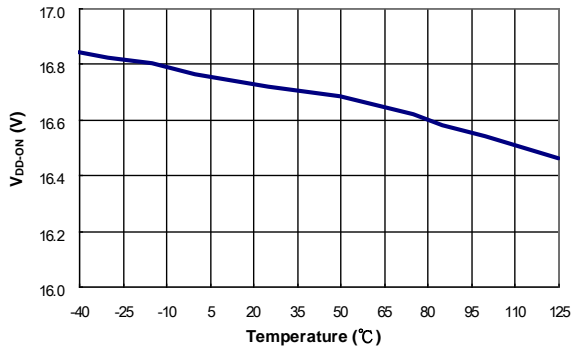

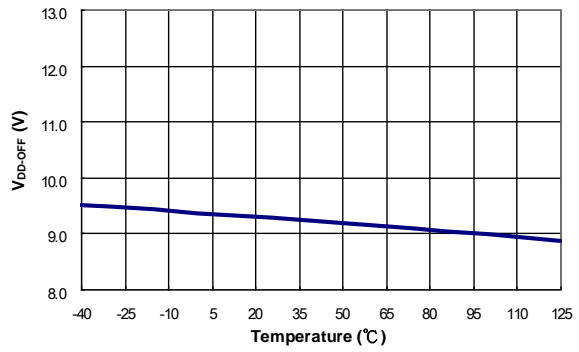Figure 6.   Turn-on Threshold Voltage (V_DD-ON)
vs. Temperature

Figure 7.   Turn-off Threshold Voltage (V_DD-ON)
vs. Temperature
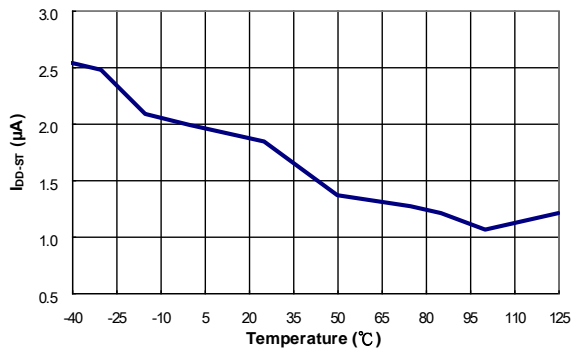

Figure 8.   Startup Current (I_DD-ST) vs. Temperature

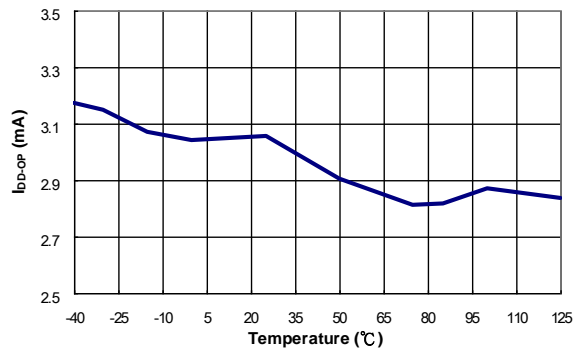

Figure 9.   Operating Supply Current (I_DD-OP)
vs. Temperature
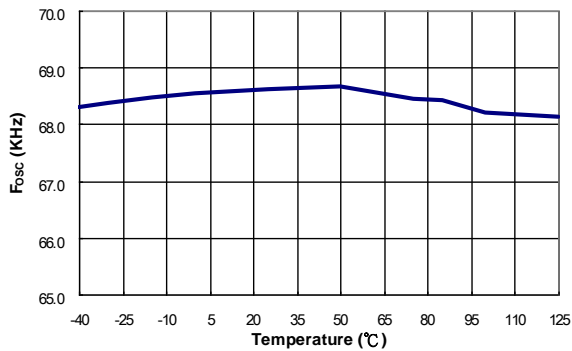

Figure 10. Center Frequency (f_OSC) vs. Temperature
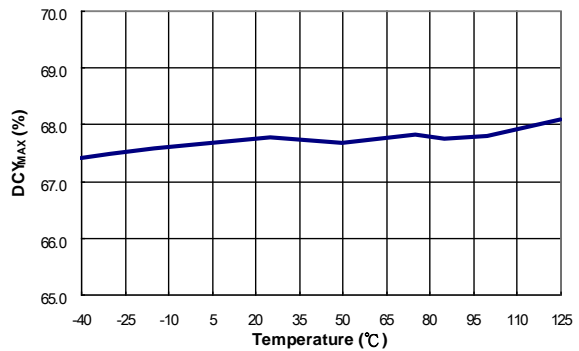

Figure 11. Maximum Duty Cycle (DCY_MAX)
vs. Temperature

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SG6859A — Low-Cost, Green-Mode PWM Controller for Flyback Converters
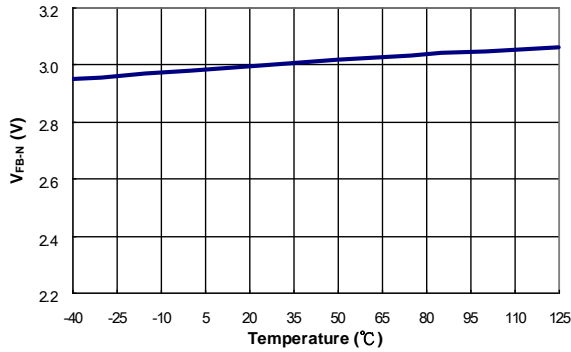
Typical Performance Characteristics

Figure 12. Green-Mode Entry FB Voltage (V$_{FB-N}$) vs. Temperature
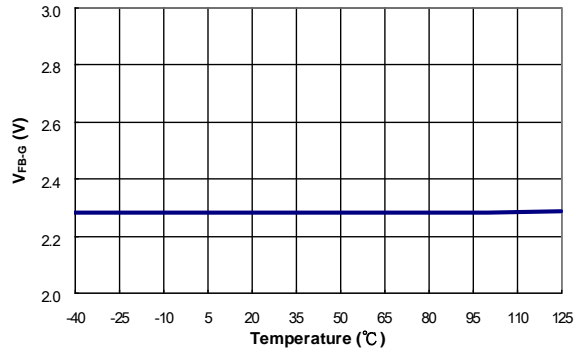

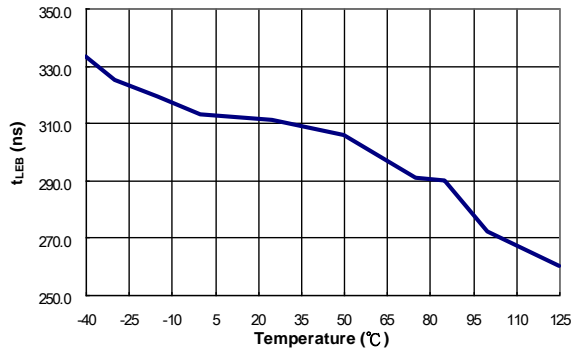**Figure 13. Green-Mode Ending FB Voltage (V$_{FB-G}$) vs. Temperature**

Figure 14. Leading-Edge Blanking Time (t$_{LEB}$) vs. Temperature
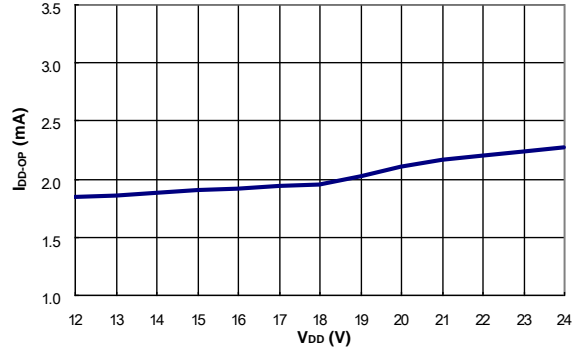

Figure 15. Operating Supply Current vs. V$_{DD}$ Voltage

Operation Description

SG6859A devices integrate many useful designs into one controller for low-power, switch-mode power supplies. The following descriptions highlight some of the features of the SG6859A series.

Startup Current

The startup current is only 9 µA. Low startup current allows a startup resistor with high resistance and low-wattage to supply the startup power for the controller. A 1.5 MΩ, 0.25 W, startup resistor and a 10 µF/25V V_{DD} hold-up capacitor are sufficient for an AC-to-DC power adapter with a wide input range (100 V_{AC} to 240 V_{AC}).

Operating Current

The operating current has been reduced to 3 mA. The low operating current results in higher efficiency and reduces the V_{DD} hold-up capacitance requirement.

Green-Mode Operation

The proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency under light-load conditions. On-time is limited to provide stronger protection against brownouts and other abnormal conditions. The feedback current, which is sampled from the voltage feedback loop, is taken as the reference. Once the feedback current exceeds the threshold current, the switching frequency starts to decrease. This green-mode function dramatically reduces power consumption under light-load and zero-load conditions. Power supplies using the SG6859A can meet even the strictest regulations regarding standby power consumption.

Oscillator Operation

A resistor connected from the RI pin to ground generates a constant current source used to charge an internal capacitor. The charge time determines the internal clock speed and the switching frequency. Increasing the resistance reduces the amplitude of the input current and the switching frequency. A 95 kΩ R_I resistor results in a 50 µA constant current, I_I, and a 70 kHz switching frequency. The relationship between R_I and the switching frequency is:

$$f_{PWM} = \frac{6650}{R_I(k\Omega)}(kHz) \tag{1}$$

The recommended f_{PWM} is from 50kHz to 80kHz.

Leading-Edge Blanking

Each time the power MOSFET is switched on, a turn-on spike occurs at the sense-resistor. To avoid premature termination of the switching pulse, a 320 ns leading-edge blanking time is built in. Conventional RC filtering can be omitted. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

Constant Output Power Limit

When the SENSE voltage across the sense resistor, R_S, reaches the threshold voltage (around 1 V), the output GATE drive is turned off following a short propagation delay, t_{PD}. This propagation delay introduces an additional current proportional to $t_{PD}\cdot V_{IN}/L_P$. The propagation delay is nearly constant, regardless of the input line voltage V_{IN}. Higher input line voltages result in larger additional currents. At high input line voltages, the output power limit is higher than at low input line voltages. To compensate for this output power limit variation across a wide AC input range, the threshold voltage is adjusted by adding a positive ramp. This ramp signal rises from 0.8 V to 1 V, then flattens out at 1 V. A smaller threshold voltage forces the output GATE drive to terminate earlier, which reduces the total PWM turn-on time and makes the output power equal to that of low line input. This proprietary internal compensation ensures a constant output power limit for a wide AC input voltage range (90 V_{AC} to 264 V_{AC}).

Under-Voltage Lockout (UVLO)

The turn-on and turn-off thresholds are fixed internally at 16.5 V and 9.5 V. During startup, the hold-up capacitor must be charged to 16.5V through the startup resistor to enable the SG6859A. The hold-up capacitor continues to supply VDD until power can be delivered from the auxiliary winding of the main transformer. V_{DD} must not drop below 9.5 V during this startup process. This UVLO hysteresis window ensures that hold-up capacitor is adequate to supply V_{DD} during startup.

Gate Output

The BiCMOS output stage is a fast totem pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 17 V Zener diode to protect power MOSFET transistors against undesired over-voltage gate signals.

Built-in Slope Compensation

The sensed voltage across the current-sense resistor is used for current-mode control and pulse-by-pulse current limiting. Built-in slope compensation improves stability and prevents sub-harmonic oscillations due to peak-current mode control. The SG6859A has a synchronized, positively-sloped ramp built-in at each switching cycle. The slope of the ramp is:

$$\frac{0.36 \times Duty}{Duty\,(max.)} \tag{2}$$

Noise Immunity

Noise from the current sense or the control signal can cause significant pulse-width jitter, particularly in continuous-conduction mode (CCM). While slope compensation helps alleviate these problems, further precautions should still be taken. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the SG6859A, and increasing power MOS gate resistance improve performance.
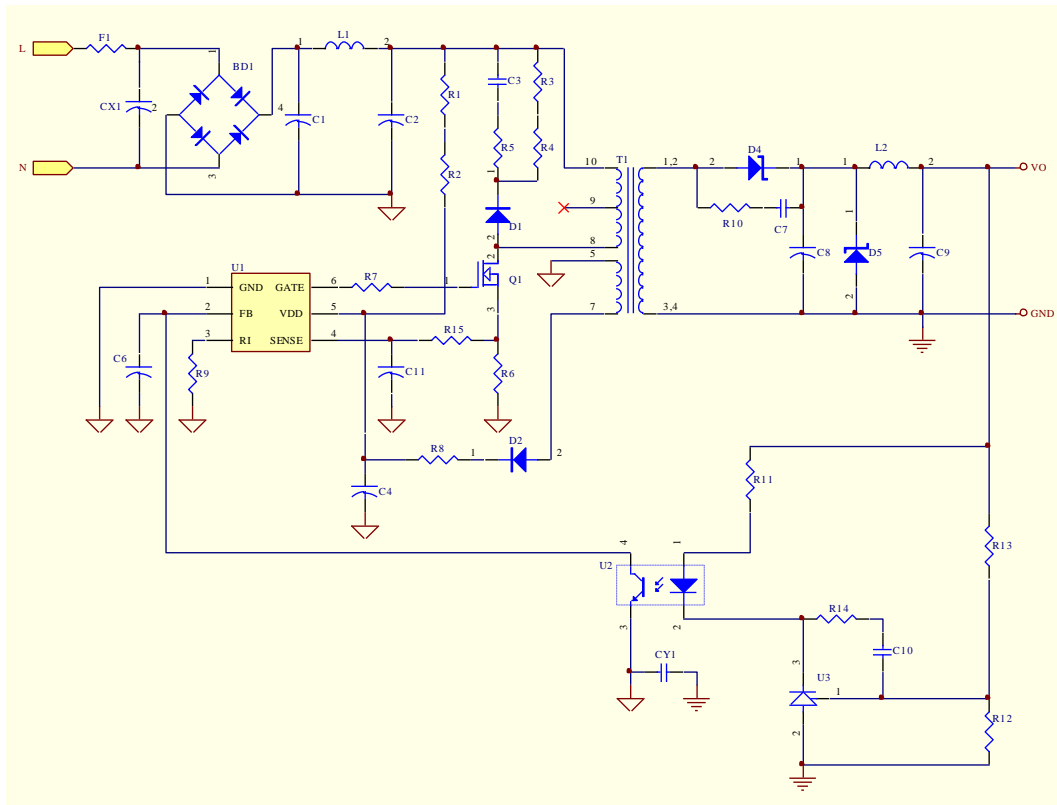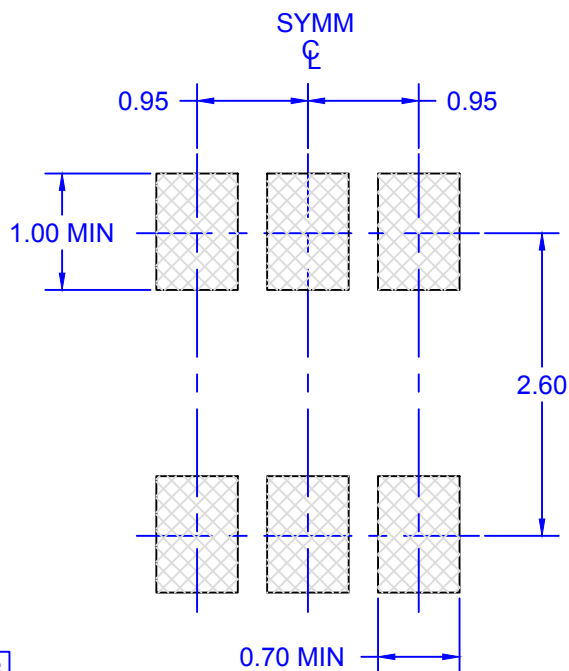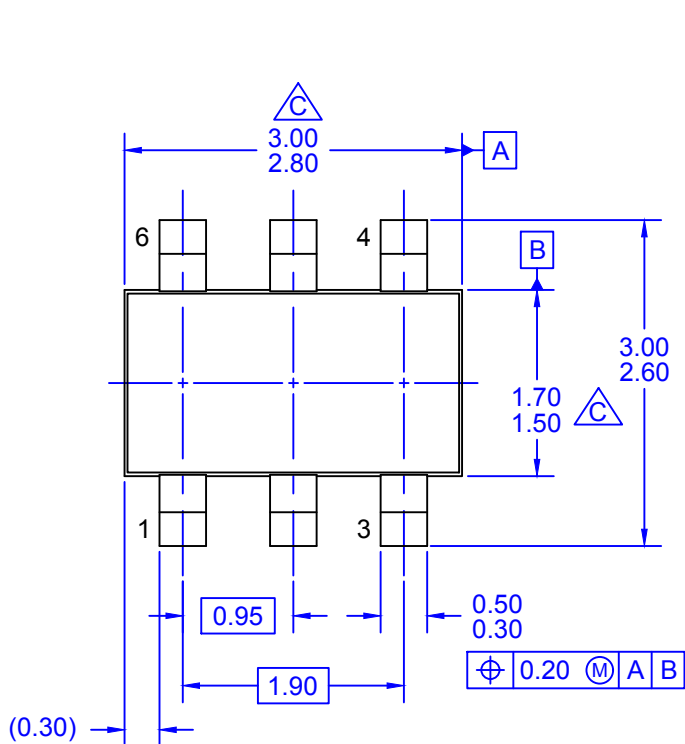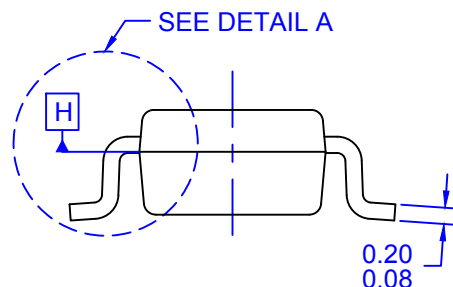
Applications Information

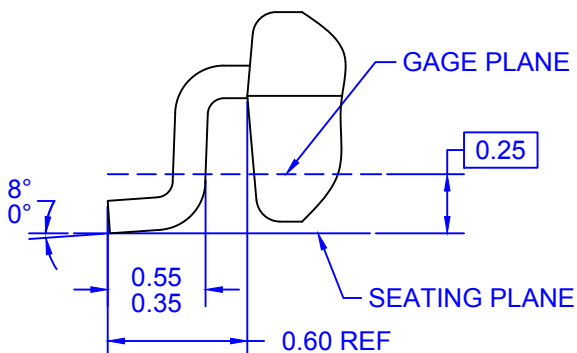**Figure 16. Reference Circuit**

Bill of Materials (BOM)

Reference	Component	Reference	Component
BD1	BD 1 A/500 V	L2	10 µH 6 mm
CX1 (Optional)	XC 0.1 µF	Q1	MOSFET 1 A/600 V
CY1 (Optional)	YC 1nF/400 V (Y1)	R1,R2	R 750 KΩ 1206
C1	CC 10 nF/500 V	R3,R4	R 47 KΩ 1206
C2	EC 10 µF/400 V 105°C	R5	R 47 Ω 1206
C3	CC 1 nF/500 V	R6	R 4.7 Ω 1206
C4	EC 10 µF/50 V	R7	R 100 Ω 0805
C6	CC 4.7 nF 0805	R8	R 10 Ω 1206
C7 (Optional)	CC 1 nF/100 V 1206	R9	R 100 KΩ 0805
C8	EC 470 µF/10 V 105°C	R10 (Optional)	R 10 Ω 1206
C9	EC 220 µF/10 V 105°C	R11	R 100 Ω 1/8W
C10	CC 2.2 nF 0805	R12	R 33 KΩ 0805
C11	N.C.	R13	R 33 KΩ 1/8W
D1	Diode FRI07	R14	R 4.7 KΩ 0805
D2	Diode FR102	R15	R 0 Ω 0805
D4	Diode SB360	T1	EE-16
D5 (Optional)	ZD 6.8 V 0.5 W	U1	IC SG6859A
F1	R 1 Ω/0.5 W	U2	PC817
L1	20 mH 6•8 mm	U3	TL431

SYMM
CL

0.95 | 0.95

1.00 MIN

2.60

0.70 MIN

LAND PATTERN RECOMMENDATION

△C
3.00
2.80 | A

B

6 4

3.00
2.60

1.70
1.50 △C

1 3

0.95

0.50
0.30

⊕ | 0.20 Ⓜ | A | B

1.90

(0.30)

1.10 MAX

1.00
0.70

0.10
0.00

C

⌒ | 0.10 | C

SEE DETAIL A

H

0.20
0.08
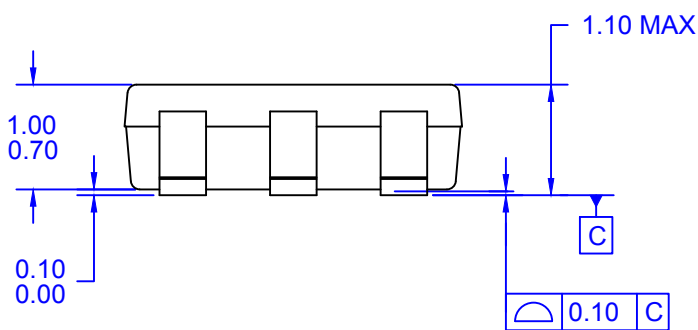
NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC MO-193.
   VAR. AA, ISSUE E.
B) ALL DIMENSIONS ARE IN MILLIMETERS.

△C PACKAGE LENGTH DOES NOT INCLUDE MOLD
   FLASH, PROTRUSIONS OR GATE BURRS. MOLD
   FLASH, PROTRUSIONS OR GATE BURRS SHALL
   NOT EXCEED 0.25mm PER END. PACKAGE WIDTH
   DOES NOT INCLUDE INTERLEAD FLASH OR
   PROTRUSION. INTERLEAD FLASH OR
   PROTRUSION SHALL NOT EXCEED 0.25mm PER
   SIDE. PACKAGE LENGTH AND WIDTH DIMENSIONS
   ARE DETERMINED AT DATUM H.
D) DRAWING FILE NAME: MKT-MA06AREVF

GAGE PLANE

0.25

8°
0°

0.55
0.35

SEATING PLANE

0.60 REF

DETAIL A
SCALE: 50X

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ON

PUBLICATION ORDERING INFORMATION

◊