PZT2222A

NPN Silicon Planar Epitaxial Transistor

This NPN Silicon Epitaxial transistor is designed for use in linear and switching applications. The device is housed in the SOT−223 package which is designed for medium power surface mount applications.

Features

- PNP Complement is PZT2907AT1
- The SOT−223 Package Can be Soldered Using Wave or Reflow
- SOT−223 Package Ensures Level Mounting, Resulting in Improved Thermal Conduction, and Allows Visual Inspection of Soldered Joints
- The Formed Leads Absorb Thermal Stress During Soldering, Eliminating the Possibility of Damage to the Die
- Available in 12 mm Tape and Reel
- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	40	Vdc
Collector−Base Voltage	V_{CBO}	75	Vdc
Emitter−Base Voltage (Open Collector)	V_{EBO}	6.0	Vdc
Collector Current	I_C	600	mAdc
Total Power Dissipation up to T_A = 25°C (Note 1)	P_D	1.5	W
Storage Temperature Range	T_{stg}	− 65 to +150	°C
Junction Temperature Range	T_J	− 55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Device mounted on an epoxy printed circuit board 1.575 inches x 1.575 inches x 0.059 inches; mounting pad for the collector lead min. 0.93 inches^2.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	83.3	°C/W
Lead Temperature for Soldering, 0.0625″ from case Time in Solder Bath	T_L	260 10	°C Sec

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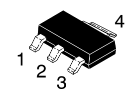
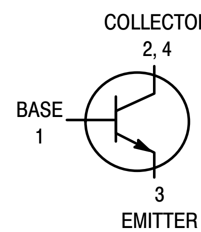
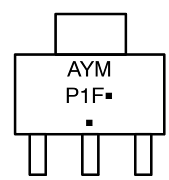
SOT−223 PACKAGE
NPN SILICON TRANSISTOR
SURFACE MOUNT



SOT−223 (TO−261)
CASE 318E−04
STYLE 1



MARKING DIAGRAM



A = Assembly Location
Y = Year
M = Month Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
PZT2222AT1G	SOT−223 (Pb−Free)	1,000 Tape & Reel
SPZT2222AT1G	SOT−223 (Pb−Free)	1,000 Tape & Reel
PZT2222AT3G	SOT−223 (Pb−Free)	4,000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	40	–	Vdc
Collector–Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	$V_{(BR)CBO}$	75	–	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	6.0	–	Vdc
Base–Emitter Cutoff Current (V_{CE} = 60 Vdc, V_{BE} = – 3.0 Vdc)	I_{BEX}	–	20	nAdc
Collector–Emitter Cutoff Current (V_{CE} = 60 Vdc, V_{BE} = – 3.0 Vdc)	I_{CEX}	–	10	nAdc
Emitter–Base Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	–	100	nAdc
Collector–Base Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0, T_A = 125°C)	I_{CBO}	 – –	 10 10	 nAdc μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 0.1 mAdc, V_{CE} = 10 Vdc) (I_C = 1.0 mAdc, V_{CE} = 10 Vdc) (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 10 mAdc, V_{CE} = 10 Vdc, T_A = – 55°C) (I_C = 150 mAdc, V_{CE} = 10 Vdc) (I_C = 150 mAdc, V_{CE} = 1.0 Vdc) (I_C = 500 mAdc, V_{CE} = 10 Vdc)	h_{FE}	 35 50 70 35 100 50 40	 – – – – 300 – –	–
Collector–Emitter Saturation Voltages (I_C = 150 mAdc, I_B = 15 mAdc) (I_C = 500 mAdc, I_B = 50 mAdc)	$V_{CE(sat)}$	 – –	 0.3 1.0	Vdc
Base–Emitter Saturation Voltages (I_C = 150 mAdc, I_B = 15 mAdc) (I_C = 500 mAdc, I_B = 50 mAdc)	$V_{BE(sat)}$	 0.6 –	 1.2 2.0	Vdc
Input Impedance (V_{CE} = 10 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz) (V_{CE} = 10 Vdc, I_C = 10 mAdc, f = 1.0 kHz)	h_{ie}	 2.0 0.25	 8.0 1.25	kΩ
Voltage Feedback Ratio (V_{CE} = 10 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz) (V_{CE} = 10 Vdc, I_C = 10 mAdc, f = 1.0 kHz)	h_{re}	 – –	 8.0×10^{-4} 4.0×10^{-4}	–
Small–Signal Current Gain (V_{CE} = 10 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz) (V_{CE} = 10 Vdc, I_C = 10 mAdc, f = 1.0 kHz)	$\|h_{fe}\|$	 50 75	 300 375	–
Output Admittance (V_{CE} = 10 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz) (V_{CE} = 10 Vdc, I_C = 10 mAdc, f = 1.0 kHz)	h_{oe}	 5.0 25	 35 200	μmhos
Noise Figure (V_{CE} = 10 Vdc, I_C = 100 μAdc, f = 1.0 kHz)	F	–	4.0	dB
DYNAMIC CHARACTERISTICS				
Current–Gain – Bandwidth Product (I_C = 20 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	 300	 –	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_c	–	8.0	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	C_e	–	25	pF

SWITCHING TIMES (T_A = 25°C)

Characteristic	Conditions	Symbol	Min	Max	Unit
Delay Time	(V_{CC} = 30 Vdc, I_C = 150 mAdc, $I_{B(on)}$ = 15 mAdc, $V_{EB(off)}$ = 0.5 Vdc) Figure 1	t_d	–	10	ns
Rise Time		t_r	–	25	
Storage Time	(V_{CC} = 30 Vdc, I_C = 150 mAdc, $I_{B(on)}$ = $I_{B(off)}$ = 15 mAdc) Figure 2	t_s	–	225	ns
Fall Time		t_f	–	60	

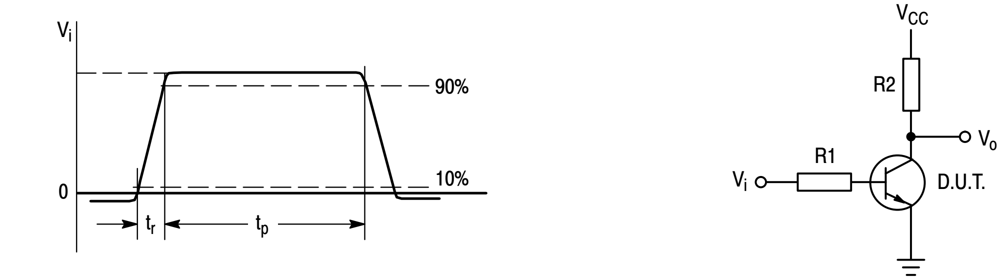


Figure 1. Input Waveform and Test Circuit for Determining Delay Time and Rise Time

V_i = – 0.5 V to +9.9 V, V_{CC} = +30 V, R1 = 619 Ω, R2 = 200 Ω.

PULSE GENERATOR:				**OSCILLOSCOPE:**			
PULSE DURATION	t_p	3	200 ns	**INPUT IMPEDANCE**	Z_i	>	100 kΩ
RISE TIME	t_r	3	2 ns	**INPUT CAPACITANCE**	C_i	<	12 pF
DUTY FACTOR	δ	=	0.02	**RISE TIME**	t_r	<	5 ns

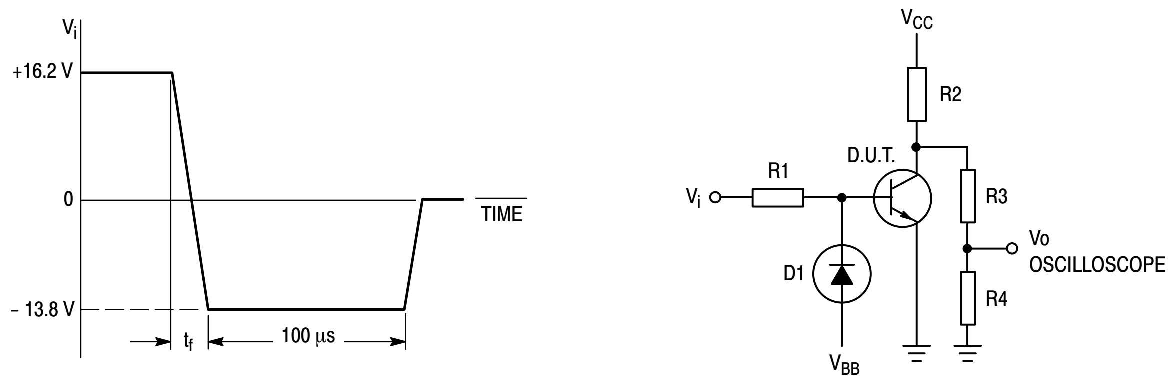


Figure 2. Input Waveform and Test Circuit for Determining Storage Time and Fall Time

TYPICAL CHARACTERISTICS

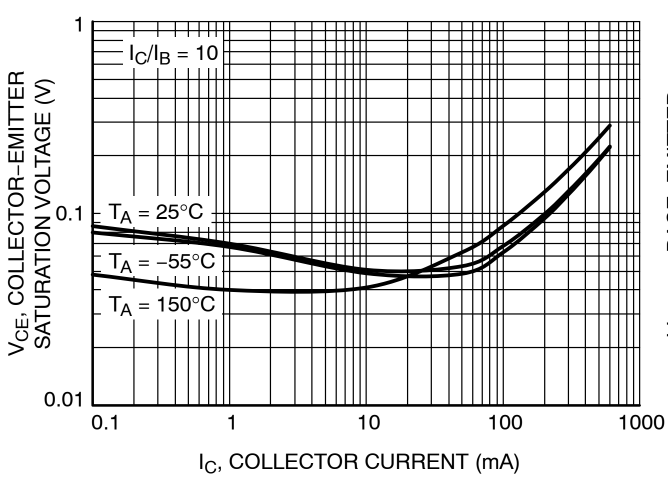


Figure 3. Collector Emitter Saturation Voltage vs. Collector Current

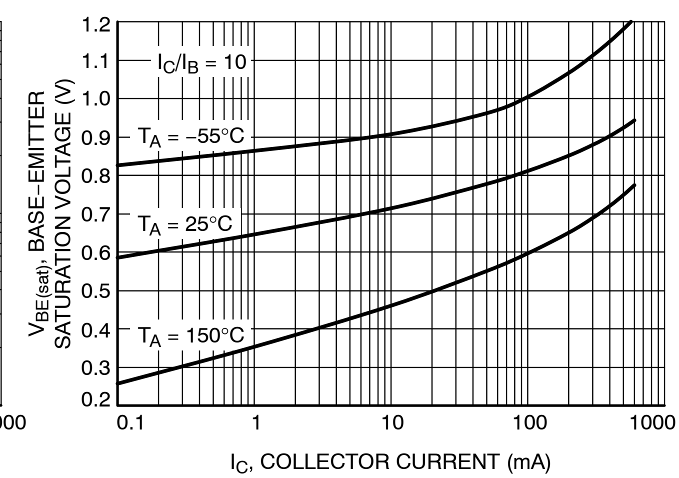


Figure 4. Base Emitter Saturation Voltage vs. Collector Current

TYPICAL CHARACTERISTICS

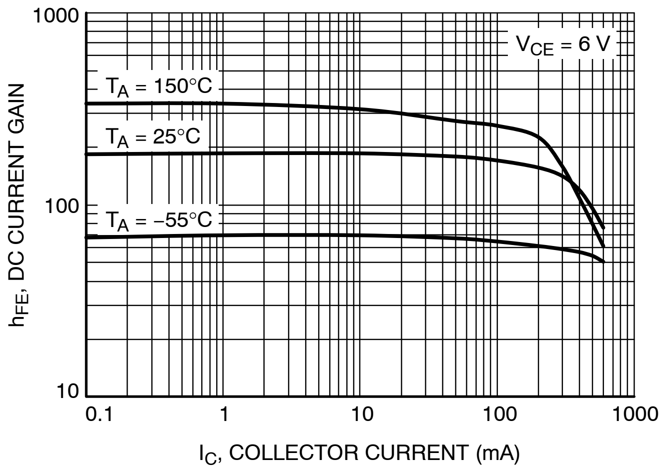


Figure 5. DC Current Gain vs. Collector Current

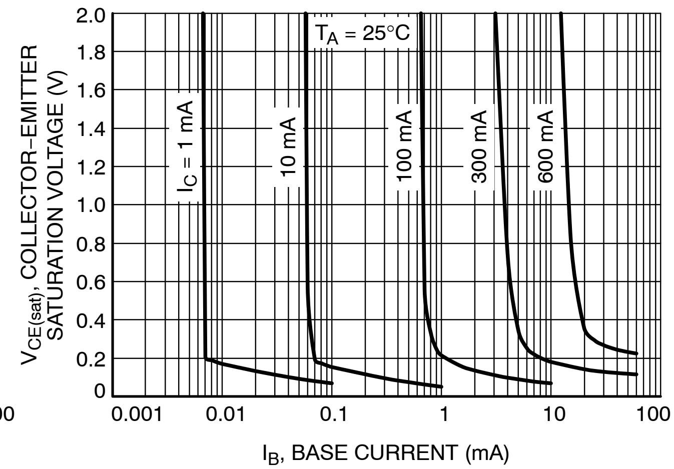


Figure 6. Saturation Region

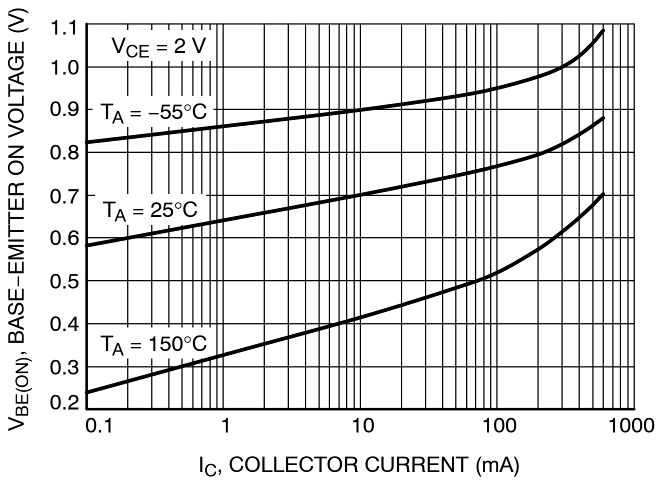


Figure 7. Base−Emitter Turn−On Voltage vs. Collector Current

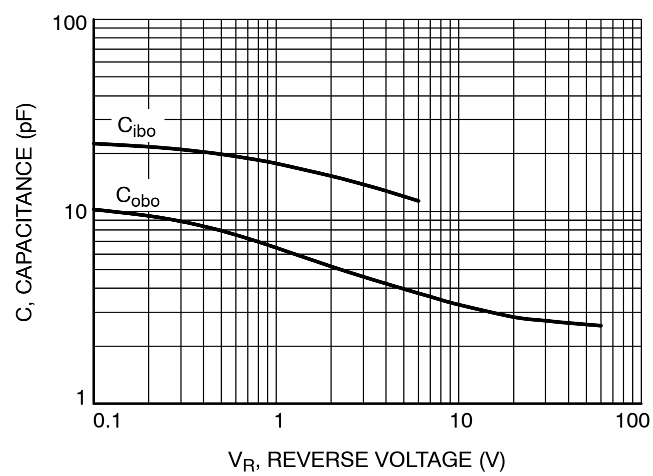


Figure 8. Capacitance

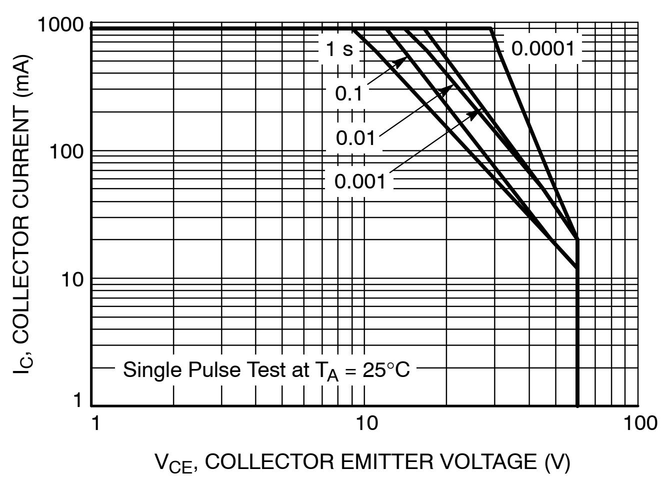


Figure 9. Safe Operating Area

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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