

# MOSFET - Power, Single N-Channel, WDFN8

## 25 V, 1.3 mΩ, 150 A

### NTTFS1D8N02P1E

#### Features

- Small Footprint for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### Typical Applications

- DC-DC Converters
- Power Load Switch
- Notebook Battery Management

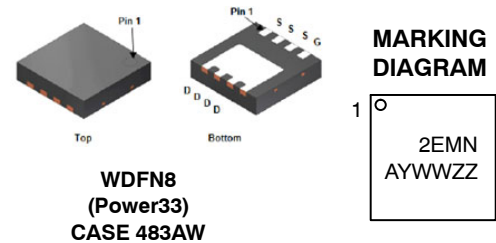
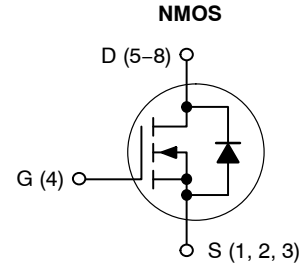
#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DSS}$	25	V	
Gate-to-Source Voltage		$V_{GS}$	+16, -12	V	
Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$	150	A
		$T_C = 85^\circ\text{C}$		108	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	$P_D$	46	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	36	A
		$T_A = 85^\circ\text{C}$		26	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$	2.7	W
Continuous Drain Current $R_{\theta JA}$ (Notes 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	20	A
		$T_A = 85^\circ\text{C}$		14	
Power Dissipation $R_{\theta JA}$ (Notes 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$	0.8	W
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$	508	A	
Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 48.3 \text{ A}, L = 0.1 \text{ mH}$ ) (Note 4)		$E_{AS}$	117	mJ	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$	
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using a 1 in<sup>2</sup> pad size, 2 oz Cu pad.
2. Surface-mounted on FR4 board using minimum pad size, 2 oz Cu pad.
3. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted. Actual continuous current will be limited by thermal & electro-mechanical application board design.  $R_{\theta CA}$  is determined by the user's board design.
4. 100% UIS tested at  $L = 0.1 \text{ mH}, I_{AV} = 32 \text{ A}$ .

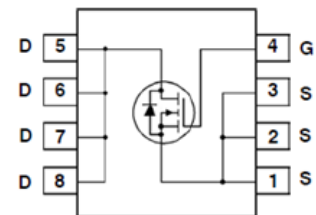
$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
25 V	1.3 mΩ @ 10 V	150 A
	1.8 mΩ @ 4.5 V	



WDFN8 (Power33) CASE 483AW

- 2EMN = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- ZZ = Assembly Lot Code

#### PIN CONNECTIONS



(Top View)

#### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

# NTTFS1D8N02P1E

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case – Steady State (Note 1)	$R_{\theta JC}$	2.7	°C/W
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	47	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	152	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	25			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 1\text{ mA}$ , ref to $25^\circ\text{C}$		16		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$	$T_J = 25^\circ\text{C}$		10	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = +16\text{ V}, -12\text{ V}$			$\pm 100$	$\pm\text{nA}$

## ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 660\ \mu\text{A}$	1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 660\ \mu\text{A}$ , ref to $25^\circ\text{C}$		-4.4		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 17\text{ A}$	1.05	1.3	m $\Omega$
		$V_{GS} = 4.5\text{ V}$	$I_D = 13\text{ A}$	1.3	1.8	
Forward Transconductance	$g_{FS}$	$V_{DS} = 5\text{ V}, I_D = 17\text{ A}$		118		S
Gate Resistance	$R_G$	$T_A = 25^\circ\text{C}$		0.6		$\Omega$

## CHARGES & CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, V_{DS} = 13\text{ V}, f = 1\text{ MHz}$		2980		pF
Output Capacitance	$C_{OSS}$			805		
Reverse Capacitance	$C_{RSS}$			41		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 13\text{ V}; I_D = 17\text{ A}$		17.1		nC
Threshold Gate Charge	$Q_{G(TH)}$			4		
Gate-to-Drain Charge	$Q_{GD}$			2.7		
Gate-to-Source Charge	$Q_{GS}$			7		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 13\text{ V}; I_D = 17\text{ A}$		39		

## SWITCHING CHARACTERISTICS, $V_{GS} = 4.5\text{ V}$ (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DD} = 13\text{ V}, I_D = 17\text{ A}, R_G = 6\ \Omega$		21.3		ns
Rise Time	$t_r$			8		
Turn-Off Delay Time	$t_{d(OFF)}$			30		
Fall Time	$t_f$			7		

## SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$ (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DD} = 13\text{ V}, I_D = 17\text{ A}, R_G = 6\ \Omega$		13		ns
Rise Time	$t_r$			2.8		
Turn-Off Delay Time	$t_{d(OFF)}$			44		
Fall Time	$t_f$			5.4		

## SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 17\text{ A}$	$T_J = 25^\circ\text{C}$		0.77	1.2	V
			$T_J = 125^\circ\text{C}$		0.61		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, di/dt = 100\text{ A}/\mu\text{s}, I_S = 17\text{ A}$			34		ns
Reverse Recovery Charge	$Q_{RR}$				22		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Switching characteristics are independent of operating junction temperatures.

# NTTFS1D8N02P1E

## TYPICAL CHARACTERISTICS

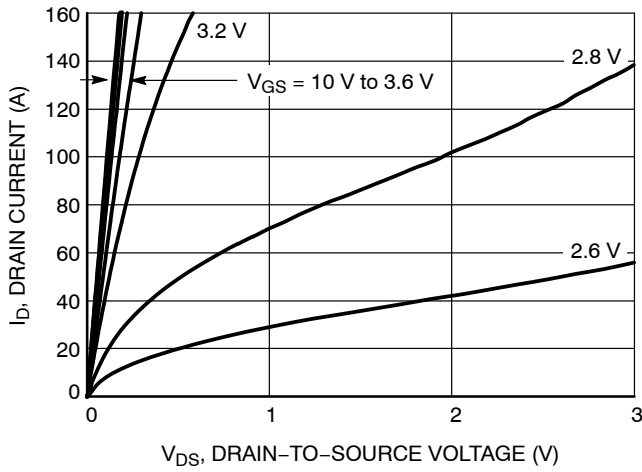


Figure 1. On-Region Characteristics

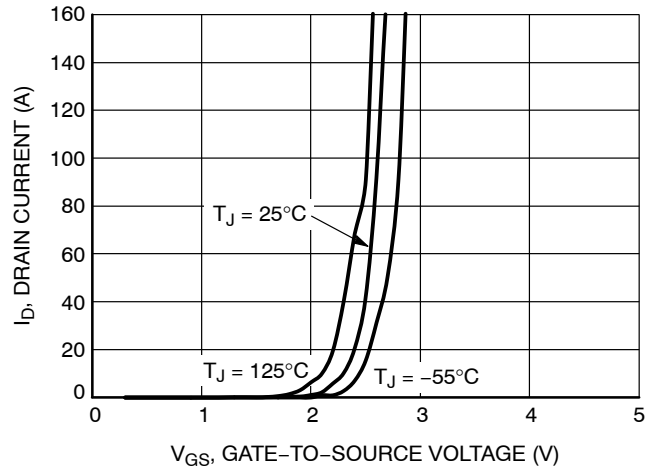


Figure 2. Transfer Characteristics

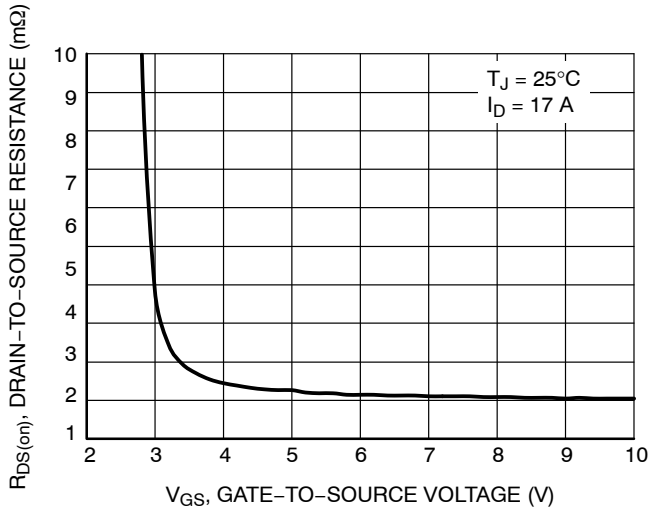


Figure 3. On-Resistance vs. Gate-to-Source Voltage

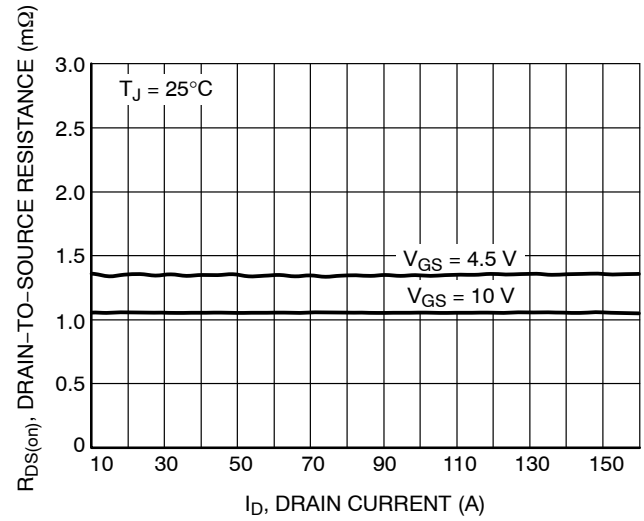


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

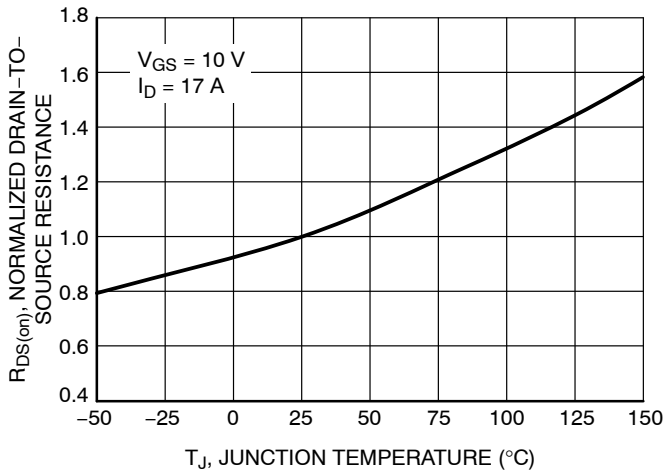


Figure 5. On-Resistance Variation with Temperature

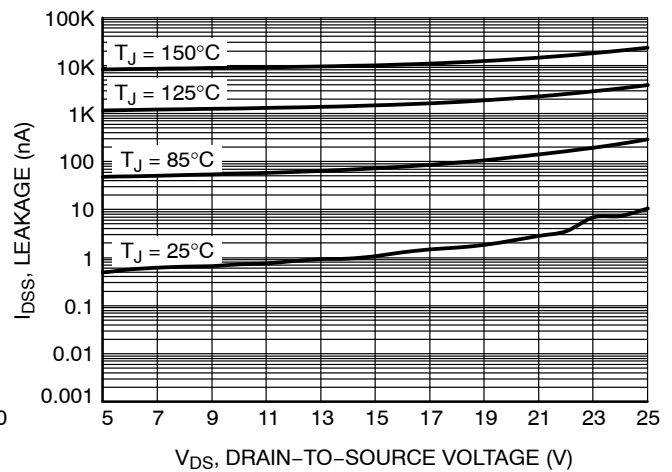


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NTTFS1D8N02P1E

## TYPICAL CHARACTERISTICS

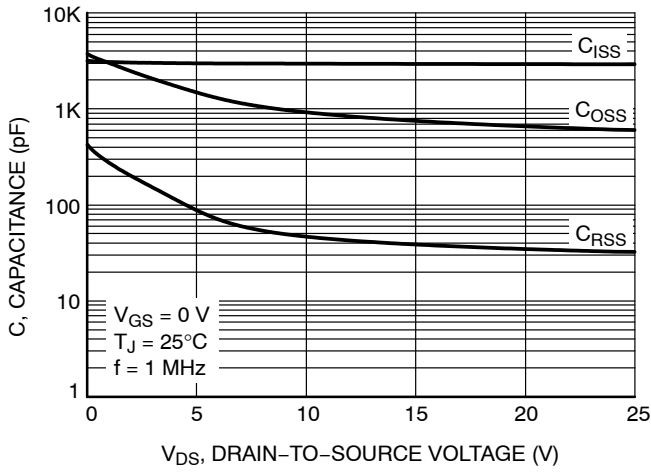


Figure 7. Capacitance Variation

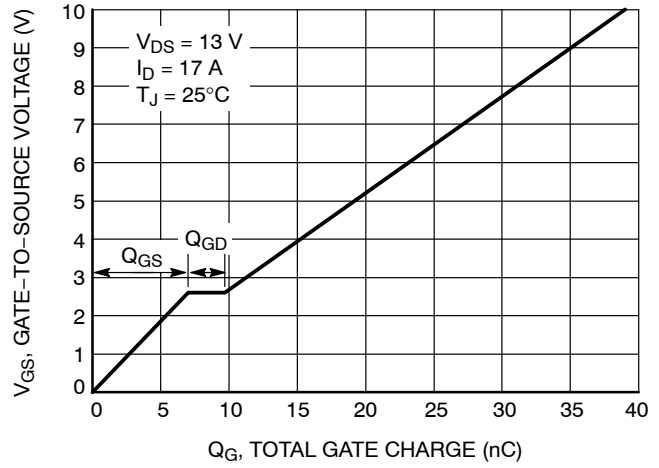


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

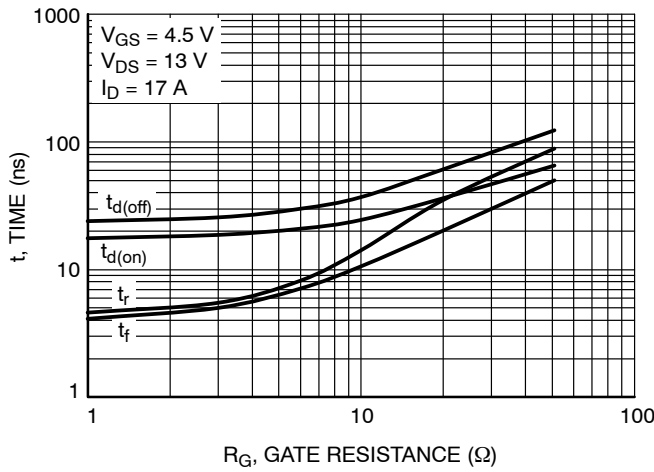


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

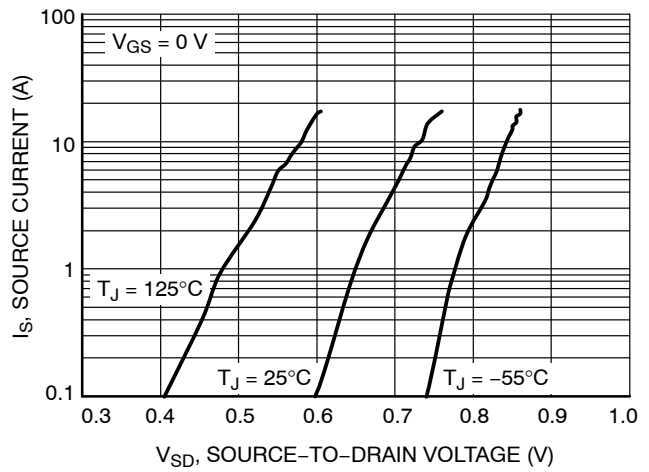


Figure 10. Diode Forward Voltage vs. Current

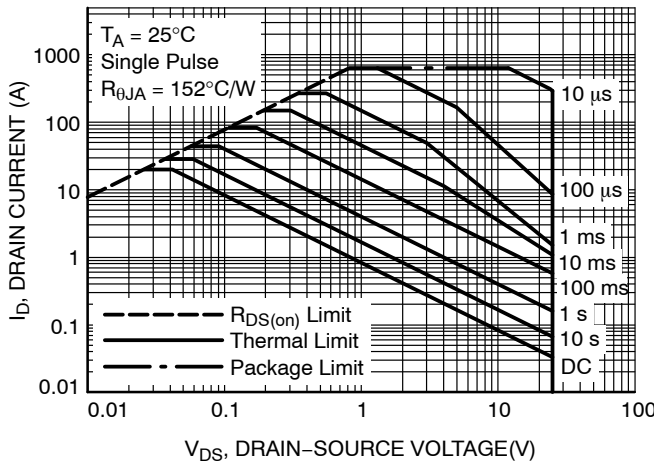


Figure 11. Safe Operating Area

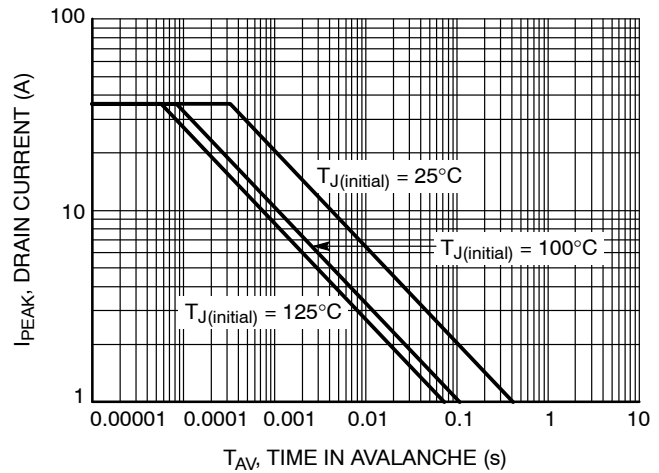


Figure 12.  $I_{PEAK}$  vs. Time in Avalanche

# NTTFS1D8N02P1E

## TYPICAL CHARACTERISTICS

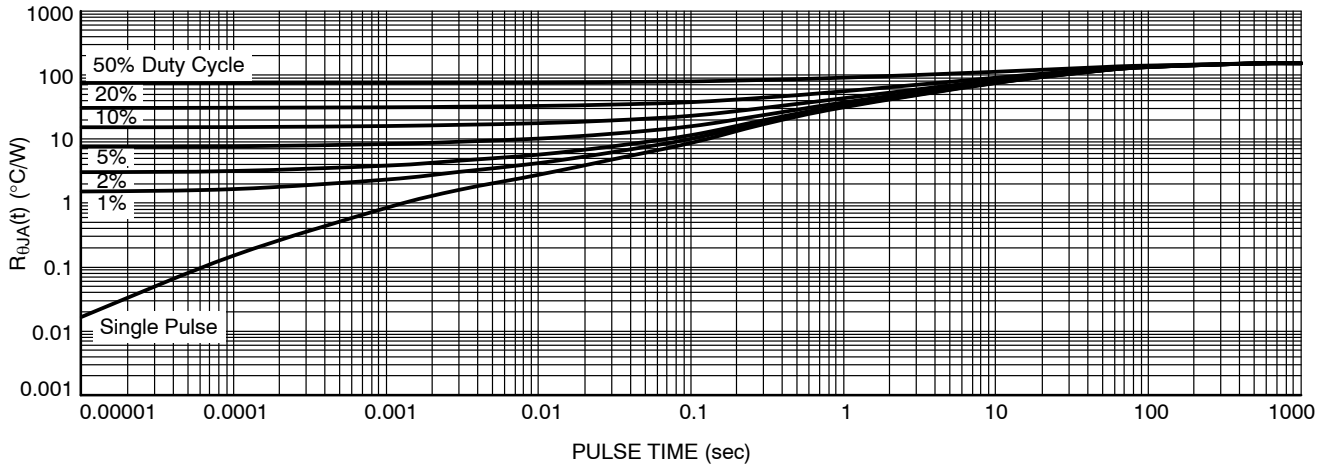


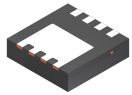
Figure 13. Thermal Characteristics

### ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
NTTFS1D8N02P1E	2EMN	WDFN8 (Pb-Free)	3000 / Tape & Reel

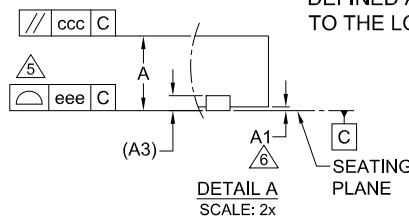
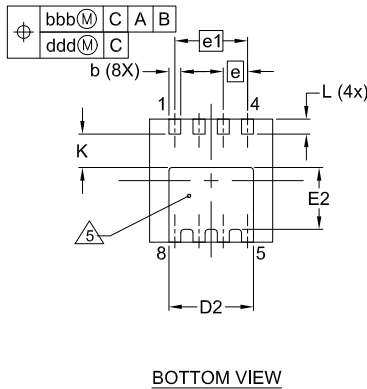
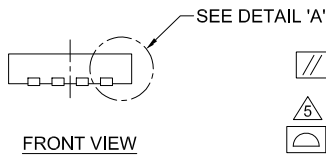
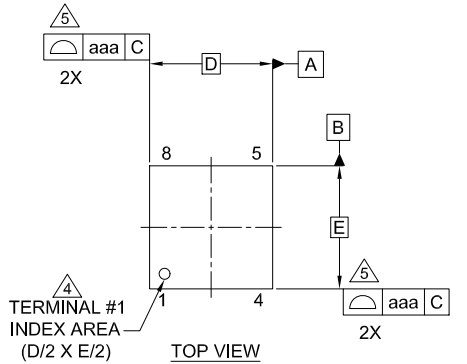
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

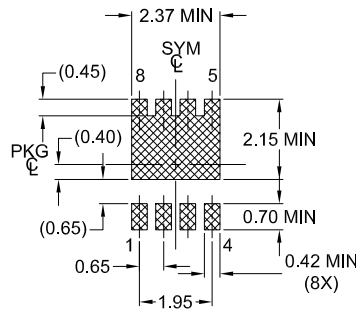


**WDFN8 3.30x3.30x0.75, 0.65P**  
CASE 483AW  
ISSUE B

DATE 22 MAR 2024



### LAND PATTERN RECOMMENDATION



### NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEP95 SEC. 3 SPP-12. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD, EMBEDDED METAL OR MARKED FEATURE.
5. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	--	--	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.30 BSC		
D2	2.17	2.27	2.37
E	3.30 BSC		
E2	1.56	1.66	1.76
e	0.65 BSC		
e1	1.95 BSC		
K	0.90	--	--
L	0.30	0.40	0.50
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.05		

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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<b>DESCRIPTION:</b>	<b>WDFN8 3.30x3.30x0.75, 0.65P</b>	<b>PAGE 1 OF 1</b>

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