NTP30N06L, NTB30N06L

Power MOSFET

30 Amps, 60 Volts, Logic Level, N–Channel TO–220 and D²PAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

• Pb–Free Packages are Available

Typical Applications

• Power Supplies
• Converters
• Power Motor Controls
• Bridge Circuits

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 10 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage – Continuous – Non–Repetitive ($t_p \leq$ 10 ms)	V_{GS} V_{GS}	± 15 ± 20	Vdc
Drain Current – Continuous @ T_A = 25°C – Continuous @ T_A = 100°C – Single Pulse ($t_p \leq$ 10 μs)	I_D I_D I_{DM}	30 15 90	Adc Apk
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	88.2 0.59	W W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to +175	°C
Single Pulse Drain–to–Source Avalanche Energy – Starting T_J = 25°C (V_{DD} = 50 Vdc, V_{GS} = 5.0 Vdc, L = 0.3 mH $I_{L(pk)}$ = 26 A, V_{DS} = 60 Vdc)	E_{AS}	101	mJ
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	1.7	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8 in from case for 10 seconds	T_L	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.
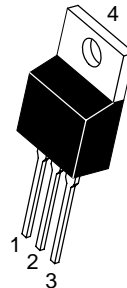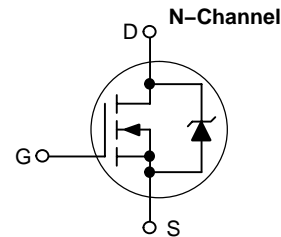
N–Channel

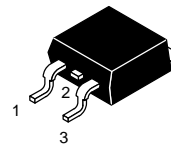**MARKING DIAGRAMS**

TO–220 CASE 221A STYLE 5

4
Drain

NTx30N06LG
AYWW

1 3
Gate Source
2
Drain
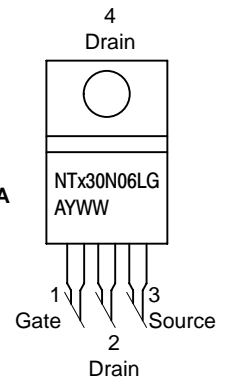
D²PAK CASE 418B STYLE 2

4
Drain

NTx 30N06LG AYWW

1 2 3
Gate Drain Source
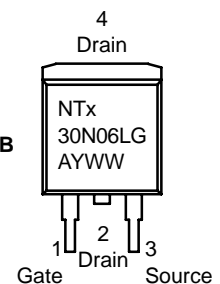
NTx30N06L	= Device Code
x	= P or B
A	= Assembly Location
Y	= Year
WW	= Work Week
G	= Pb–Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Breakdown Voltage (Note 1) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	60 –	71.8 69	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)	I_{DSS}	 – –	 – –	 1.0 10	μAdc
Gate–Body Leakage Current (V_{GS} = ±15 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	–	–	±100	nAdc
ON CHARACTERISTICS (Note 1)					
Gate Threshold Voltage (Note 1) (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	1.0 –	1.7 4.8	2.0 –	Vdc mV/°C
Static Drain–to–Source On–Resistance (Note 1) (V_{GS} = 5.0 Vdc, I_D = 15 Adc)	$R_{DS(on)}$	 –	 38	 46	mΩ
Static Drain–to–Source On–Voltage (Note 1) (V_{GS} = 5.0 Vdc, I_D = 30 Adc) (V_{GS} = 5.0 Vdc, I_D = 15 Adc, T_J = 150°C)	$V_{DS(on)}$	 – –	 1.3 1.06	 1.7 –	Vdc
Forward Transconductance (Note 1) (V_{DS} = 7.0 Vdc, I_D = 15 Adc)	g_{FS}	–	21	–	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	C_{iss}	–	810	1150	pF
Output Capacitance	C_{oss}	–	260	370	
Transfer Capacitance	C_{rss}	–	80	115	

(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz) applies to Input/Output/Transfer Capacitance

SWITCHING CHARACTERISTICS (Note 2)

Characteristic	Symbol	Min	Typ	Max	Unit
Turn–On Delay Time	$t_{d(on)}$	–	10	20	ns
Rise Time	t_r	–	200	400	
Turn–Off Delay Time	$t_{d(off)}$	–	15.6	30	
Fall Time	t_f	–	62	120	
Gate Charge	Q_T	–	16	32	nC
	Q_1	–	3.9	–	
	Q_2	–	10	–	

(V_{DD} = 30 Vdc, I_D = 30 Adc, V_{GS} = 5.0 Vdc, R_G = 9.1 Ω) (Note 1) applies to switching times

(V_{DS} = 48 Vdc, I_D = 30 Adc, V_{GS} = 5.0 Vdc) (Note 1) applies to Gate Charge

SOURCE–DRAIN DIODE CHARACTERISTICS

Characteristic		Symbol	Min	Typ	Max	Unit
Forward On–Voltage	(I_S = 30 Adc, V_{GS} = 0 Vdc) (Note 1) (I_S = 30 Adc, V_{GS} = 0 Vdc, T_J = 150°C)	V_{SD}	– –	1.01 1.03	1.2 –	Vdc
Reverse Recovery Time	(I_S = 30 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (Note 1)	t_{rr}	–	50	–	ns
		t_a	–	32	–	
		t_b	–	17	–	
Reverse Recovery Stored Charge		Q_{RR}	–	0.082	–	μC

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperatures.
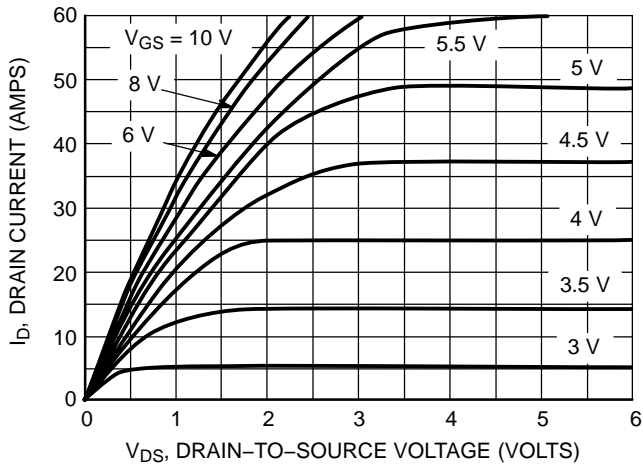
NTP30N06L, NTB30N06L

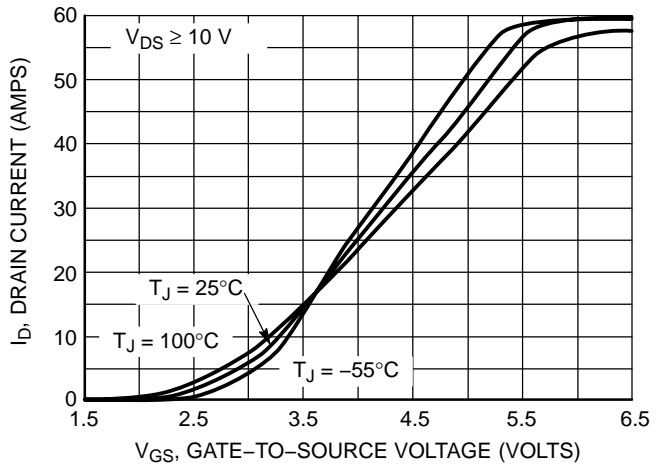Figure 1. On−Region Characteristics

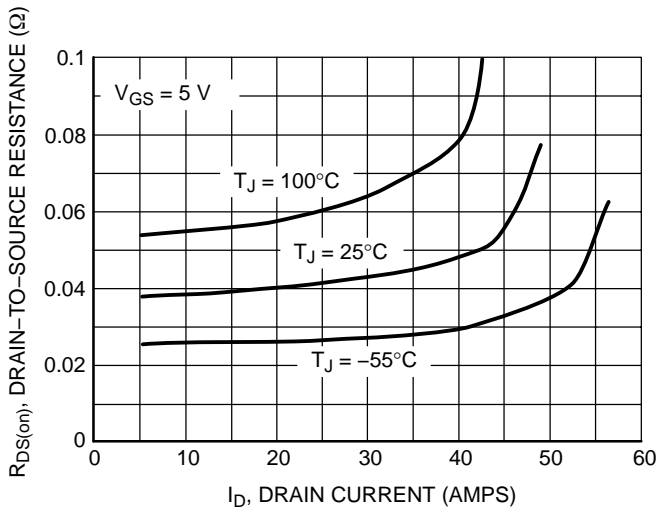$V_{GS} = 10$ V, 8 V, 6 V, 5.5 V, 5 V, 4.5 V, 4 V, 3.5 V, 3 V

I_D, DRAIN CURRENT (AMPS) vs V_{DS}, DRAIN−TO−SOURCE VOLTAGE (VOLTS)

Figure 2. Transfer Characteristics

$V_{DS} \geq 10$ V

$T_J = 25°C$, $T_J = 100°C$, $T_J = -55°C$

I_D, DRAIN CURRENT (AMPS) vs V_{GS}, GATE−TO−SOURCE VOLTAGE (VOLTS)

Figure 3. On−Resistance versus Gate−to−Source Voltage

$V_{GS} = 5$ V

$T_J = 100°C$, $T_J = 25°C$, $T_J = -55°C$

$R_{DS(on)}$, DRAIN−TO−SOURCE RESISTANCE (Ω) vs I_D, DRAIN CURRENT (AMPS)
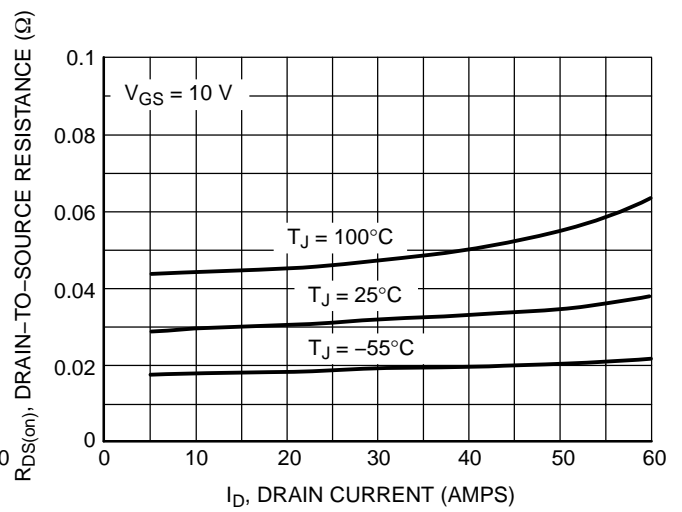
Figure 4. On−Resistance versus Drain Current and Gate Voltage

$V_{GS} = 10$ V

$T_J = 100°C$, $T_J = 25°C$, $T_J = -55°C$

$R_{DS(on)}$, DRAIN−TO−SOURCE RESISTANCE (Ω) vs I_D, DRAIN CURRENT (AMPS)
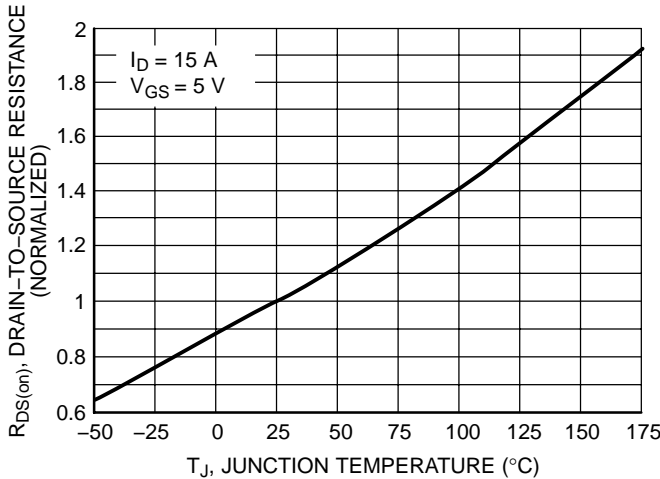
Figure 5. On−Resistance Variation with Temperature

$I_D = 15$ A, $V_{GS} = 5$ V

$R_{DS(on)}$, DRAIN−TO−SOURCE RESISTANCE (NORMALIZED) vs T_J, JUNCTION TEMPERATURE (°C)
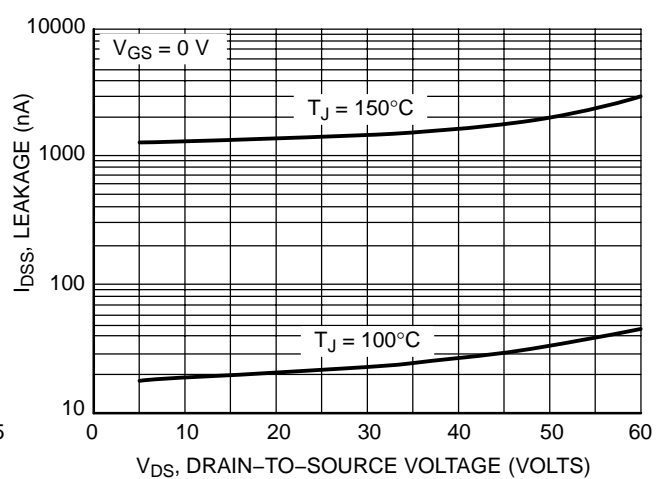
Figure 6. Drain−to−Source Leakage Current versus Voltage

$V_{GS} = 0$ V

$T_J = 150°C$, $T_J = 100°C$

I_{DSS}, LEAKAGE (nA) vs V_{DS}, DRAIN−TO−SOURCE VOLTAGE (VOLTS)

NTP30N06L, NTB30N06L
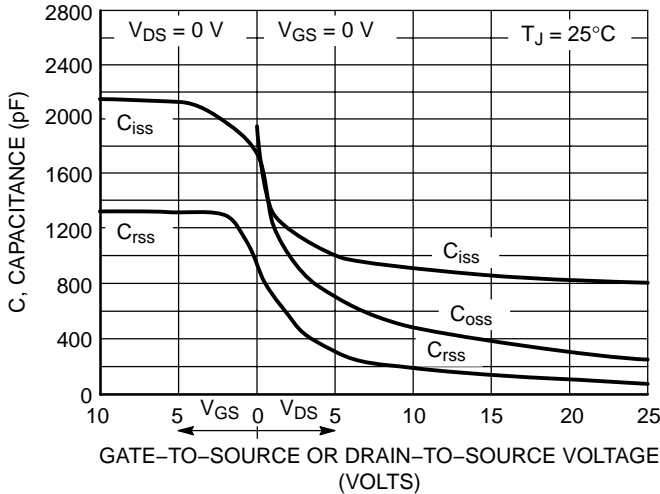
Figure 7. Capacitance Variation
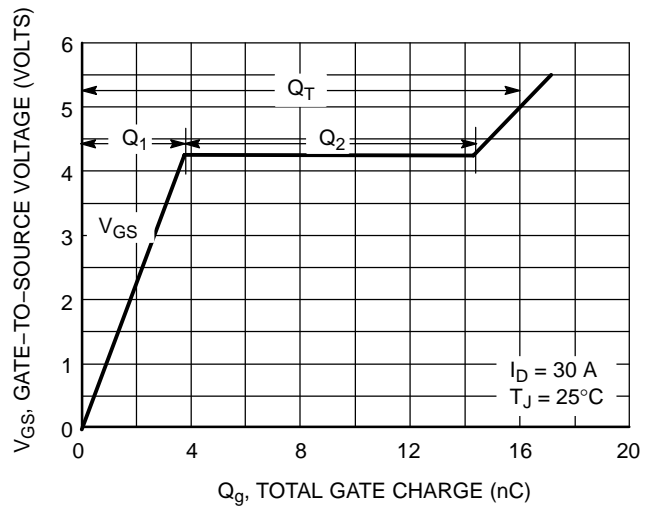
Figure 8. Gate–to–Source and Drain–to–Source Voltage versus Total Charge
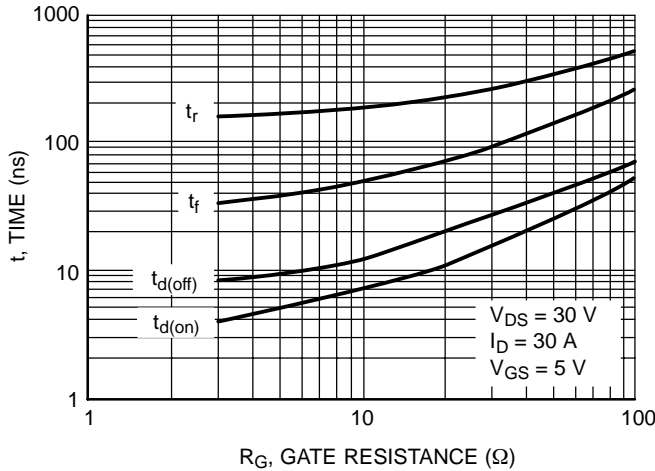
Figure 9. Resistive Switching Time Variation versus Gate Resistance
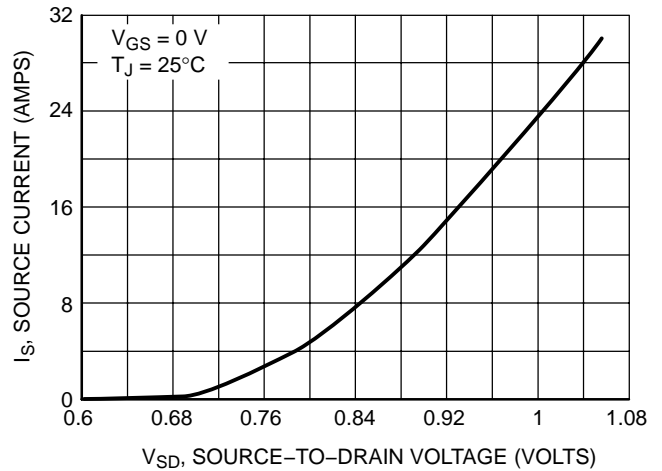
Figure 10. Diode Forward Voltage versus Current
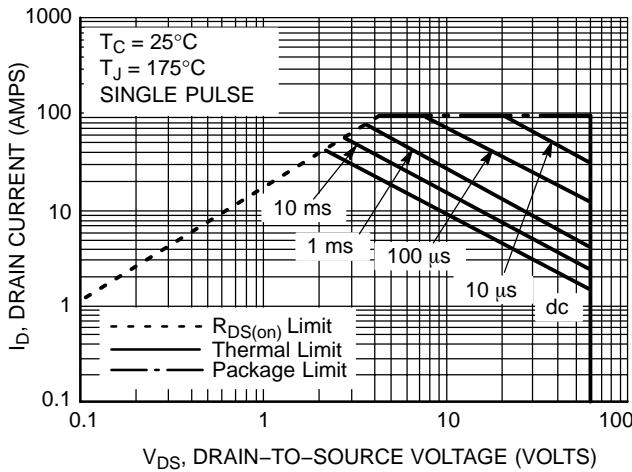
Figure 11. Maximum Rated Forward Biased Safe Operating Area
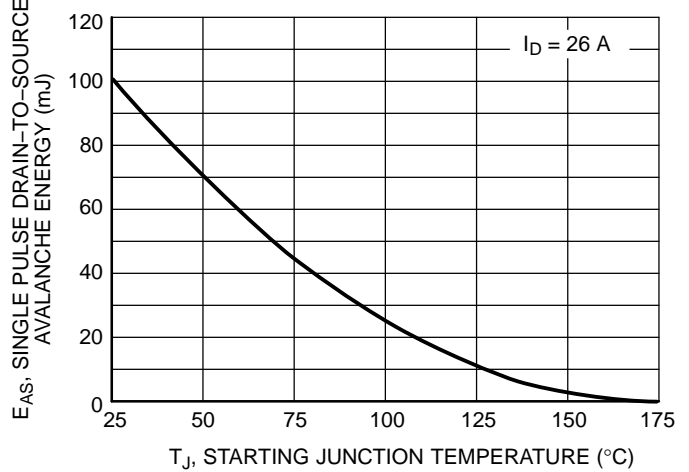
Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature
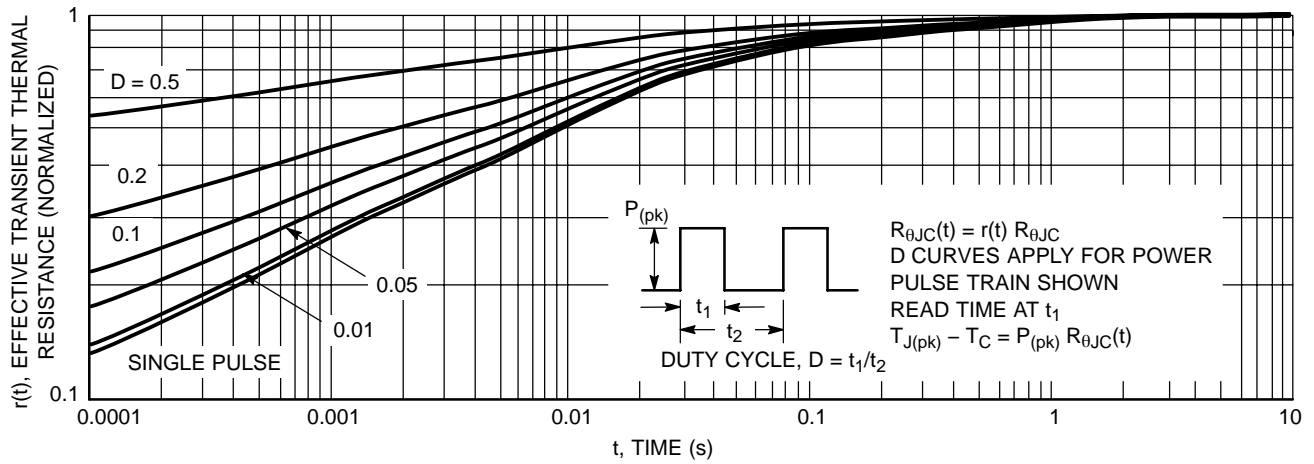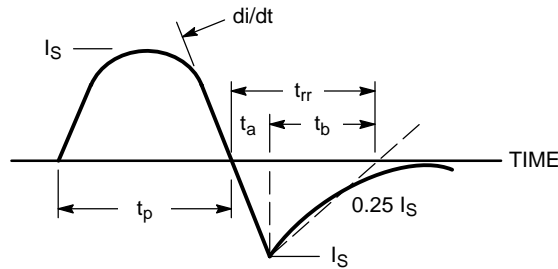
NTP30N06L, NTB30N06L

Figure 13. Thermal Response

$$R_{\theta JC}(t) = r(t)\, R_{\theta JC}$$
D CURVES APPLY FOR POWER
PULSE TRAIN SHOWN
READ TIME AT t_1
$$T_{J(pk)} - T_C = P_{(pk)}\, R_{\theta JC}(t)$$

DUTY CYCLE, $D = t_1/t_2$

Figure 14. Diode Reverse Recovery Waveform

ORDERING INFORMATION

Device	Package	Shipping†
NTP30N06L	TO−220	50 Units / Rail
NTP30N06LG	TO−220 (Pb−Free)	50 Units / Rail
NTB30N06L	D²PAK	50 Units / Rail
NTB30N06LG	D²PAK (Pb−Free)	50 Units / Rail
NTB30N06LT4	D²PAK	800 Tape & Reel
NTB30N06LT4G	D²PAK (Pb−Free)	800 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

D²PAK 3
CASE 418B–04
ISSUE L

DATE 17 FEB 2015

SCALE 1:1

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B–01 THRU 418B–03 OBSOLETE, NEW STANDARD 418B–04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

⊕ | 0.13 (0.005) Ⓜ | T | B Ⓜ

SEATING PLANE –T–

VARIABLE CONFIGURATION ZONE

VIEW W–W 1

VIEW W–W 2

VIEW W–W 3

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. NO CONNECT
2. CATHODE
3. ANODE
4. CATHODE

MARKING INFORMATION AND FOOTPRINT ON PAGE 2

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DESCRIPTION:	D²PAK 3		PAGE 1 OF 2

D²PAK 3
CASE 418B−04
ISSUE L

DATE 17 FEB 2015

GENERIC
MARKING DIAGRAM*

```
   xx              xxxxxxxxG        AYWW
xxxxxxxxx          AYWW          xxxxxxxxG
AWLYWWG                            AKA
```

IC   **Standard**   **Rectifier**

xx   = Specific Device Code
A   = Assembly Location
WL   = Wafer Lot
Y   = Year
WW   = Work Week
G   = Pb−Free Package
AKA   = Polarity Indicator

*This information is generic. Please refer to
 device data sheet for actual part marking.
 Pb−Free indicator, "G" or microdot " ▪ ",
 may or may not be present.

SOLDERING FOOTPRINT*

10.49

8.38

16.155

2X
3.504

2X
1.016

5.080
PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering
 details, please download the ON Semiconductor Soldering and
 Mounting Techniques Reference Manual, SOLDERRM/D.

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ADDITIONAL INFORMATION

◊