

MOSFET – Power, Single, P-Channel with ESD Protection, SOT-723

-20 V, -780 mA

NTK3139P

Features

- P-channel Switch with Low $R_{DS(on)}$
- 44% Smaller Footprint and 38% Thinner than SC-89
- Low Threshold Levels Allowing 1.5 V $R_{DS(on)}$ Rating
- Operated at Low Logic Level Gate Drive
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Load/Power Switching
- Interfacing, Logic Switching
- Battery Management for Ultra Small Portable Electronics

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

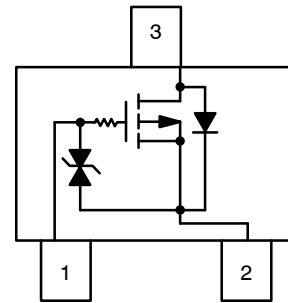
Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	-20	V
Gate-to-Source Voltage			V_{GS}	± 6	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D	-780	mA
		$T_A = 85^\circ\text{C}$		-570	
	$t \leq 5 \text{ s}$	$T_A = 25^\circ\text{C}$		-870	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	P_D	450	mW
	$t \leq 5 \text{ s}$			550	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	I_D	-660	mA
		$T_A = 85^\circ\text{C}$		-480	
Power Dissipation (Note 2)		$T_A = 25^\circ\text{C}$	P_D	310	mW
Pulsed Drain Current	$t_p = 10 \mu\text{s}$		I_{DM}	-1.2	A
Operating Junction and Storage Temperature			T_J, T_{STG}	-55 to 150	$^\circ\text{C}$
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
2. Surface mounted on FR4 board using the minimum recommended pad size

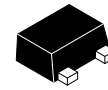
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D Max
-20 V	0.38 Ω @ -4.5 V	-780 mA
	0.52 Ω @ -2.5 V	-660 mA
	0.70 Ω @ -1.8 V	-100 mA
	0.95 Ω @ -1.5 V	-100 mA

SOT-723 (3-LEAD)



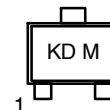
Top View

1 – Gate
2 – Source
3 – Drain



SOT-723
CASE 631AA
STYLE 5

MARKING DIAGRAM



KD = Specific Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
NTK3139PT1G	SOT-723 Pb-Free	4000 / Tape & Reel
NTK3139PT5G		8000 / Tape & Reel
NTK3139PT3G		40000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTK3139P

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	280	°C/W
Junction-to-Ambient – $t = 5$ s (Note 3)	$R_{\theta JA}$	228	
Junction-to-Ambient – Steady State Minimum Pad (Note 4)	$R_{\theta JA}$	400	

3. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
 4. Surface mounted on FR4 board using the minimum recommended pad size

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = -250$ μ A	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250$ μ A, Reference to 25°C		-16.5		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0$ V, $V_{DS} = -16$ V	$T_J = 25^\circ\text{C}$		-1.0	μ A
			$T_J = 125^\circ\text{C}$		-2.0	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 4.5$ V			± 2.0	μ A

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = -250$ μ A	-0.45		-1.2	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			2.4		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -4.5$ V, $I_D = -780$ mA		0.38	0.48	Ω
		$V_{GS} = -2.5$ V, $I_D = -660$ mA		0.52	0.67	
		$V_{GS} = -1.8$ V, $I_D = -100$ mA		0.70	0.95	
		$V_{GS} = -1.5$ V, $I_D = -100$ mA		0.95	2.20	
Forward Transconductance	g_{FS}	$V_{DS} = -10$ V, $I_D = -540$ mA		1.2		S
Gate Resistance	R_G	$T_A = 25^\circ\text{C}$		112		Ω

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0$ V, $f = 1$ MHz, $V_{DS} = -16$ V		113	170	μ F
Output Capacitance	C_{OSS}			15	25	
Reverse Transfer Capacitance	C_{RSS}			9.0	15	

SWITCHING CHARACTERISTICS, $V_{GS} = 4.5$ V (Note 6)

Turn On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5$ V, $V_{DS} = -10$ V, $I_D = -200$ mA, $R_G = 10$ Ω		9.0		ns
Rise Time	t_r			5.8		
TurnOff Delay Time	$t_{d(OFF)}$			32.7		
Fall Time	t_f			20.3		

DRAIN SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0$ V, $I_S = -350$ mA	$T_J = 25^\circ\text{C}$		-0.8	-1.2	V
Reverse Recovery Time	t_{RR}	$V_{GS} = 0$ V, $dI_{SD}/dt = 100$ A/ μ s, $I_S = -1.0$ A, $V_{DD} = -20$ V			13.2		ns
Charge Time	t_a				11.8		
Discharge Time	t_b				1.4		
Reverse Recovery Charge	Q_{RR}				5.0		

5. Pulse Test: pulse width = 300 μ s, duty cycle = 2%
 6. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

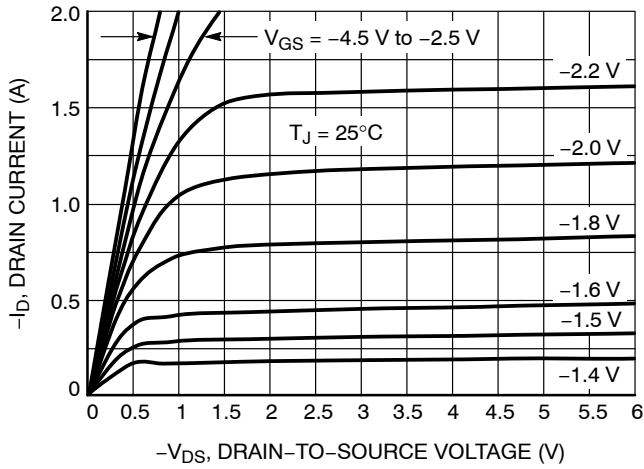


Figure 1. On-Region Characteristics

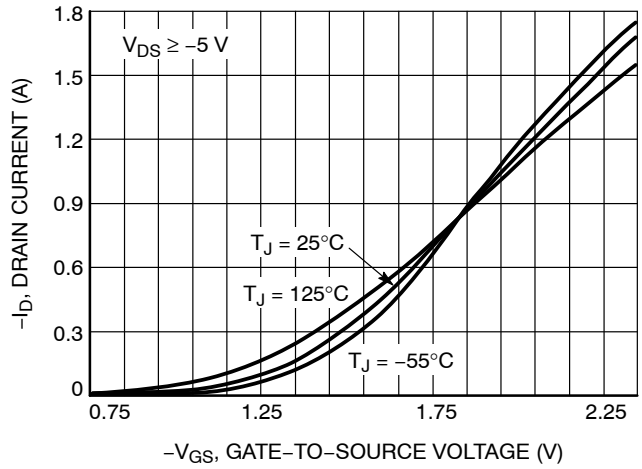


Figure 2. Transfer Characteristics

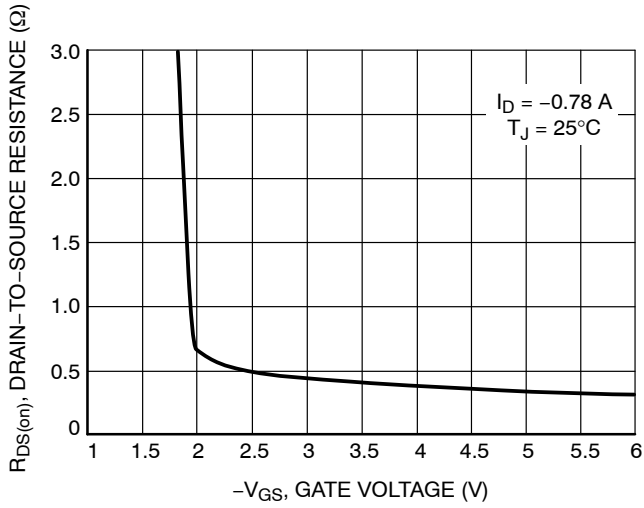


Figure 3. On-Resistance vs. Gate-to-Source Voltage

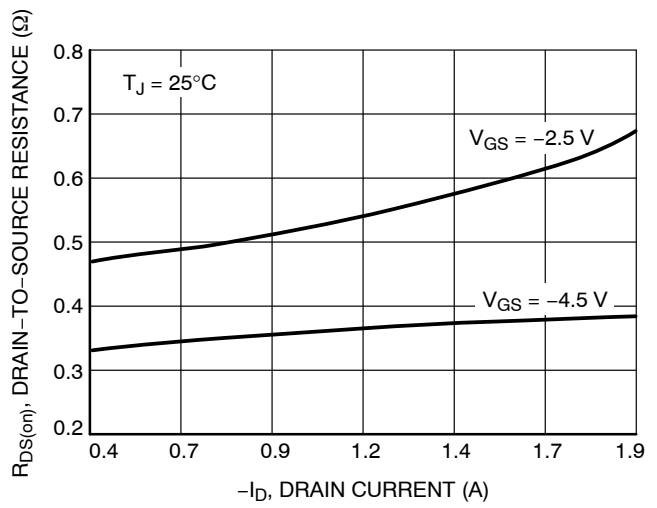


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

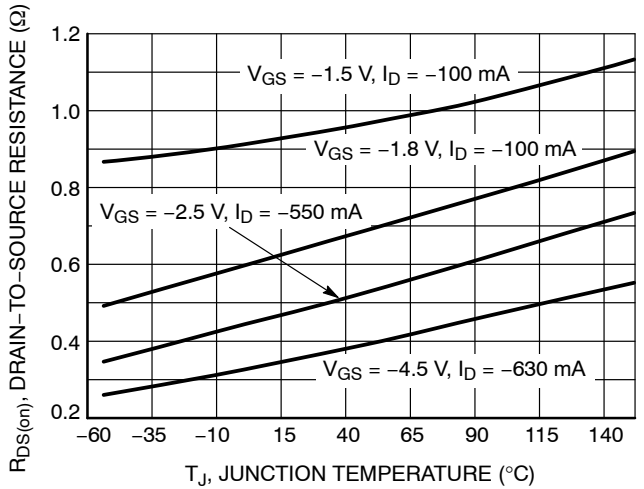


Figure 5. On-Resistance Variation with Temperature

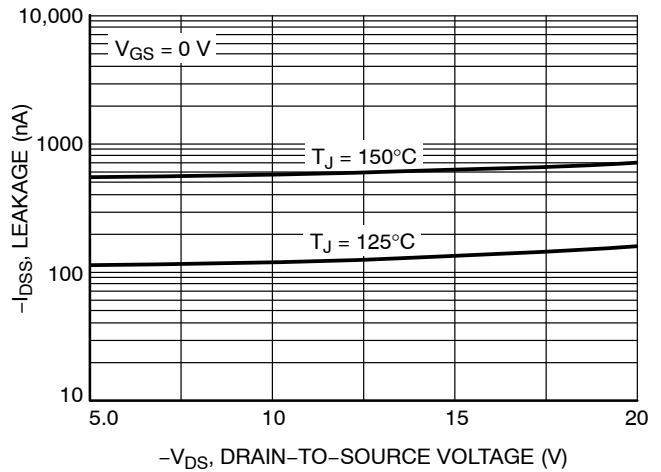


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

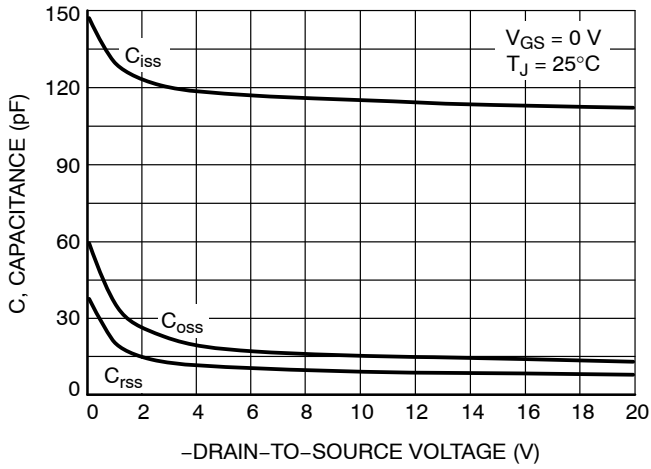


Figure 7. Capacitance Variation

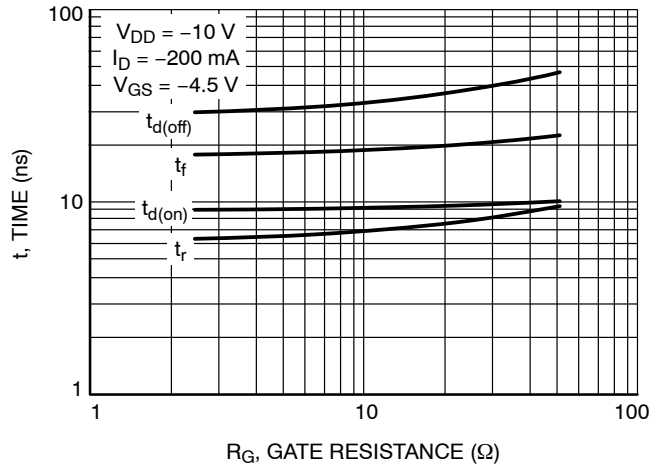


Figure 8. Resistive Switching Time Variation vs. Gate Resistance

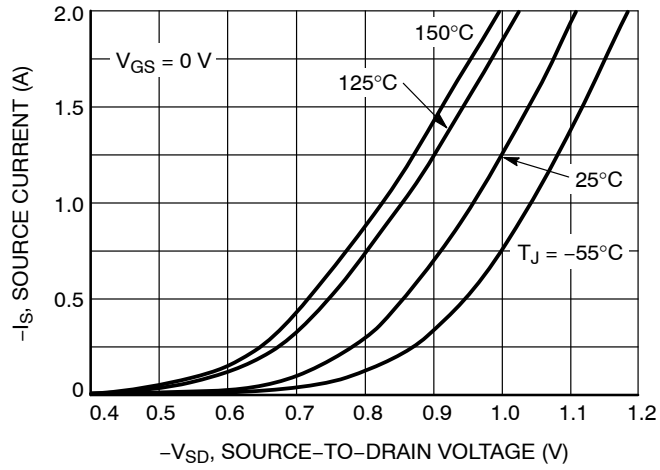


Figure 9. Diode Forward Voltage vs. Current

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



SOT-723 1.20x0.80x0.50, 0.40P
CASE 631AA
ISSUE E

DATE 24 JAN 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

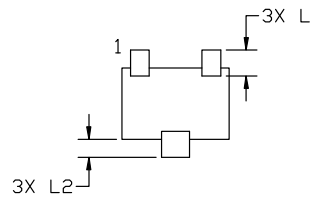
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.45	0.50	0.55
b	0.15	0.21	0.27
b1	0.25	0.31	0.37
c	0.07	0.12	0.17
D	1.15	1.20	1.25
E	0.75	0.80	0.85
e	0.40 BSC		
H	1.15	1.20	1.25
L	0.29 REF		
L2	0.15	0.20	0.25



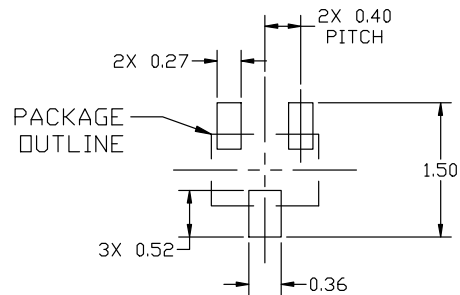
TOP VIEW



SIDE VIEW



BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLE 1:	STYLE 2:	STYLE 3:	STYLE 4:	STYLE 5:
PIN 1. BASE	PIN 1. ANODE	PIN 1. ANODE	PIN 1. CATHODE	PIN 1. GATE
2. EMITTER	2. N/C	2. ANODE	2. CATHODE	2. SOURCE
3. COLLECTOR	3. CATHODE	3. CATHODE	3. ANODE	3. DRAIN

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