# NTD4808N, NVD4808N

# MOSFET – Power, Single, N-Channel, DPAK/IPAK
## 30 V, 63 A

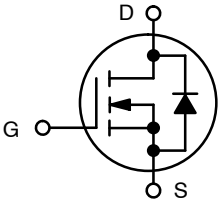
**ON Semiconductor®**

**http://onsemi.com**

| $V_{(BR)DSS}$ | $R_{DS(ON)}$ MAX | $I_D$ MAX |
|---|---|---|
| 30 V | 8.0 mΩ @ 10 V | 63 A |
| | 12.4 mΩ @ 4.5 V | |

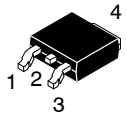
### Features
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These are Pb−Free Devices

### Applications
- CPU Power Delivery
- DC−DC Converters
- Low Side Switching

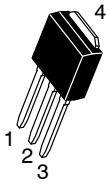



**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise stated)

| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | 30 | V |
| Gate−to−Source Voltage | | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current $R_{\theta JA}$ (Note 1) | Steady State | $T_A$ = 25°C | $I_D$ | 13.8 | A |
| | | $T_A$ = 85°C | | 10.7 | |
| Power Dissipation $R_{\theta JA}$ (Note 1) | | $T_A$ = 25°C | $P_D$ | 2.63 | W |
| Continuous Drain Current $R_{\theta JA}$ (Note 2) | | $T_A$ = 25°C | ID | 10 | A |
| | | $T_A$ = 85°C | | 7.8 | |
| Power Dissipation $R_{\theta JA}$ (Note 2) | | $T_A$ = 25°C | $P_D$ | 1.4 | W |
| Continuous Drain Current $R_{\theta JC}$ (Note 1) | | $T_C$ = 25°C | $I_D$ | 63 | A |
| | | $T_C$ = 85°C | | 49 | |
| Power Dissipation $R_{\theta JC}$ (Note 1) | | $T_C$ = 25°C | $P_D$ | 54.6 | W |
| Pulsed Drain Current | $t_p$=10μs | $T_A$ = 25°C | $I_{DM}$ | 126 | A |
| Current Limited by Package | | $T_A$ = 25°C | $I_{DmaxPkg}$ | 45 | A |
| Operating Junction and Storage Temperature | | | $T_J$, $T_{STG}$ | −55 to +175 | °C |
| Source Current (Body Diode) | | | $I_S$ | 45 | A |
| Drain to Source dV/dt | | | dV/dt | 6 | V/ns |

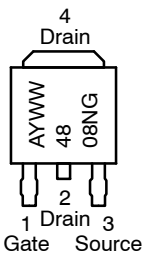


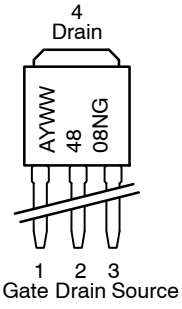

**DPAK**
**CASE 369AA**
**STYLE 2**




**IPAK**
**CASE 369D**
**STYLE 2**

### MARKING DIAGRAMS & PIN ASSIGNMENTS




A = Assembly Location*
Y = Year
WW = Work Week
4808N = Device Code
G = Pb−Free Package

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

### ORDERING INFORMATION
See detailed ordering and shipping information on page 6 of this data sheet.

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**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise stated)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Single Pulse Drain−to−Source Avalanche Energy ($V_{DD}$ = 24 V, $V_{GS}$ = 10 V, $I_L$ = 17 $A_{pk}$, L = 1.0 mH, $R_G$ = 25 Ω) | EAS | 144.5 | mJ |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | $T_L$ | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**THERMAL RESISTANCE MAXIMUM RATINGS**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Junction−to−Case (Drain) | $R_{\theta JC}$ | 2.75 | °C/W |
| Junction−to−TAB (Drain) | $R_{\theta JC-TAB}$ | 3.5 | |
| Junction−to−Ambient − Steady State (Note 1) | $R_{\theta JA}$ | 57 | |
| Junction−to−Ambient − Steady State (Note 2) | $R_{\theta JA}$ | 107 | |

1. Surface−mounted on FR4 board using 1 sq−in pad, 1 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise specified)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | | 30 | | | V |
| Drain−to−Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | | | | 27 | | mV/°C |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 24 V | $T_J$ = 25 °C | | | 1 | μA |
| | | | $T_J$ = 125°C | | | 10 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | | | | ±100 | nA |
| **ON CHARACTERISTICS** (Note 3) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | | 1.5 | | 2.5 | V |
| Negative Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | | | | 5.6 | | mV/°C |
| Drain−to−Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 to 11.5 V | $I_D$ = 30 A | | 6.7 | 8.0 | mΩ |
| | | | $I_D$ = 15 A | | 6.6 | | |
| | | $V_{GS}$ = 4.5 V | $I_D$ = 30 A | | 10.3 | 12.4 | |
| | | | $I_D$ = 15 A | | 9.8 | | |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ = 15 V, $I_D$ = 15 A | | | 11.4 | | S |
| **CHARGES AND CAPACITANCES** | | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{GS}$ = 0 V, f = 1 MHz, $V_{DS}$ = 12 V | | | 1538 | | pF |
| Output Capacitance | $C_{OSS}$ | | | | 334 | | |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | | 180 | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise specified) (continued)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **CHARGES AND CAPACITANCES** | | | | | | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 4.5 V, $V_{DS}$ = 15 V; $I_D$ = 30 A | | | 11.3 | 13 | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | | 1.6 | | |
| Gate−to−Source Charge | $Q_{GS}$ | | | | 4.9 | | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | | 4.9 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 11.5 V, $V_{DS}$ = 15 V; $I_D$ = 30 A | | | 26 | | nC |
| **SWITCHING CHARACTERISTICS** (Note 4) | | | | | | | |
| Turn−On Delay Time | $t_{d(ON)}$ | $V_{GS}$ = 4.5 V, $V_{DS}$ = 15 V, $I_D$ = 15 A, $R_G$ = 3.0 Ω | | | 12.3 | | ns |
| Rise Time | $t_r$ | | | | 21.3 | | |
| Turn−Off Delay Time | $t_{d(OFF)}$ | | | | 14.6 | | |
| Fall Time | $t_f$ | | | | 6.0 | | |
| Turn−On Delay Time | $t_{d(ON)}$ | $V_{GS}$ = 11.5 V, $V_{DS}$ = 15 V, $I_D$ = 15 A, $R_G$ = 3.0 Ω | | | 7.7 | | ns |
| Rise Time | $t_r$ | | | | 19.5 | | |
| Turn−Off Delay Time | $t_{d(OFF)}$ | | | | 23 | | |
| Fall Time | $t_f$ | | | | 3.5 | | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = 30 A | $T_J$ = 25°C | | 0.93 | 1.2 | V |
| | | | $T_J$ = 125°C | | 0.83 | | |
| Reverse Recovery Time | $t_{RR}$ | $V_{GS}$ = 0 V, $dI_S/dt$ = 100 A/μs, $I_S$ = 30 A | | | 20 | | ns |
| Charge Time | $t_a$ | | | | 10.4 | | |
| Discharge Time | $t_b$ | | | | 9.6 | | |
| Reverse Recovery Charge | $Q_{RR}$ | | | | 9.7 | | nC |
| **PACKAGE PARASITIC VALUES** | | | | | | | |
| Source Inductance | $L_S$ | $T_A$ = 25°C | | | 2.49 | | nH |
| Drain Inductance, DPAK | $L_D$ | | | | 0.0164 | | |
| Drain Inductance, IPAK | $L_D$ | | | | 1.88 | | |
| Gate Inductance | $L_G$ | | | | 3.46 | | |
| Gate Resistance | $R_G$ | | | | 1.1 | | Ω |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

## TYPICAL PERFORMANCE CURVES

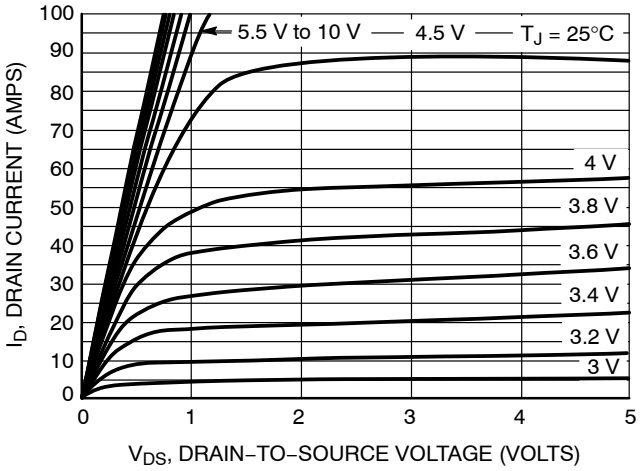



**Figure 1. On−Region Characteristics**

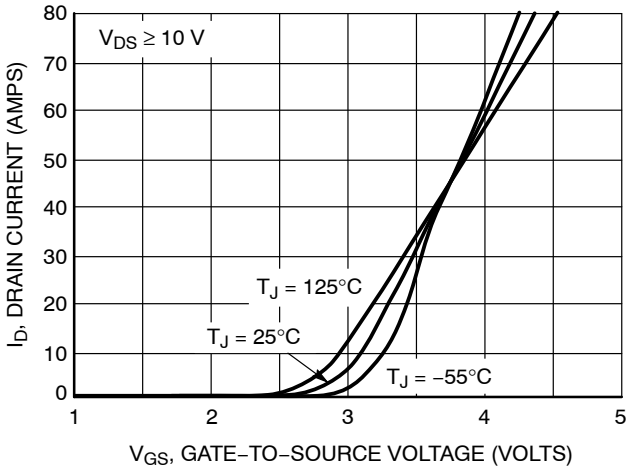



**Figure 2. Transfer Characteristics**

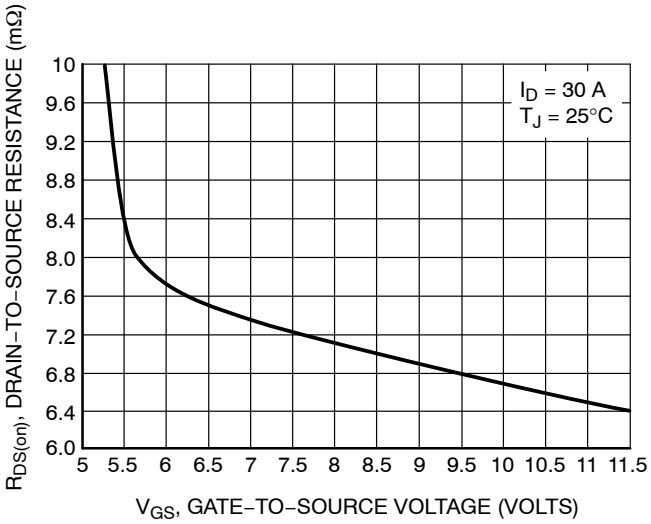



**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

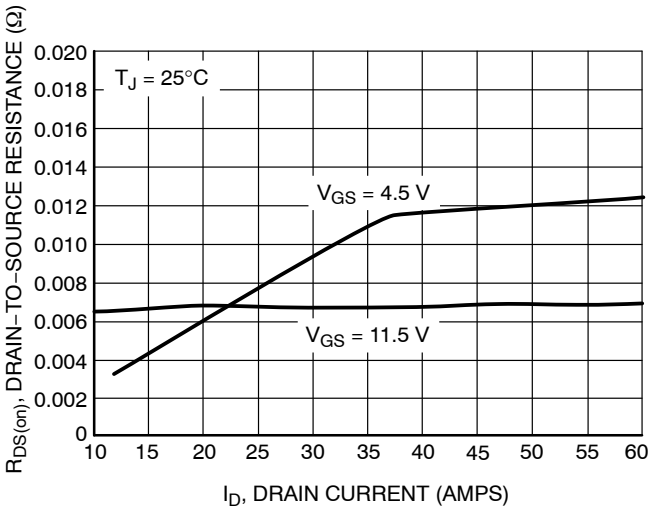



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

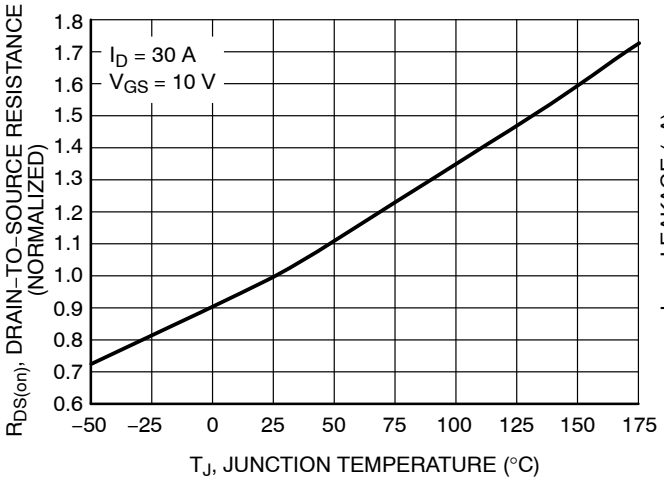



**Figure 5. On−Resistance Variation with Temperature**

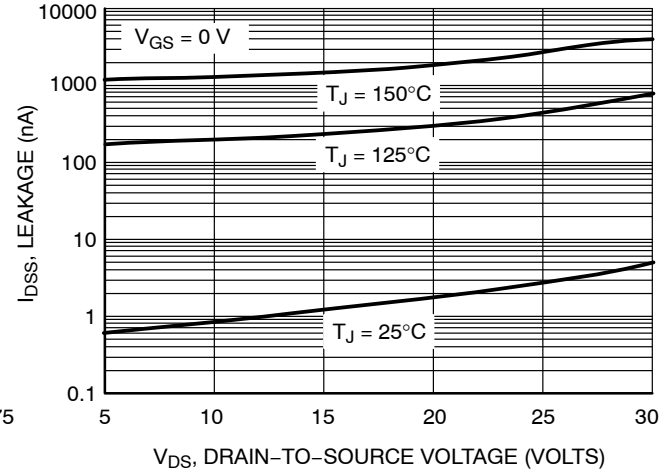



**Figure 6. Drain−to−Source Leakage Current vs. Drain Voltage**

## TYPICAL PERFORMANCE CURVES

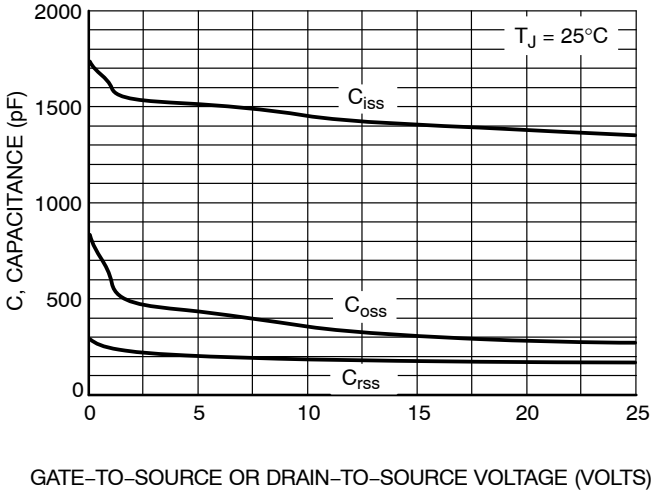



**Figure 7. Capacitance Variation**

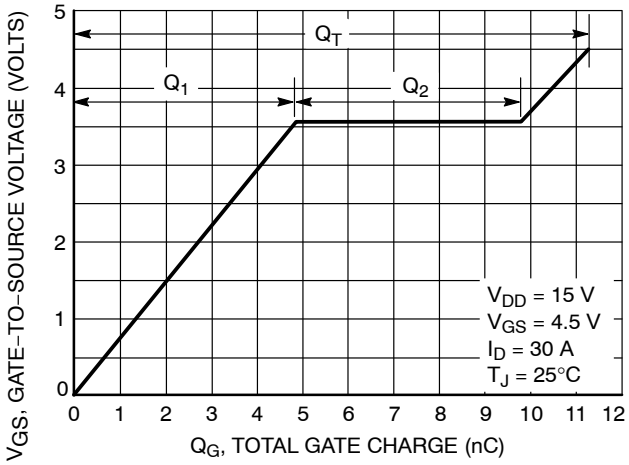



**Figure 8. Gate−To−Source and Drain−To−Source Voltage vs. Total Charge**

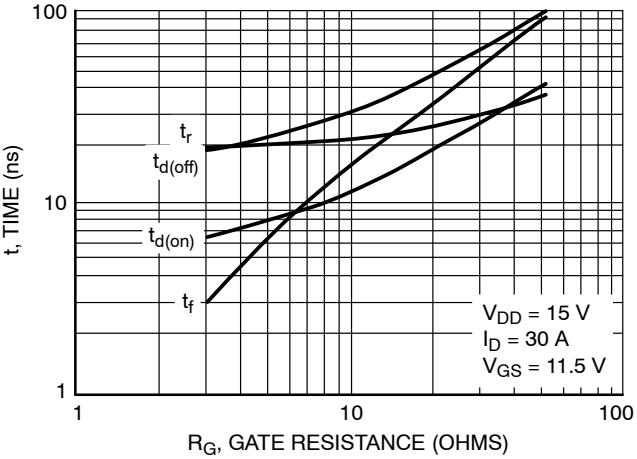



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

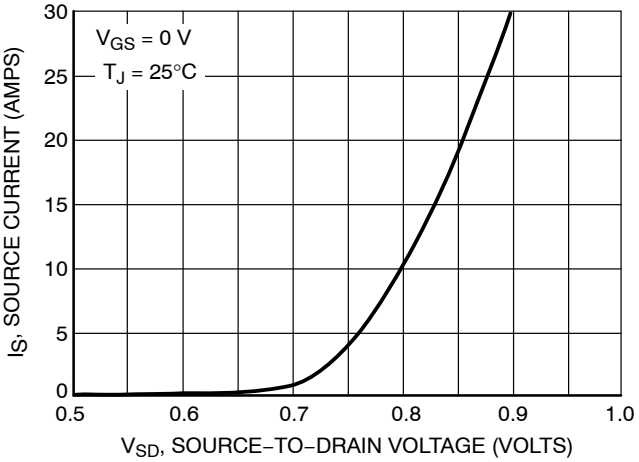



**Figure 10. Diode Forward Voltage vs. Current**

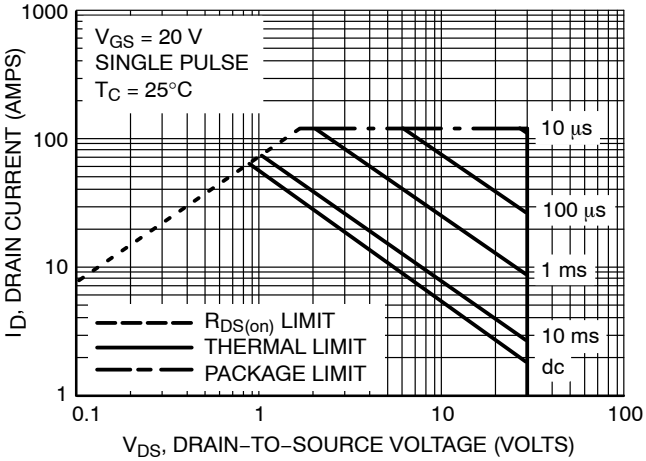



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

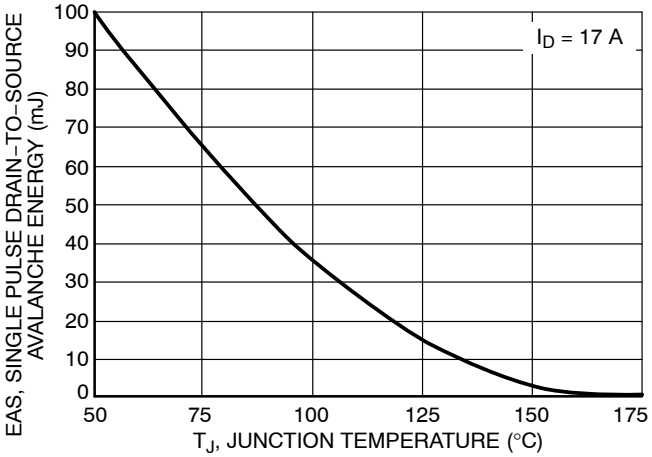



**Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature**

## TYPICAL PERFORMANCE CURVES

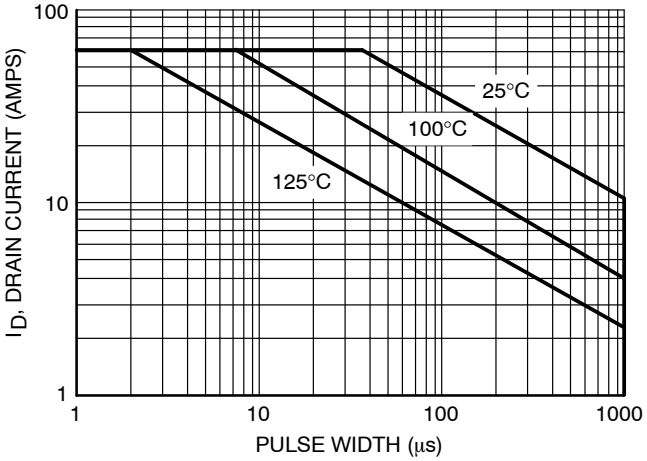



**Figure 13. Avalanche Characteristics**

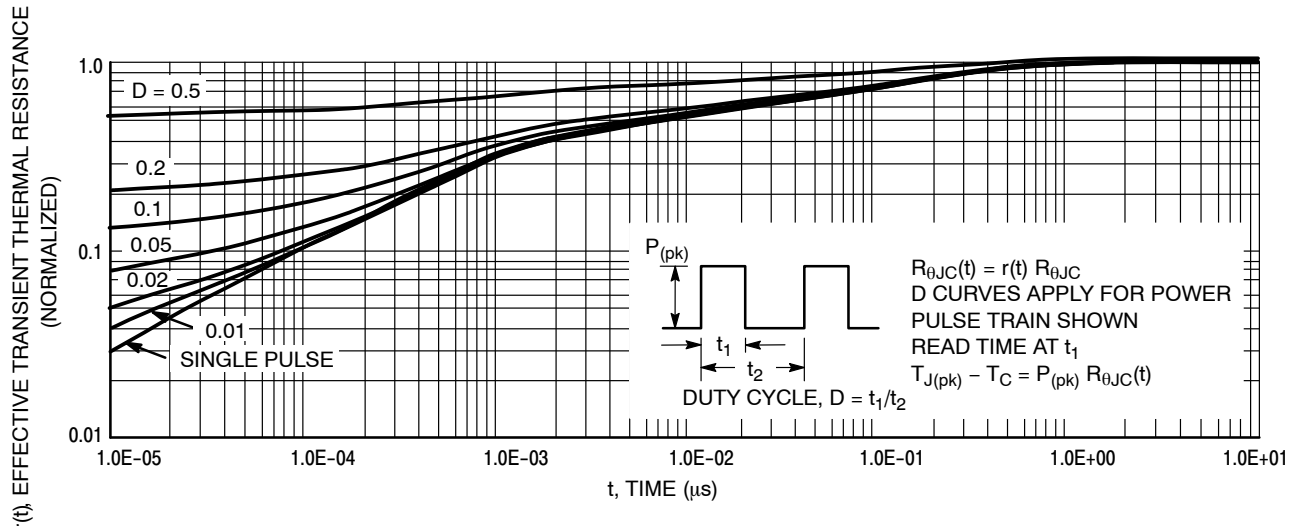



**Figure 14. Thermal Response**

### ORDERING INFORMATION

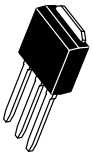
| Device | Package | Shipping† |
|---|---|---|
| NTD4808NT4G | DPAK (Pb−Free) | 2500 / Tape & Reel |
| NTD4808N−1G | IPAK (Pb−Free) | 75 Units / Rail |
| NVD4808NT4G* | DPAK (Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.

**IPAK**
CASE 369D–01
ISSUE C

DATE 15 DEC 2010



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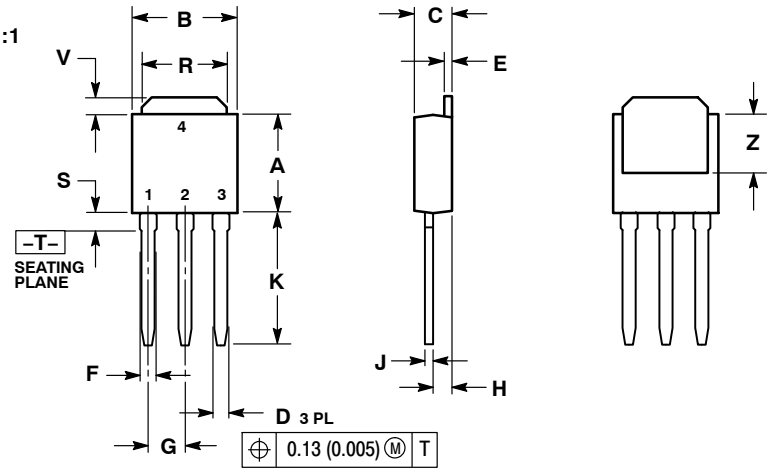



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.35 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.037 | 0.045 | 0.94 | 1.14 |
| G | 0.090 BSC | | 2.29 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.350 | 0.380 | 8.89 | 9.65 |
| R | 0.180 | 0.215 | 4.45 | 5.45 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | --- | 3.93 | --- |

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

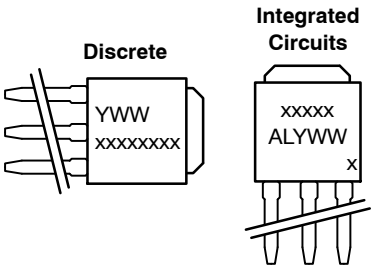
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

## MARKING DIAGRAMS




xxxxxxxxx = Device Code
A = Assembly Location
IL = Wafer Lot
Y = Year
WW = Work Week

| DOCUMENT NUMBER: | 98AON10528D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
|---|---|---|
| DESCRIPTION: | IPAK (DPAK INSERTION MOUNT) | PAGE 1 OF 1 |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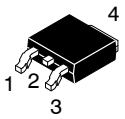
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

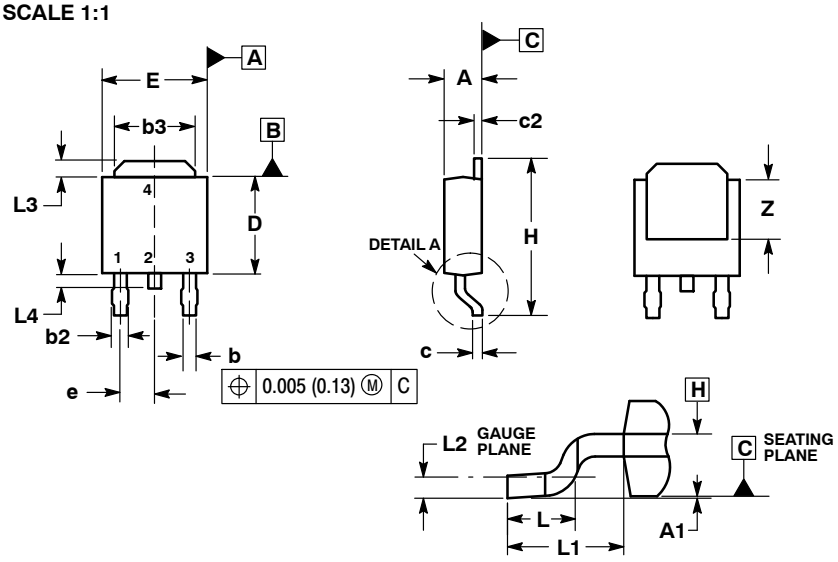
ON Semiconductor®




SCALE 1:1

**DPAK (SINGLE GUAGE)**
CASE 369AA−01
ISSUE B

DATE 03 JUN 2010




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.030 | 0.045 | 0.76 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 BSC | | 2.29 BSC | |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.108 REF | | 2.74 REF | |
| L2 | 0.020 BSC | | 0.51 BSC | |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | −−− | 0.040 | −−− | 1.01 |
| Z | 0.155 | −−− | 3.93 | −−− |

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

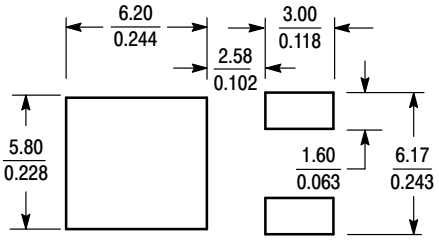
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

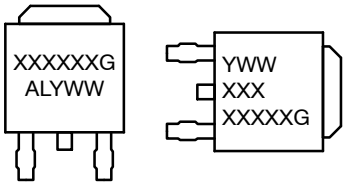
### SOLDERING FOOTPRINT*




SCALE 3:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




IC Discrete

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

| | | |
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