

N-Channel JFET

15 V, 10 to 32 mA, 35 mS

NSVJ3557SA3

Automotive JFET designed for compact and efficient designs and including high gain performance. AEC-Q101 qualified JFET and PPAP capable suitable for automotive applications.

Features

- Large |yfs|
- Small Ciss
- This Small Package Enables Sets to be Smaller and Thinner
- Ultralow Noise Figure
- This Device is Pb-Free and RoHS Compliant
- AEC-Q101 Qualified and PPAP Capable

Applications

- AM Tuner RF Amplification, Low Noise Amplifier
- Low Noise Amplifier

SPECIFICATIONS ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

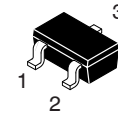
Symbol	Parameter	Value	Unit
V _{DSX}	Drain-to-Source Voltage	15	V
V _{GDS}	Gate-to-Drain Voltage	-15	V
I _G	Gate Current	10	mA
I _D	Drain Current	50	mA
P _D	Allowable Power Dissipation	200	mW
T _j , T _{stg}	Operating Junction and Storage Temperature	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V _{(BR)GDS}	Gate-to-Drain Breakdown Voltage	I _G = -10 μA, V _{DS} = 0 V	-15	-	-	V
I _{GSS}	Gate Cutoff Current	V _{GS} = -10 V, V _{DS} = 0 V	-	-	-1	nA
V _{GS(off)}	Cutoff Voltage	V _{DS} = 5 V, I _D = 100 μA	-0.3	-0.7	-1.5	V
I _{DSS}	Drain Current	V _{DS} = 5 V, V _{GS} = 0 V	10	-	32	mA
yfs	Forward Transfer Admittance	V _{DS} = 5 V, V _{GS} = 0 V, f = 1 kHz	24	35	-	mS
C _{iss}	Input Capacitance	V _{DS} = 5 V, V _{GS} = 0 V, f = 1 MHz	-	10	-	pF
C _{rss}	Reverse Transfer Capacitance		-	2.9	-	pF
NF	Noise Figure	V _{DS} = 5 V, R _g = 1 kΩ, I _D = 1 mA, f = 1 kHz	-	1	-	dB

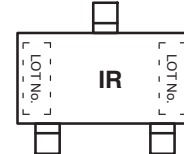
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



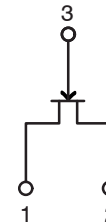
1: Source
2: Drain
3: Gate

SC-59 / CP3
CASE 318BJ

MARKING DIAGRAM



ELECTRICAL CONNECTION



1: Source
2: Drain
3: Gate

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

NSVJ3557SA3

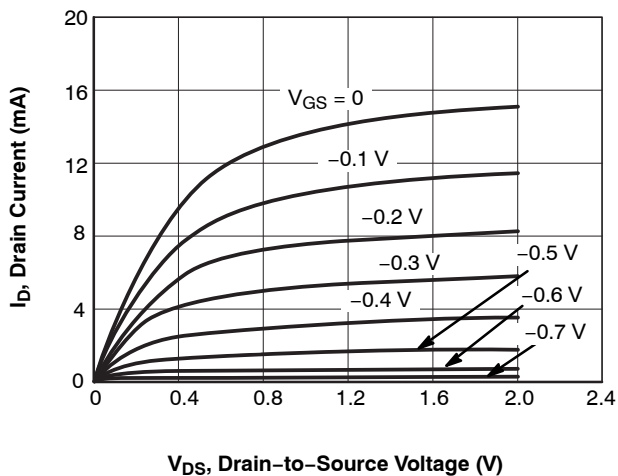


Figure 1. $I_D - V_{DS}$

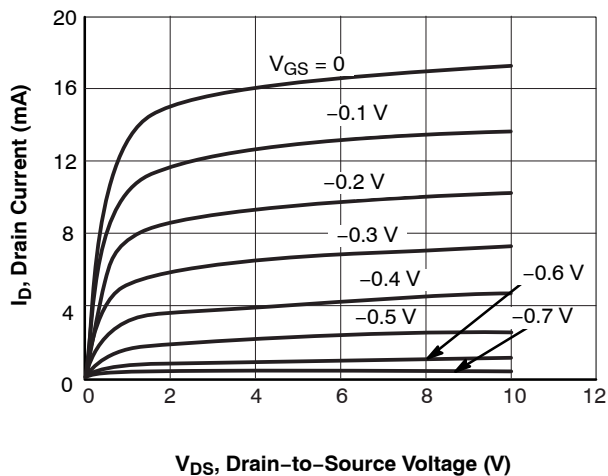


Figure 2. $I_D - V_{DS}$

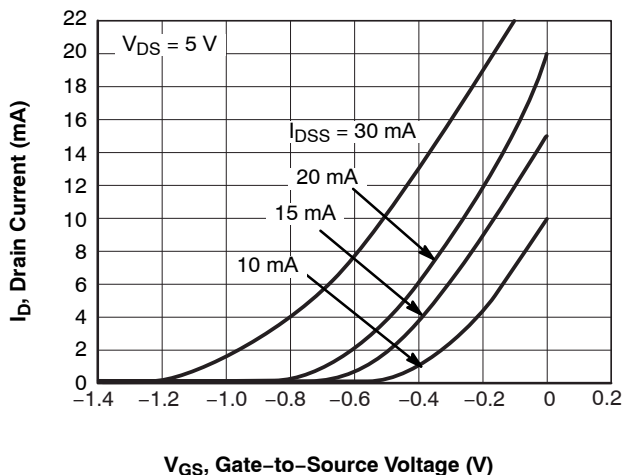


Figure 3. $I_D - V_{GS}$

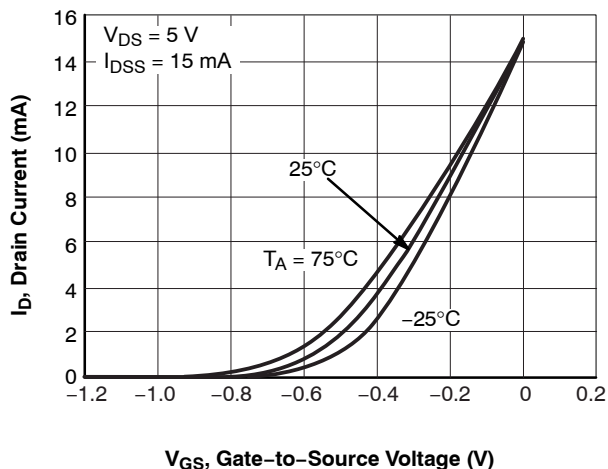


Figure 4. $I_D - V_{GS}$

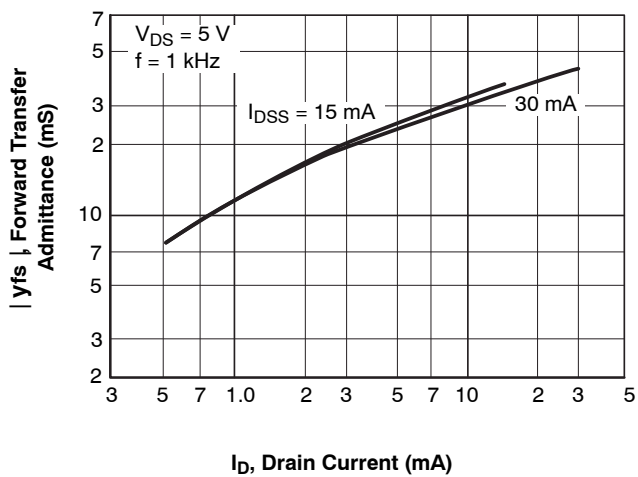


Figure 5. $|y_{fs}| - I_D$

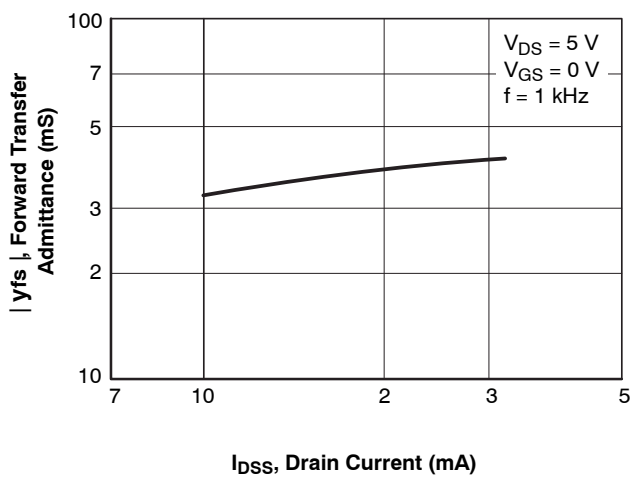


Figure 6. $|y_{fs}| - I_{DSS}$

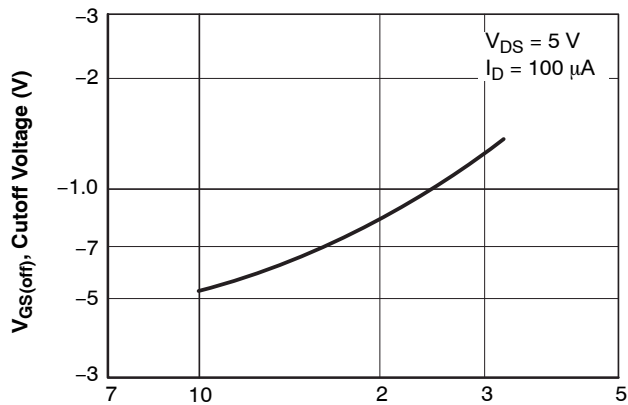


Figure 7. $V_{GS(off)}$ - I_{DSS}

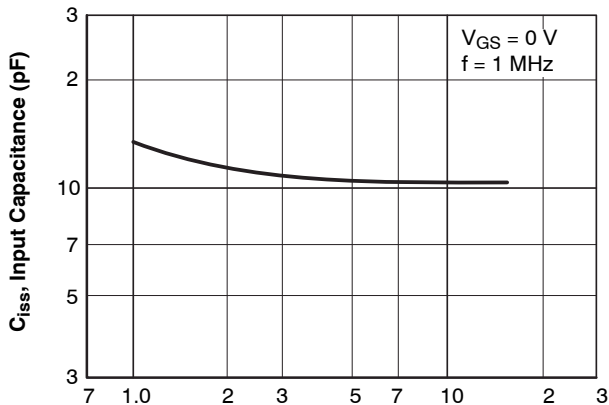


Figure 8. C_{iss} - V_{DS}

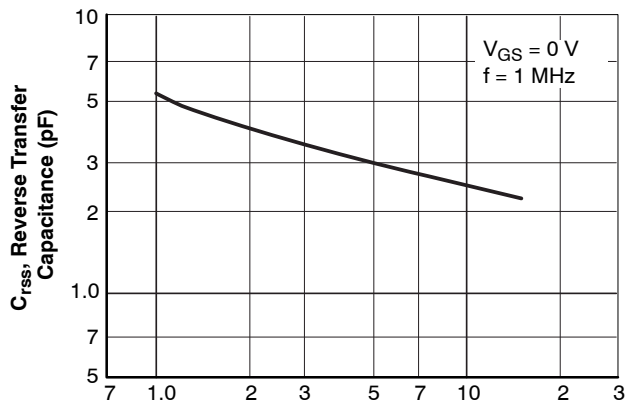


Figure 9. C_{rss} - V_{DS}

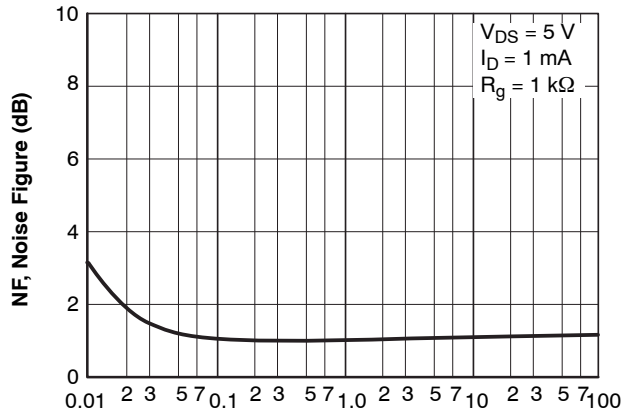


Figure 10. NF - f

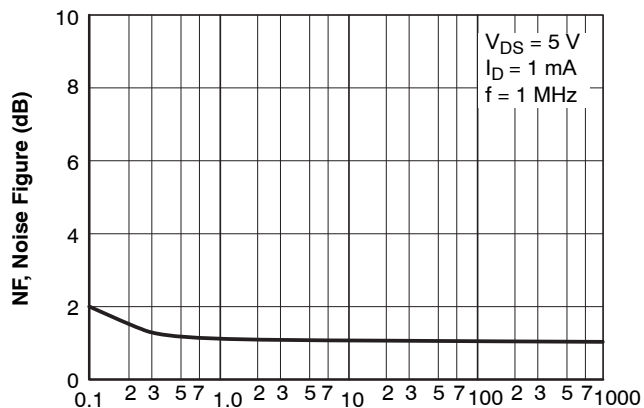


Figure 11. NF - R_g

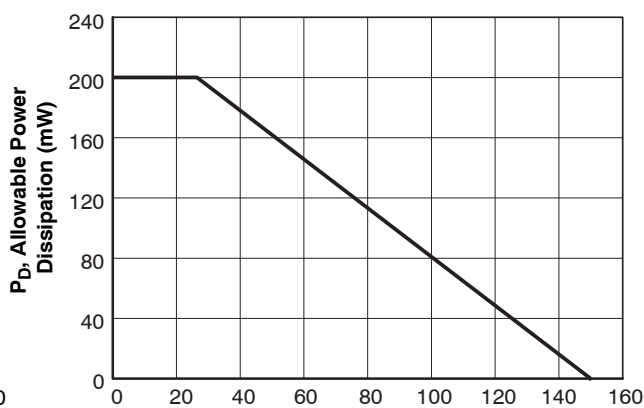


Figure 12. P_D - T_A

NSVJ3557SA3

ORDERING INFORMATION

Part Number	Marking	Package	Shipping†
NSVJ3557SA3T1G	IR	SC-59 3-Lead / CP3 (Pb-Free)	3,000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

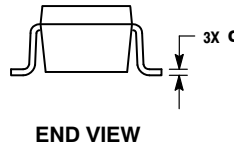
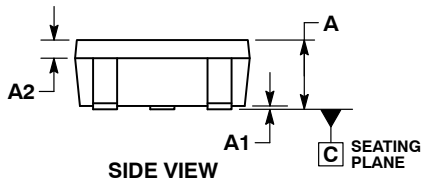
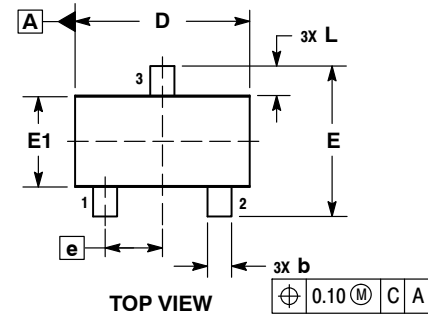
ON Semiconductor®



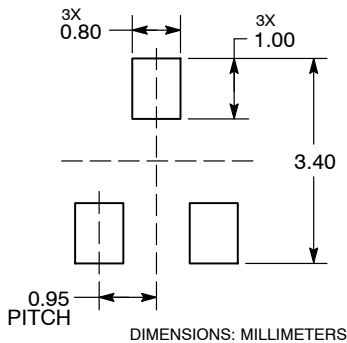
SCALE 2:1

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ISSUE O

DATE 09 JAN 2015



RECOMMENDED SOLDERING FOOTPRINT*

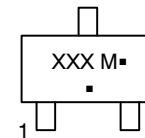


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER SIDE.
4. DIMENSIONS D AND E1 ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
5. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.20 FROM THE TIP.

MILLIMETERS		
DIM	MIN	MAX
A	0.95	1.35
A1	0.00	0.10
A2	0.20	0.40
b	0.35	0.50
c	0.10	0.20
D	2.75	3.05
E	2.30	2.70
E1	1.35	1.65
e	0.95 BSC	
L	0.35	0.75

GENERIC MARKING DIAGRAM



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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