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NOA1312

Product Preview

High-Precision Ambient Light Sensor with Three I²C Slave Addresses, EEPROM and Dark Current Compensation

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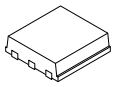
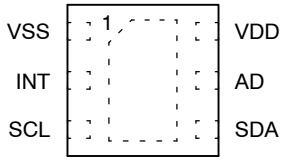


CUDFN6
CU SUFFIX
CASE 505AD

PIN ASSIGNMENT



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NOA1312CUTAG	CUDFN6 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Description

The NOA1312 high−precision ambient light sensor (ALS) is designed for very high accuracy (better than ±5% tolerance) handheld applications. The device integrates a 16−bit ADC, a 2−wire I²C digital interface with three pin−selectable I²C slave addresses, internal clock oscillator, EEPROM and a power down mode. A photopic optical color filter together with built in dynamic dark current compensation and precision calibration capability plus excellent IR and 50/60 Hz flicker rejection enables highly accurate measurements from very low light levels to full sunlight. The device can support simple count equals lux readings in interrupt−driven or polling modes. The NOA1312 employs proprietary CMOS image sensing technology from ON Semiconductor to provide large signal to noise ratio (SNR) and wide dynamic range (DR) over the entire operating temperature range.

Features

- Senses Ambient Light and Provides an Output Count Proportional to the Ambient Light Intensity
- Human Eye Spectral Response using Photopic Optical Filter
- Dynamic Dark Current Compensation
- Very High Accuracy (better than ±5% tolerance)
- Ev Sensitivity of 5.2 Counts/lux
- Three I²C Slave Addresses (0x29, 0x39 and 0x49), Pin Selectable
- Less than 240 μA Active Power Consumption in Normal Operation
- Ultra−low Quiescent Power Dissipation, less than 100 nA in Power Down Mode (below 50°C)
- Interrupt Signal Notifies Host of Significant Intensity Changes
- Internal EEPROM Stores Values to Minimize Programming Time
- Register Values Preserved during Power−down Mode
- Wide Operating Voltage Range (2.4 V to 3.6 V)
- Wide Operating Temperature Range (−40°C to 85°C)
- Linear Response over the Full Operating Range
- Senses Intensity of Ambient Light from 0.096 lux to Full Sunlight
- Programmable Integration Times
- No External Components Required
- Built−in 16−bit ADC
- I²C Serial Communication Port Supports Standard and Fast Modes
- This Device is Pb−Free, Halogen Free/BFR Free, and RoHS Compliant

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

Applications

- Saves Display Power in Applications such as:
  - Tablets, LED Backlit Displays, Smart Phones, Netbooks, PDAs, MP3 Players, GPS
  - Video Recorders

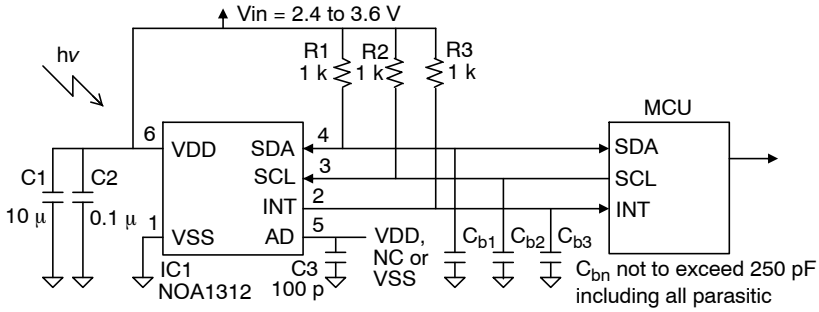


Figure 1. Typical Application Circuit

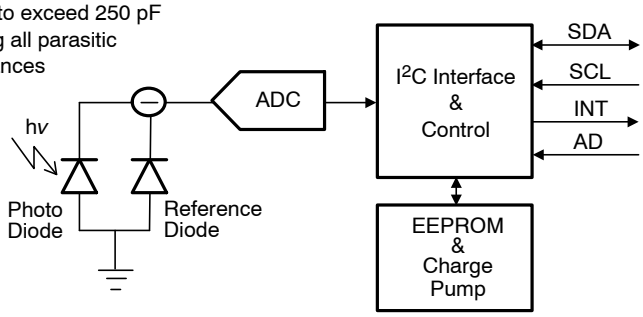


Figure 2. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin	Pin Name	Description
1	VSS	Ground pin.
2	INT	Interrupt request to the host. Active−low, open drain output and requires a 1 kΩ pull−up resistor.
3	SCL	External I²C clock provided by the I²C master. Requires a 1 kΩ pull−up resistor.
4	SDA	Bi−directional data signal for communication between this device and the I²C master. Requires a 1 kΩ pull−up resistor.
5	AD	I²C slave addresses select pin. Selects one of three I²C slave addresses (0x29, 0x39 or 0x49) depending on if this pin is connected to VDD, NC (open) or VSS at power up. This is not a programmable input, the connection should not be changed after power up.
6	VDD	Power pin.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input power supply	VDD	4.0	V
Input voltage range	V_{in}	−0.2 to VDD + 0.2	V
Output voltage range	V_{out}	−0.2 to VDD + 0.2	V
Digital output current	I_o	−10 to 10	mA
Operating Free−Air Temperature Range	T_A	−40 to 85	°C
Storage Temperature	T_{STG}	−45 to 85	°C
ESD Capability, Human Body Model (Note 1)	ESD_{HBM}	2,000	V
ESD Capability, Charged Device Model (Note 1)	ESD_{CDM}	750 (corner pins), 500 (center pins)	V
ESD Capability, Machine Model (Note 1)	ESD_{MM}	200	V
Moisture Sensitivity Level	MSL	5	−
Lead Temperature Soldering (Note 2)	T_{SLD}	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114
   ESD Charged Device Model tested per ESD−STM5.3.1−1999
   ESD Machine Model tested per EIA/JESD22−A115
   Latchup Current Maximum Rating: ≤ 100 mA per JEDEC standard: JESD78
2. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 3. OPERATING RANGES

Rating	Symbol	Min	Typ	Max	Unit
Power supply voltage	VDD	2.4	3.0	3.6	V
Power supply current	IDD		140	240	μA
Quiescent supply current (Note 3)	IDD_{qs}		12	800	nA
Low level input voltage	V_{IL}	−0.2		0.3 VDD	V
High level input voltage (Note 4)	V_{IH}	0.7 VDD		VDD + 0.2	V
Hysteresis of SCL & SDA Schmitt trigger inputs (VDD > 2 V)	V_{hys}	0.05 VDD			V
Low level output voltage (open drain) at 3 mA sink current (SDA, INT)	V_{OL}	0		0.4	V
Output low current (SDA, INT)	I_{OL}	3		–	mA
Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance, C_b from 10 pF to 250 pF (Note 4)	t_{of}	–	–	250	ns
Input current of IO pin with an input voltage between 0.1 VDD and 0.9 VDD	I_I	−10		10	μA
Capacitance for IO pin (Note 4)	C_b			10	pF
Operating free−air temperature range	T_A	−40		85	°C

3. Current dissipation when in Power Down mode. 800 nA power down current at 85°C (see Figure 14).
4. Cb = capacitance of one bus line, maximum value including all parasitic capacitances should be less than 250 pF.

Table 4. ELECTRICAL CHARACTERISTICS
(Unless otherwise specified, these specifications apply over 2.4 V < VDD < 3.6 V, −40°C < T_A < 85°C, 10 pF < Cb < 100 pF) (Note 5)

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	10	100	100	400	kHz
Hold time after repeated start condition. After this period, the first clock pulse is generated.	$t_{HD;STA}$	4.0	–	0.6	–	μS
Low period of SCL clock	t_{LOW}	4.7		1.3		μS
High period of SCL clock	t_{HIGH}	4.0		0.6		μS
Set−up time for repeated START condition	t_{SUSTA}	4.7	–	0.6	–	μS
SDA Data hold time	t_{HDDAT}	0	3.45	0	0.9	μS
SDA Data set−up time	t_{SUDAT}	250	–	100	–	nS
Rise time of both SDA and SCL (input signals) (Note 6)	t_r	5	1000	20 + 0.1C_b	300	nS
Fall time of both SDA and SCL (input signals) (Note 6)	t_f	5	300	20 + 0.1C_b	300	nS
Set−up time for STOP condition	t_{SUSTO}	4.0	–	0.6	–	μS
Bus free time between STOP and START condition	t_{BUF}	4.7	–	1.3	–	μS
Capacitive load for each bus line	C_b	–	250	–	250	pF
Noise margin at the low level for each connected device (including hysteresis)	V_{nL}	0.1 VDD	–	0.1 VDD	–	V
Noise margin at the high level for each connected device (including hysteresis)	V_{nH}	0.2 VDD	–	0.2 VDD	–	V
Parameter	**Symbol**	**Typ**		**Typ**		**Unit**
Internal Oscillator Frequency	f_{osc}	1		1		MHz

5. Refer to Figure 3 for more information on AC characteristics
6. The rise time and fall time are measured with a pull−up resistor R_p = 1 kΩ and C_b of 250 pF (including all parasitic capacitances). The maximum t_f for the SDA and SCL bus lines (300 ns) is longer than the specified maximum t_{of} for the output stages (250 ns). This allows series protection resistors (Rs) to be connected between the SDA/SCL pads and the SDA/SCL bus lines without exceeding the maximum specified t_f.

Table 5. OPTICAL CHARACTERISTICS (Unless otherwise specified, these specifications are for VDD = 3.0 V, T_A = 25°C)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Irradiance responsivity	λp (see Figure 4)	R_e		550		nm
Trimmed response	White LED light source, Ev = 100 lux, Tint = 200 ms (see Figure 7)	R_{v_trim}	494	520	546	Counts
Dark response	Ev = 0 lux, Tint = 400 ms, VDD = 2.4 to 3.6 V,−40°C to 85°C	R_{v_dark}		0	1	Counts
Illuminance responsivity	White LED light source, Ev = 12,603 lux, Tint = 200 ms (see Figure 5, Figure 6, Note 7)	R_{v_max}			65,535	Counts
Counts vs Vdd	Ev = 100 lux, Tint = 200 ms, VDD = 2.4 to 3.6 V, relative to VDD = 3.0 V	dC/dVDD	−5		5	%
Counts vs Temperature (−40°C to 0°C)	Ev = 100 lux, Tint = 200 ms, VDD = 3.0 V, −40°C to 0°C, relative to room temperature (25°C)	dC/dT_{low}	−20		20	%
Counts vs Temperature (0°C to 85°C)	Ev = 100 lux, Tint = 200 ms, VDD = 3.0 V, 0°C to 85°C, relative to room temperature (25°C)	dC/dT_{high}	−5		5	%
Linearity (Low Ev)	White LED light source, Ev = 0 − 15 lux, Tint = 200 ms	L_{low}	(5.2*Ev)−5		(5.2*Ev)+2	Counts
Linearity (High Ev)	White LED light source, Ev = 15 − 16,250 lux, Tint = 200 ms (Note 8)	L_{high}	−5		3.5	%
Count stability	Ev = 100 lux, Tint = 200 ms, VDD = 3.0 V (Note 9)	dC/dt	−1		1	%
Trimming range	Ev = 100 lux, Tint = 200 ms, −37% to +65%, VDD = 2.4 to 3.6 V, −40°C to 85°C (Note 10)	$TRIM_{range}$	315		825	Counts

7. The maximum count that can be accumulated in a 16−bit register is 65,535.
8. Linearity (high Ev) is estimated using the following formula:
   Linearity (High Ev) = ((Counts(n) − Ideal_counts(n))/ Ideal_counts(n)))* 100
   where:
   n is an Ev value between 0 lux and 16,250 lux
   Ideal_counts (at any Ev): 5.2 counts/lux (Tint = 200 ms)
   Linearity values shown above after the final trimming.
9. Count stability is measured over a duration of 5 minutes using a stable white LED at Ev = 100 lux, VDD = 3.0 V, T_A = 25°C
10. Output counts prior to trimming: low counts = 520/1.65, high counts = 520/0.63.

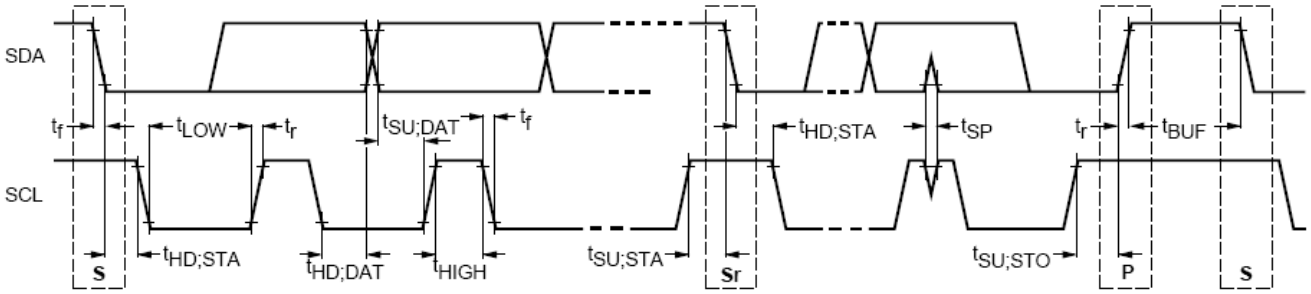


Figure 3. AC Characteristics

TYPICAL CHARACTERISTICS

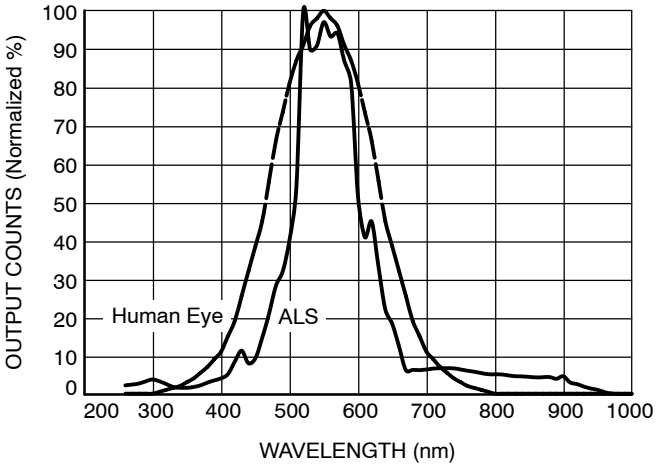


Figure 4. Spectral Response (Normalized)

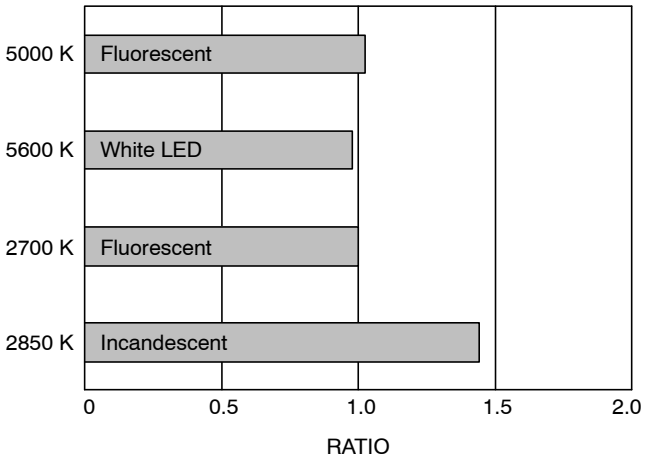


Figure 5. Light Source Dependency (Normalized to Fluorescent Light, Tint = 200 ms)

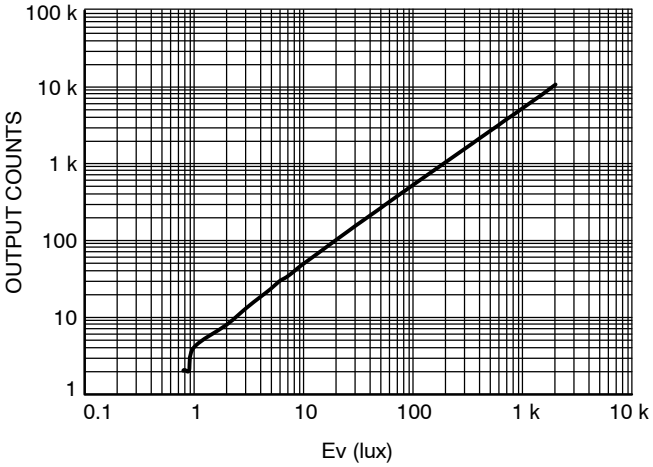


Figure 6. Output Counts vs. Ev, 0−2000 lux (Tint = 200 ms)

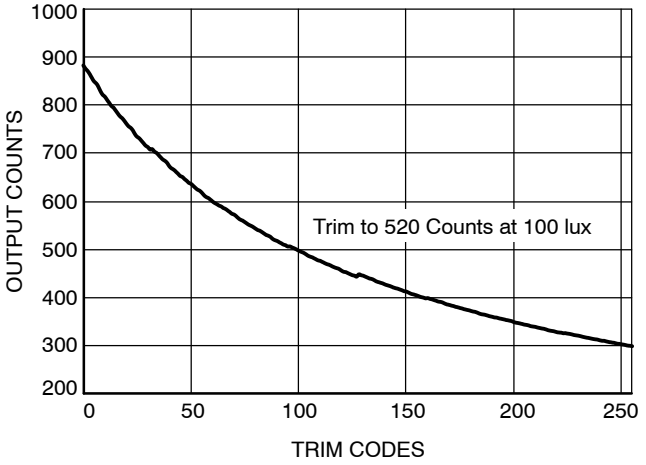


Figure 7. Output Counts and Trim Codes (100 lux, VDD = 3.0 V, Tint = 200 ms)

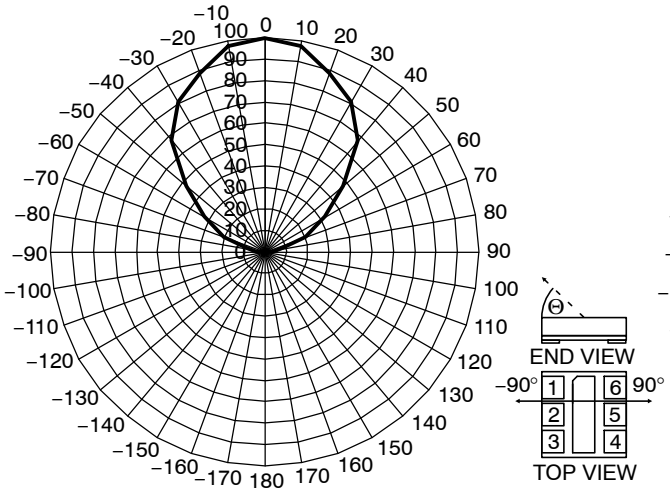


Figure 8. Output Counts vs. Angle (End View, Normalized)

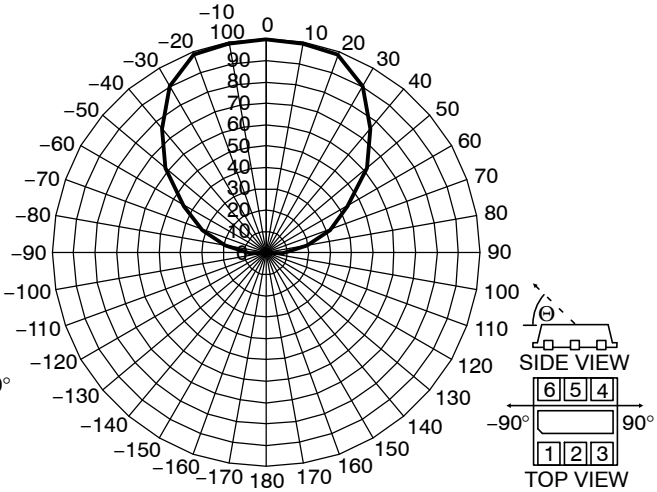


Figure 9. Output Counts vs. Angle (Side View, Normalized)

TYPICAL CHARACTERISTICS

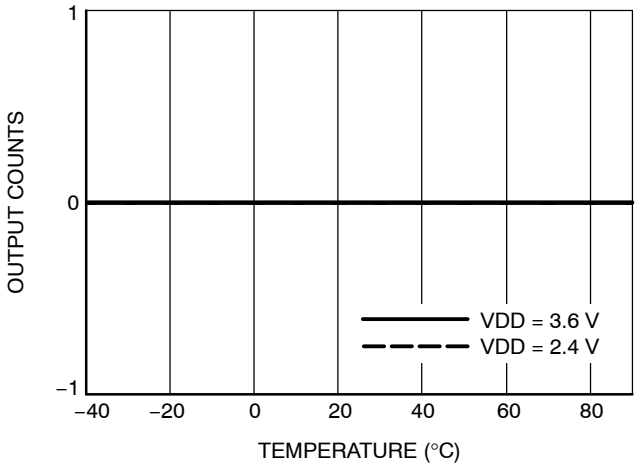


Figure 10. Output Counts at 0 lux vs. Temperature (Tint = 400 ms)

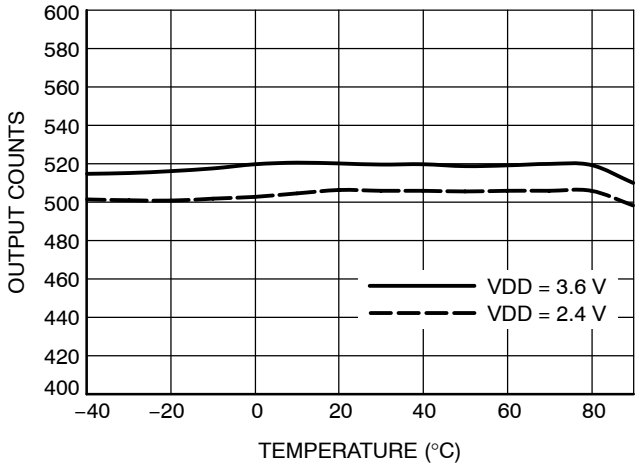


Figure 11. Output Counts at 100 lux vs. Temperature (Tint = 200 ms)

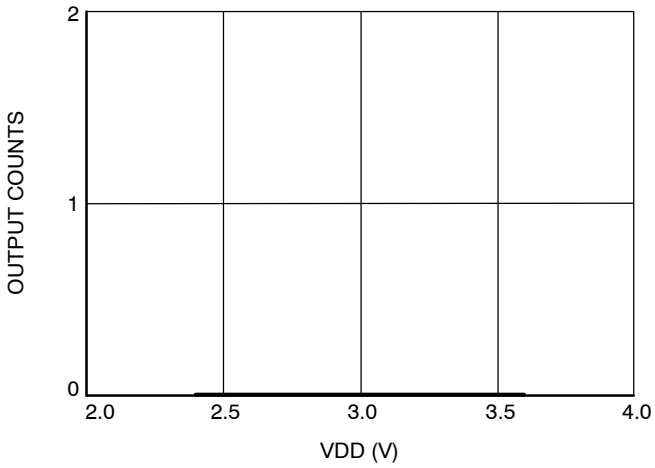


Figure 12. Output Counts at 0 lux vs. Supply Voltage (Tint = 400 ms)

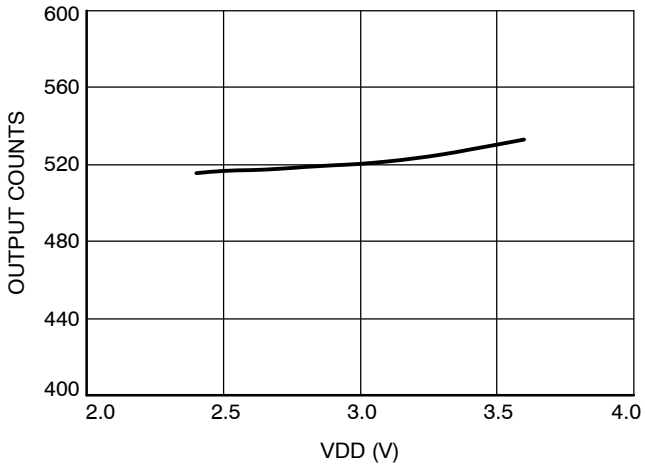


Figure 13. Output Counts at 100 lux vs. Supply Voltage (Tint = 200 ms)

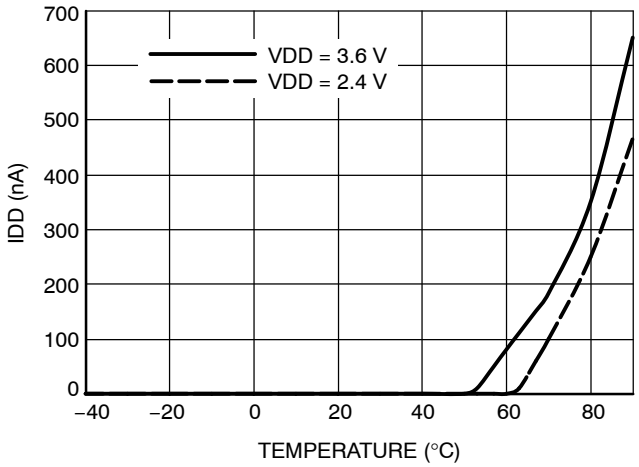


Figure 14. Supply Current in Power Down Mode vs. Temperature (100 lux, Tint = 200 ms)

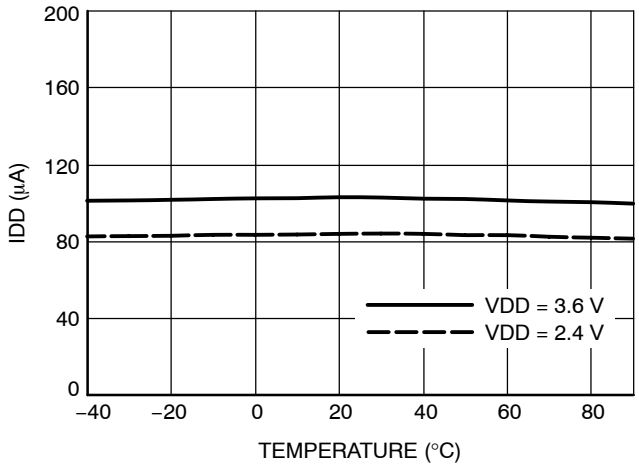


Figure 15. Supply Current vs. Temperature (100 lux, Tint = 200 ms)

TYPICAL CHARACTERISTICS

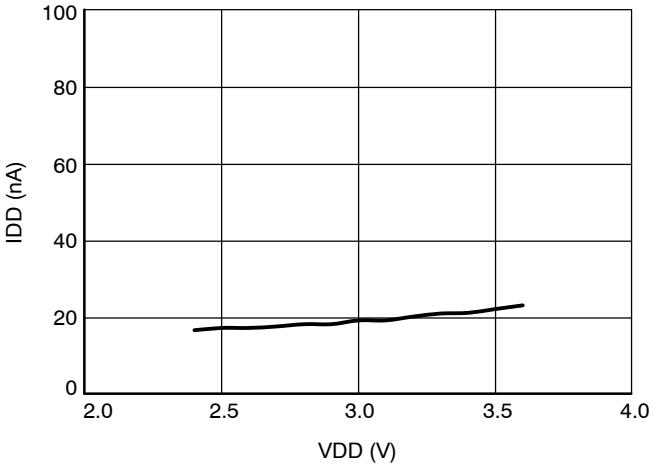


Figure 16. Supply Current in Power Down Mode vs. Supply Voltage (100 lux, Tint = 200 ms)

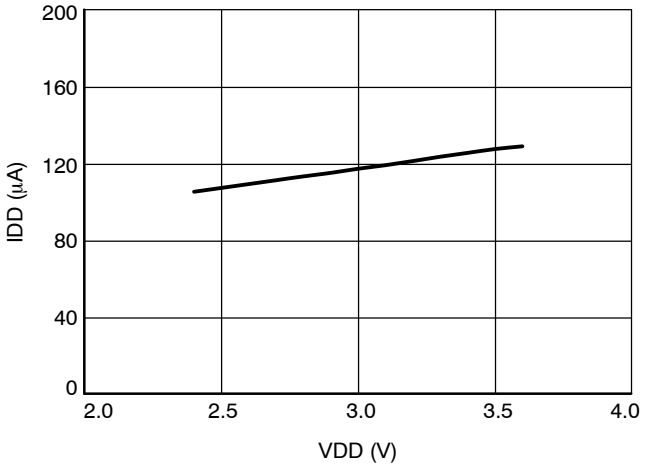
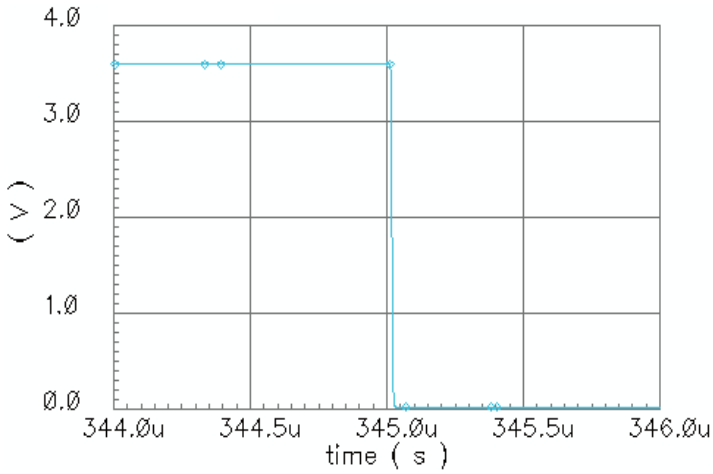


Figure 17. Supply Current vs. Supply Voltage (100 lux, Tint = 200 ms)



C_L = 250 pF (including all parasitic capacitances)
Rp = 1 K
Fall time t_f = 36 ns

Figure 18. SDA and INT Fall Time (t_f)

DESCRIPTION OF OPERATION

Ambient Light Sensor Architecture

The NOA1312 employs a sensitive photo diode fabricated in ON Semiconductor's standard CMOS process technology. The major components of this sensor are as shown Figure 2. The photons which are to be detected pass through the photopic filter limiting extraneous photons and thus performing as a band pass filter on the incident wave front. The filter only transmits photons in the visible spectrum which are primarily detected by the human eye and exhibits excellent IR rejection. The photo response of this sensor is as shown in Figure 4.

The ambient light signal detected by the photo diode is converted to digital signal using a variable slope integrating ADC with a resolution of 16−bits, unsigned. The ADC value is stored in the ALS_DATA register where it can be read by the I^2C interface.

Sensor Accuracy Trim

Highly accurate ambient light intensity reading can be obtained from the NOA1312 by following a simple trimming procedure which stores the trim value in the EEPROM memory. This not only enables more accurate readings, but also provides a way to match readings between devices. Matching to better than 2% is achievable when devices share a common power supply and thermal environment.

The NOA1312 uses a type of binary weighted trim code approach which allows the output count to be calibrated to a known light intensity. The factory default code stored in the EEPROM is shown in Table 8. Figure 7 shows the trimming of the output counts when Ev = 100 lux. The trimming operation is performed by writing an 8−bit code in the range of 0 to 255 (0x00 to 0xFF) to the EEPROM OUTPUT_TRIM register 0x16. Changes to the trim register are reflected in real time on the output value of the device.

As indicated in Table 5, the trimming range is from 315 (when trim code is 0xFF) to 825 (when trim code is 0x00). One possible trimming algorithm is to perform a binary search starting with trim code 0x00, refining the search to find a trim code providing 520 counts at Ev=100 lux within the desired accuracy.

Modes of Operation

The NOA1312 can be placed in any of the following modes of operation by programming registers over the I^2C bus:

1. Interrupt driven mode
2. Polling mode
3. Power−down mode

In the interrupt driven mode, once the NOA1312 is configured, no I^2C activity is necessary until the ambient light intensity goes above the value programmed in the interrupt threshold register (see INT_SELECT register 0x03 for details). When this occurs, the device signals an interrupt on the INT pin. Then it is up to the I^2C master host to read the ALS_DATA count from the device.

In polling mode, interrupts are typically disabled, but the NOA1312 continuously takes measurements and the I^2C master host reads out the most recent count whenever it desires to do so, typically in a timed repeat loop.

In power−down mode, the NOA1312 stops taking ambient light measurements and powers down most of the internal circuitry and the INT pin is deactivated. Power is maintained to preserve the register values (static memory) and a portion of the I^2C remains active to monitor for a power−on command to the NOA1312.

I^2C Interface

The NOA1312 acts as an I^2C slave device and supports single register read and write operations, in addition to block read and block write operations. All data transactions on the bus are 8−bits long. Each data byte transmitted is followed by an acknowledge bit. Data is transmitted with the MSB first.

The I^2C bus address of this device can be 0x29, 0x39 or 0x49, depending on the state of AD pin. When AD is connected to VDD, the address is 0x29. When AD is not connected (floating), the address is 0x39. When AD is connected to VSS, the address is 0x49. The AD connection must not be changed after power is applied to the device.

Figure 19 shows an I^2C write operation. Write transactions begin with the master sending an I^2C start sequence followed by the seven bit slave address (e.g. 0x29) and the write(0) command bit. The NOA1312 will acknowledge this byte transfer with an appropriate ACK. Next the master will send the 8−bit register address to be written to. Again the NOA1312 will acknowledge reception with an ACK. Finally, the master will begin sending 8−bit data segment(s) to be written to the NOA1312 register bank. The NOA1312 will send an ACK after each byte and increment the address pointer by one in preparation for the next transfer. Write transactions are terminated with either an I^2C STOP or with another I^2C START (repeated START).

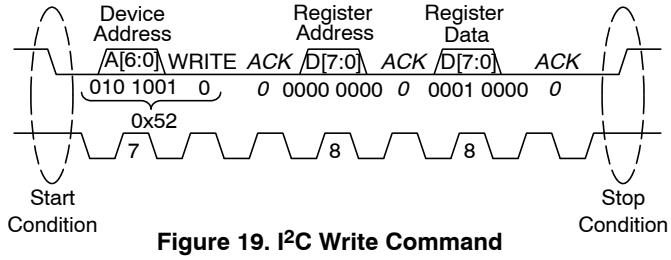
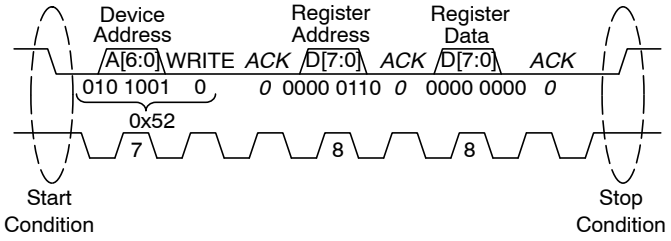


Figure 19. I²C Write Command



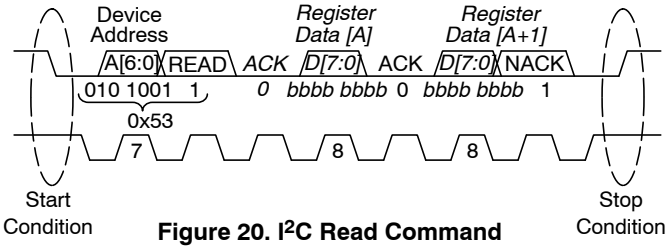


Figure 20. I²C Read Command

Figure 20 shows the most basic I²C read command sequence sent by the master to the slave device. The sequence consists of a complete I²C write command which sets the address pointer in preparation for the I²C read command since the read command itself does not include a register address. When reading from a read only data register in the NOA1312 it is acceptable to write a 0 to the register in order to update the address pointer, but the 0 does not actually over−write the value in the data register.

Once the I²C write command is completed, the master sends an I²C start sequence followed by the seven bit slave address (e.g. 0x29) and the read(1) command bit. The NOA1312 will acknowledge this byte transfer with an appropriate ACK. The NOA1312 will then begin shifting out data from the register just addressed. If the master wishes to receive more data (next register address), it will ACK the slave at the end of the 8−bit data transmission, and the slave will respond by sending the next byte, and so on. To signal the end of the read transaction, the master will send a NACK bit at the end of a transmission followed by an I²C STOP.

Rise and Fall Time of SDA (Output)

Proper operation of the I²C bus depends on keeping the bus capacitance low and selecting suitable pull−up resistor values. Figure 18 shows the fall time on SDA in output mode under maximum load conditions. The measurement set−up is shown in Figure 21.

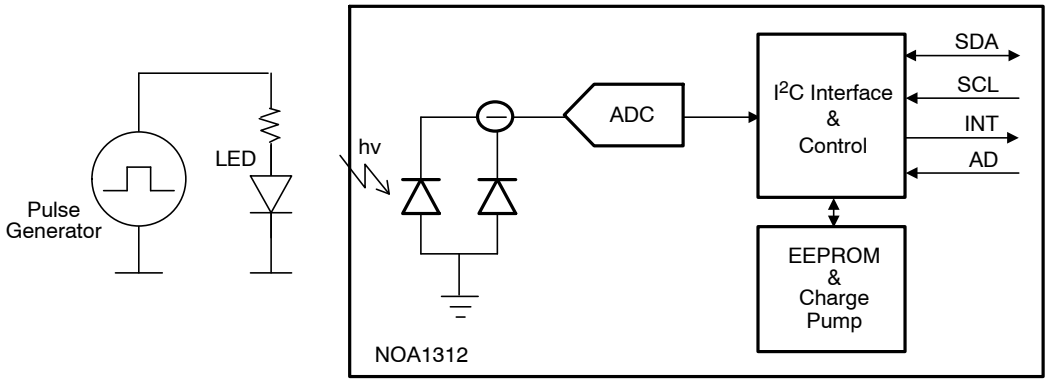


Figure 21. Measurement Set−up

NOA1312 I²C Slave Address

The NOA1312 I²C address is selected by connecting the AD pin as shown in Table 6.

Table 6. I²C SLAVE ADDRESS TABLE

AD Pin	I²C Slave Address
VDD	0x29
NC (not connected)	0x39
VSS	0x49

The AD pin is not programmable. The connection to AD should be stable before applying power to the device. The device sets the I²C slave address when power is applied. For the case where the AD pin is not connected, adding a small 100 pF decoupling capacitor is recommended to provide a stable state.

Should it be necessary, the address can be changed by following this procedure:

1. Disconnect power from the device
2. Change the AD connection to the desired level as shown in Table 6.
3. Reconnect power to the device.

Once power is applied to this device, any change in the connection to the AD pin may cause unpredictable results.

NOA1312 Data Registers

NOA1312 operation is observed and controlled by internal data registers read from and written to via the external I²C interface. Registers are listed in Table 7. Default values are set on initial power up.

Table 7. NOA1312 DATA REGISTERS

Register Address	Register	Type	Value (binary)	Description	EEPROM Address	Default (binary)
0x00	POWER_CONTROL	RW	0000 0000	Power Down	0x10	0000 0000
			0001 0000	Power On		
0x01	RESET	RW	0011 0000	Reset ALS data to 0x0000	0x11	0000 0000
0x02	INTEGRATION_TIME	RW	1001 0000	400 ms continuous measurement	0x12	1001 0001
			1001 0001	200 ms continuous measurement		
			1010 0000	100 ms continuous measurement		
			1010 0001	50 ms continuous measurement		
			1011 0000	20 ms continuous measurement		
			1011 0001	2 ms continuous measurement		
0x03	INT_SELECT	RW	0000 0001	L → H	0x13	0000 0011
			0000 0010	H → L		
			0000 0011	Inactive (H Keeper)		
0x04	INT_THRESH_LSB	RW	XXXX XXXX	Interrupt threshold, least significant bits	0x14	0000 0000
0x05	INT_THRESH_MSB	RW	XXXX XXXX	Interrupt threshold, most significant bits	0x15	0000 1000
0x06	ALS_DATA_LSB	R	XXXX XXXX	ALS measurement data, least significant bits	–	0000 0000
0x07	ALS_DATA_MSB	R	XXXX XXXX	ALS measurement data, most significant bits	–	0000 0000
0x08	DEVICE_ID_LSB	R	XXXX XXXX	Device ID value, least significant	0x18	0000 0000
0x09	DEVICE _ID_MSB	R	XXXX XXXX	Device ID value, most significant bits	0x19	0000 0000
0x0A	EEPROM_RDWR_ REG_ADDRESS	RW	XXXX XXXX	Address of EEPROM register to be read or written to (see Table 8)	–	0000 0000
0x0B	EEPROM _CONTROL_ STATUS	RW	XXXX XXXX	EEPROM read/write operation control (see Table 10)	–	0000 0000
0x10 to 0x19	Memory Mapped EEPROM Registers			EEPROM registers (see Table 8)		

POWER_CONTROL Register (0x00)

The POWER_CONTROL register is used to power the device up and down via software control. By default this device powers up in the power down mode. To reduce power consumption, the NOA1312 can be powered down at any time by writing 0x00 to this register.

To power up the device, use the following write command sequence:

1. Issue Start command
2. Issue 0x52 (lower seven bits of I^2C slave address 0x29 followed by write−bit 0) – the write address could be 0x52 (0x29), 0x72 (0x39) or 0x92 (0x49)
3. Issue 0x00 for the POWER_CONTROL register address
4. Issue 0x10 to put the device in the power on state
5. Issue Stop command

After applying power to the device or after issuing a power−on command, stable ALS_DATA and INT signal may not be available for the first three integration times. For example with a default of 200 ms integration time, the I^2C master should wait at least 600 ms before accessing this device.

To power down the device, use the following write command sequence:

1. Issue Start command
2. Issue 0x52 (lower seven bits of I^2C slave address 0x29 followed by write−bit 0) – the write address could be 0x52 (0x29), 0x72 (0x39) or 0x92 (0x49)
3. Issue 0x00 for the POWER_CONTROL register address
4. Issue 0x00 to put the device in the power down state
5. Issue Stop command

After issuing a power−down command, the I^2C master should wait at least 1.5 ms before accessing this device.

The data registers are set to the values stored in the EEPROM when power is first applied to the device. However the power−down and power−on commands do not affect the values of the data registers.

RESET Register (0x01)

Software reset is controlled by this register. Setting this register followed by an I2C_STOP sequence will immediately reset the NOA1312 to the startup standby state and clear the ALS_DATA register. However the values of the other data registers are not affected.

To reset the device, use the following write command sequence:

1. Issue Start command
2. Issue 0x52 (lower seven bits of I^2C slave address 0x29 followed by write−bit 0) – the write address could be 0x52 (0x29), 0x72 (0x39) or 0x92 (0x49)
3. Issue 0x01 for the RESET register address
4. Issue 0x30 to reset the device
5. Issue Stop command

After issuing a reset command, the device will reset the RESET register to 0x00.

INTEGRATION_TIME Register (0x02)

The INTEGRATION_TIME register controls the integration time of the ambient light sensor which directly affects the sensitivity.

To set the integration time, use the following write command sequence:

1. Issue Start command
2. Issue 0x52 (lower seven bits of I^2C slave address 0x29 followed by write−bit 0) – the write address could be 0x52 (0x29), 0x72 (0x39) or 0x92 (0x49)
3. Issue 0x02 for the INTEGRATION_TIME register address
4. Issue 0x91 to set the integration time to 200 ms (for example)
5. Issue Stop command

INT_SELECT Register (0x03)

The INT_SELECT register controls the polarity of the interrupt pin INT and enables or disables interrupts on that pin.

To specify low to high transitions on INT to signal an interrupt, use the following write command sequence:

1. Issue Start command
2. Issue 0x52 (lower seven bits of I^2C slave address 0x29 followed by write−bit 0) – the write address could be 0x52 (0x29), 0x72 (0x39) or 0x92 (0x49)
3. Issue 0x03 for the INT_SELECT register address
4. Issue 0x01 to specify low to high signaling on INT
5. Issue Stop command

To specify high to low transitions on INT to signal an interrupt, use the following write command sequence:

1. Issue Start command
2. Issue 0x52 (lower seven bits of I^2C slave address 0x29 followed by write−bit 0) – the write address could be 0x52 (0x29), 0x72 (0x39) or 0x92 (0x49)
3. Issue 0x03 for the INT_SELECT register address
4. Issue 0x02 to specify high to low signaling on INT
5. Issue Stop command

Disabling interrupts causes the INT pin to be held in the open−drain or high state. To disable interrupts on the INT pin, use the following write command sequence:

1. Issue Start command
2. Issue 0x52 (lower seven bits of I^2C slave address 0x29 followed by write−bit 0) – the write address could be 0x52 (0x29), 0x72 (0x39) or 0x92 (0x49)
3. Issue 0x03 for the INT_SELECT register address
4. Issue 0x03 to disable interrupts on INT
5. Issue Stop command

INT_THRESH_LSB and INT_THRES_MSB Registers (0x04, 0x05)

The INT_THRESH register specifies an ambient light threshold value for signaling interrupts on the INT pin. The INT_THRESH register is 16−bits wide to match the 16−bit ALS_DATA register and is accessed over the I^2C bus as two 8−bit registers for the least and most significant bits (LSB and MSB). On any measurement cycle where the

ALS_DATA intensity count exceeds the INT_THRESH value, the INT pin will become active and will remain active until a measurement cycle where the count is less than or equal to the threshold (and provided the INT pin is enabled, see INT_SELECT register).

Changing the INT_THRESH register value can cause the INT pin to change immediately if the ALS_DATA to INT_THRESH comparison changes.

Powering down the device will cause the INT pin to become inactive.

To program a value into the INT_THRESH register, use the following write command sequence:

1. Issue Start command
2. Issue 0x52 (lower seven bits of I^2C slave address 0x29 followed by write−bit 0) – the write address could be 0x52 (0x29), 0x72 (0x39) or 0x92 (0x49)
3. Issue 0x04 for the INT_THRES_LSB register address
4. Issue the 8−bit LSB value
5. Issue Stop command
6. Issue Start command
7. Issue 0x52 (lower seven bits of I^2C slave address 0x29 followed by write−bit 0) – the write address could be 0x52 (0x29), 0x72 (0x39) or 0x92 (0x49)
8. Issue 0x05 for the INT_THRES_MSB register address
9. Issue the 8−bit MSB value
10. Issue Stop command

ALS_DATA_LSB and ALS_DATA_MSB Registers (0x06, 0x07)

The ALS_DATA register holds the ambient light intensity count from the most recent measurement. The ALS_DATA register is 16−bits wide and is accessed from the I^2C bus as two 8−bit registers for the least and most significant bits (LSB and MSB).

To read the ALS_DATA register, use the following read command sequence:

1. Issue Start command
2. Issue 0x52 (lower seven bits of I^2C slave address 0x29 followed by write−bit 0) – the write address could be 0x52 (0x29), 0x72 (0x39) or 0x92 (0x49)
3. Issue 0x06 for the INT_DATA_LSB register address
4. Issue Start command
5. Issue 0x53 (lower seven bits of I^2C slave address 0x29 followed by read−bit 1) – the read address could be 0x53 (0x29), 0x73 (0x39) or 0x93 (0x49)
6. Read the ALS_DATA_LSB byte
7. Read the ALS_DATA_MSB byte
8. Issue Stop command

After a power−down and power−on sequence, wait at least three integration times for the data to stabilize, before accessing any ALS_DATA values from NOA1312.

DEVICE_ID_LSB and DEVICE_ID_MSB Registers (0x08, 0x09)

The DEVICE_ID registers hold the ID number for this device. This ID number could be changed at any time by writing appropriate ID number to the EEPROM registers 0x18 and 0x19. The DEVICE_ID register is 16−bits wide and is accessed from the I^2C bus as two 8−bit registers for the least and most significant bits (LSB and MSB).

To read the DEVICE_ID register, use the following read command sequence:

1. Issue Start command
2. Issue 0x52 (lower seven bits of I^2C slave address 0x29 followed by write−bit 0) – the write address could be 0x52 (0x29), 0x72 (0x39) or 0x92 (0x49)
3. Issue 0x08 for the DEVICE_ID_LSB register address
4. Issue Start command
5. Issue 0x53 (lower seven bits of I^2C slave address 0x29 followed by read−bit 1) – the read address could be 0x53 (0x29), 0x73 (0x39) or 0x93 (0x49)
6. Read the DEVICE_ID_LSB byte
7. Read the DEVICE_ID_MSB byte
8. Issue Stop command

NOA1312 EEPROM Registers

The EEPROM registers are listed in Table 8. The defaults values are set at the factory and will retain their values until modified by the user. They retain their values even when the device is not powered.

Table 8. EEPROM REGISTERS

EEPROM Address	Register	Type	Factory Default Value (binary)
0x10	POWER_CONTROL	RW	0000 0000
0x11	RESET_ALS_DATA	RW	0000 0000
0x12	INTEGRATION_TIME	RW	1001 0001
0x13	INT_SELECT	RW	0000 0011
0x14	INT_THRESH_LSB	RW	0000 0000
0x15	INT_THRESH_MSB	RW	0000 1000
0x16	OUTPUT_TRIM	RW	0101 1101
0x17	For future use	RW	XXXX XXXX
0x18	DEVICE_ID_LSB	RW	0000 0000
0x19	DEVICE_ID_MSB	RW	0000 0000

EEPROM_RDWR_REG_ADDRESS Register (0x0A)

The EEPROM_RDWR_REG_ADDRESS register specifies the address of an EEPROM register to be read or written to and is used in conjunction with the EEPROM_CONTROL_STATAUS register (0x0B) to effect read and write operations with the EEPROM.

The EEPROM enables the NOA1312 to retain register values even when fully powered down, facilitating a quick and simple power on sequence. Table 8 shows the EEPROM registers and their values as shipped from the factory. During power up, the values in the EEPROM registers are automatically transferred to the I^2C registers as specified in Table 9. EEPROM register values are not automatically updated during power down and must be explicitly updated with a write operation as described below.

EEPROM register address 0x16 contains an 8−bit OUTPUT_TRIM value. Writing to the OUTPUT_TRIM register will change the output count value in real time.

EEPROM register address 0x17 is reserved for future use.

Table 9. NOA1312 Data Registers Stored in EEPROM

I^2C Register Address	EEPROM Register Address	Register Name
0x00	0x10	POWER_CONTROL
0x01	0x11	RESET_ALS_DATA
0x02	0x12	INTEGRATION_TIME
0x03	0x13	INT_SELECT
0x04	0x14	INT_THRESH_LSB
0x05	0x15	INT_THRESH_MSB
none	0x16	OUTPUT_TRIM
none	0x17	For future use
0x08	0x18	DEVICE_ID_LSB
0x09	0x19	DEVICE_ID_MSB

Table 10. EEPROM_CONTROL_STATUS REGISTER BITS

Bit	Description
0	Write to EEPROM – when this bit is set to ‘1’, the register whose address is written in the EEPROM_RDWR_REG_ADDRESS register (located at address 0x0A) is written to the EEPROM. The data to be written to EEPROM should be written to registers 0x10 – 0x19 before writing a ‘1’ to this bit.
1	EEPROM write complete flag – after bit[0] of this register is written with a value of ‘1’, the EEPROM write operation is started. After the EEPROM write operation is complete, bit[1] is set to ‘1’ and bit[0] is cleared to ‘0’.
2	Read from EEPROM – when this bit is set to ‘1’, the register whose address is written in the EEPROM_RDWR_REG_ADDRESS register (located at address 0x0A) is read from EEPROM. The data read from EEPROM is placed in the appropriate register 0x10 – 0x19.
3	EEPROM read complete flag – after bit[2] of this register is written with a value of ‘1’, the EEPROM read operation is started. After the EEPROM read operation is complete, bit[3] is set to ‘1’ and bit[2] is cleared to ‘0’.
4−7	Reserved

EEPROM_CONTROL_STATUS Register (0x0B)

The EEPROM_CONTROL_STATUS register is used to effect reads and writes to the EEPROM register specified in EEPROM_RDWR_REG_ADDRESS. Individual control and status register bits are used to initiate reads and writes and to indicate when the operation is complete. Table 10 shows the register bits and their values.

For example, to write the DEVICE_ID_LSB value to the EEPROM, write the DEVICE_ID_LSB to register 0x18. Read back register 0x18 to verify the write and then transfer the data to the EEPROM with the following write command sequence:

1. Issue Start command
2. Issue 0x52 (lower seven bits of I^2C slave address 0x29 followed by write−bit 0) – the write address could be 0x52 (0x29), 0x72 (0x39) or 0x92 (0x49)
3. Issue 0x0A for the EEPROM_RDWR_REG_ADDRESS register address
4. Issue 0x18 for the EEPROM DEVICE_ID_LSB register address to be read
5. Issue Stop command
6. Issue Start command
7. Issue 0x52 (lower seven bits of I^2C slave address 0x29 followed by write−bit 0) – the write address could be 0x52 (0x29), 0x72 (0x39) or 0x92 (0x49)
8. Issue 0x0B for the EEPROM_CONTROL_STATUS register address
9. Issue 0x01 value to initiate an EEPROM write operation
10. Issue Stop command.
11. Wait 15 ms for the EEPROM write operation to complete
12. Issue Start command
13. Issue 0x52 (lower seven bits of I^2C slave address 0x29 followed by write−bit 0) – the write address could be 0x52 (0x29), 0x72 (0x39) or 0x92 (0x49)
14. Issue 0x0B for the EEPROM_CONTROL_STATUS register address
15. Issue Start command
16. Issue 0x53 (lower seven bits of I^2C slave address 0x29 followed by read−bit 1) – the read address could be 0x53 (0x29), 0x73 (0x39) or 0x93 (0x49)
17. Read the EEPROM_CONTROL_STATUS byte
18. Issue Stop command
19. If the EEPROM_CONTROL_STATUS byte equals 0x02 the write is complete, otherwise go to step 12.

To write the DEVICE_ID_MSB value to the EEPROM, the above sequence must be repeated substituting the MSB register address values.

To read the DEVICE_ID_LSB value from the EEPROM, use the following read command sequence:

1. Issue Start command
2. Issue 0x52 (lower seven bits of I^2C slave address 0x29 followed by write−bit 0) – the write address could be 0x52 (0x29), 0x72 (0x39) or 0x92 (0x49)
3. Issue 0x0A for the EEPROM_RDWR_REG_ADDRESS register address
4. Issue 0x18 for the EEPROM DEVICE_ID_LSB register address to be read
5. Issue Stop command
6. Issue Start command
7. Issue 0x52 (lower seven bits of I^2C slave address 0x29 followed by write−bit 0) – the write address could be 0x52 (0x29), 0x72 (0x39) or 0x92 (0x49)
8. Issue 0x0B for the EEPROM_CONTROL_STATUS register address
9. Issue 0x04 value to initiate an EEPROM read operation
10. Issue Stop command.
11. Wait 3 ms for the EEPROM read operation to complete
12. Issue Start command
13. Issue 0x52 (lower seven bits of I^2C slave address 0x29 followed by write−bit 0) – the write address could be 0x52 (0x29), 0x72 (0x39) or 0x92 (0x49)
14. Issue 0x0B for the EEPROM_CONTROL_STATUS register address
15. Issue Start command
16. Issue 0x53 (lower seven bits of I^2C slave address 0x29 followed by read−bit 1) – the read address could be 0x53 (0x29), 0x73 (0x39) or 0x93 (0x49)
17. Read the EEPROM_CONTROL_STATUS byte
18. Issue Stop command
19. If the EEPROM_CONTROL_STATUS byte equals 0x08 proceed to the next step, otherwise go to step 12.
20. Issue Start command
21. Issue 0x52 (lower seven bits of I^2C slave address 0x29 followed by write−bit 0) – the write address could be 0x52 (0x29), 0x72 (0x39) or 0x92 (0x49)
22. Issue 0x18 for the EEPROM DEVICE_ID_LSB register address
23. Issue Start command
24. Issue 0x53 (lower seven bits of I^2C slave address 0x29 followed by read−bit 1) – the read address could be 0x53 (0x29), 0x73 (0x39) or 0x93 (0x49)
25. Read the DEVICE_ID_LSB byte
26. Issue Stop command

To read the DEVICE_ID_MSB value from the EEPROM, the above sequence must be repeated substituting the MSB register address values.

OUTPUT_TRIM Register (0x16)

EEPROM Register Address 0x16 contains 8−bits of output trim covering the range of 0x00 to 0xFF (0 to 255). Table 11 shows the minimum, default and maximum trim available.

Table 11. OUTPUT_TRIM REGISTER VALUES

Input Code	Trim Gain
0000 0000	165%
0101 1101	100%
1111 1111	63%

Changes to the trim register are reflected in real time on the output value of the device.

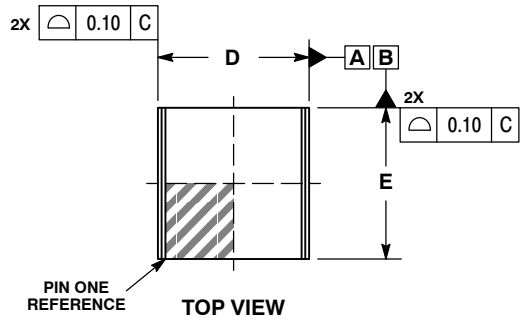
Example Programming Sequence

The following pseudo code configures the NOA1312 ambient light sensor and then runs it in an interrupt driven mode. When the controller receives an interrupt, it reads the ALS_Data from the device, sets a flag and then waits for the main polling loop to respond to the ambient light change.

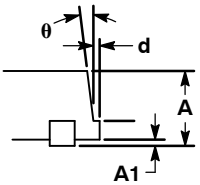
```
external subroutine I2C_Read_Byte (I2C_Address, Data_Address);
external subroutine I2C_Read_Block (I2C_Address, Data_Start_Address, Count, Memory_Map);
external subroutine I2C_Write_Byte (I2C_Address, Data_Address, Data);
external subroutine I2C_Write_Block (I2C_Address, Data_Start_Address, Count, Memory_Map);

subroutine Initialize_ALS () {
 MemBuf[0x00] = 0x10;   // POWER_CONTROL assert Power On
 MemBuf[0x01] = 0x30;   // RESET assert reset
 MemBuf[0x02] = 0x91;   // INTEGRATION_TIME select 200ms
 MemBuf[0x03] = 0x01;   // INT_SELECT select Low to High
 MemBuf[0x04] = 0xFF;   // INT_THRESH_LSB
 MemBuf[0x05] = 0x8F;   // INT_THRESH_MSB
 I2C_Write_Block (I2CAddr, 0x00, 6, MemBuf);
}

subroutine I2C_Interupt_Handler () {
 // Retrieve and store the ALS data
 ALS_Data_LSB = I2C_Read_Byte (I2CAddr, 0x06);
 ALS_Data_MSB = I2C_Read_Byte (I2CAddr, 0x07);
 NewALS = 0x01;
 }

subroutine main_loop () {
 I2CAddr = 0x29;
 NewALS = 0x00;
 Initialize_ALS ();
 loop {
  // Do some other polling operations
  if (NewALS == 0x01) {
   NewALS = 0x00;
   // Do some operations with ALS_Data
   }
  }
 }
```

PACKAGE DIMENSIONS

CUDFN6, 2x2
CASE 505AD−01
ISSUE B



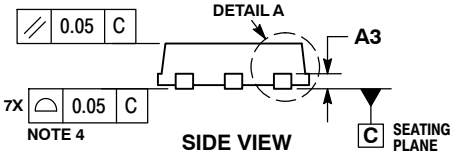
TOP VIEW



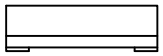
DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

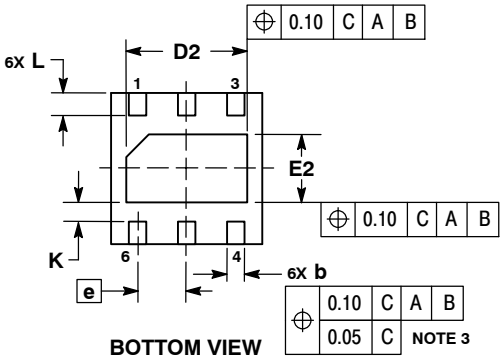
	MILLIMETERS	
DIM	MIN	MAX
A	0.55	0.65
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.28
D	2.00 BSC	
D2	1.50	1.70
d	---	0.10
E	2.00 BSC	
E2	0.80	1.00
e	0.65 BSC	
K	0.20	---
L	0.25	0.35
θ	4°	10°



SIDE VIEW

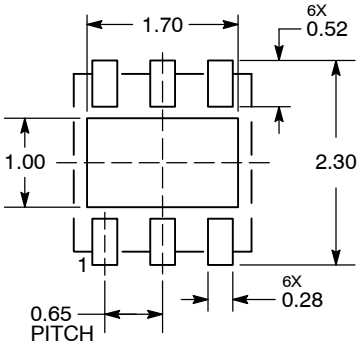


END VIEW



BOTTOM VIEW

MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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