NCV8165

LDO Regulator for RF and Analog Circuits - Ultra-Low Noise and High PSRR

500 mA

The NCV8165 is a linear regulator capable of supplying 500 mA output current. Designed to meet the requirements of RF and analog circuits, the NCV8165 device provides low noise, high PSRR, low quiescent current, and very good load/line transients. The device is designed to work with a 1 μF input and a 1 μF output ceramic capacitor. It is available in DFNW8 3 mm x 3 mm package with wettable flanks.

Features

- Operating Input Voltage Range: 1.9 V to 5.5 V
- Available in Fixed Voltage Option: 1.8 V to 5.2 V
- ±2% Accuracy Over Load/Temperature
- Ultra Low Quiescent Current Typ. 12 μA
- Standby Current: Typ. 0.1 μA
- Very Low Dropout: 190 mV at 500 mA
- Ultra High PSRR: Typ. 85 dB at 20 mA, f = 1 kHz
- Ultra Low Noise: 8.5 μV_{RMS}
- Stable with a 1 μF Small Case Size Ceramic Capacitors
- Available in −DFNW8 0.65P, 3 mm x 3 mm x 0.9 mm Package
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Battery−powered Equipment
- Wireless LAN Devices
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders

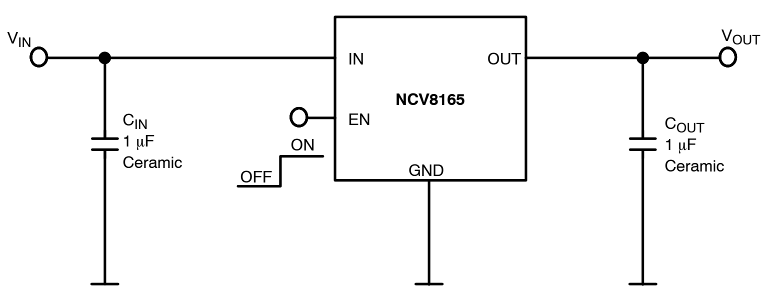

Figure 1. Typical Application Schematics

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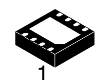
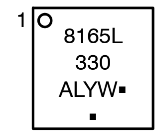
MARKING DIAGRAM



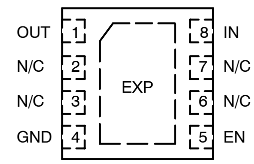
DFNW8, 3x3
CASE 507AD



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



DFNW8 3x3 mm
(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

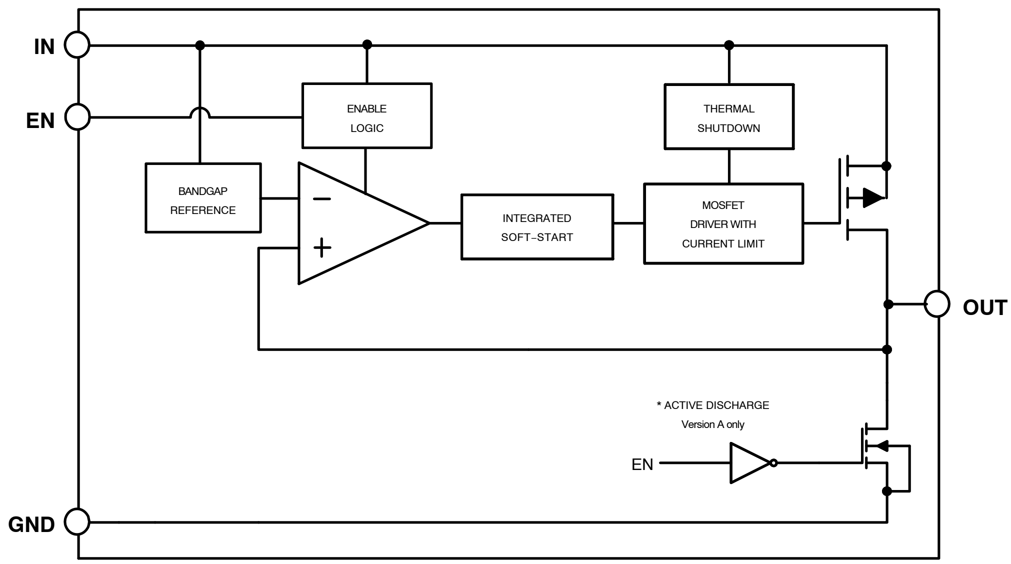


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
8	IN	Input voltage supply pin
1	OUT	Regulated output voltage. The output should be bypassed with small 1 μF ceramic capacitor.
5	EN	Chip enable: Applying V_{EN} < 0.4 V disables the regulator, Pulling V_{EN} > 1.2 V enables the LDO.
4	GND	Common ground connection
EPAD	EPAD	Expose pad should be tied to ground plane for better power dissipation

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 V to 6	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} + 0.3, max. 6 V	V
Chip Enable Input	V_{CE}	−0.3 to V_{IN} + 0.3, max. 6 V	V
Output Short Circuit Duration	t_{SC}	unlimited	s
Maximum Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Input Voltage	V_{IN}	1.9	5.5	V
Junction Temperature	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, DFNW8 (Note 3) Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	100	°C/W

3. Measured according to JEDEC board specification. Detailed description of the board can be found in JESD51−7.

ELECTRICAL CHARACTERISTICS −40°C ≤ T_J ≤ 125°C; V_{IN} = $V_{OUT(NOM)}$ + 1 V; I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1 µF, unless otherwise noted. V_{EN} = 1.2 V. Typical values are at T_J = +25°C (Note 4).

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	1.9		5.5	V
Output Voltage Accuracy (Note 5)	V_{IN} = $V_{OUT(NOM)}$ + 1 V to 5.5 V 0 mA ≤ I_{OUT} ≤ 500 mA		V_{OUT}	−2		+2	%
Line Regulation	$V_{OUT(NOM)}$ + 1 V ≤ V_{IN} ≤ 5.5 V		$Line_{Reg}$		0.09		mV/V
Load Regulation	I_{OUT} = 1 mA to 500 mA		$Load_{Reg}$		0.01		mV/mA
Dropout Voltage (Note 6)	I_{OUT} = 500 mA	$V_{OUT(NOM)}$ = 1.8 V	V_{DO}		315	450	mV
		$V_{OUT(NOM)}$ = 3.3 V			190	290	
Output Current Limit	V_{OUT} = 90% $V_{OUT(NOM)}$		I_{CL}	800	1000		mA
Short Circuit Current	V_{OUT} = 0 V		I_{SC}		1050		
Quiescent Current	I_{OUT} = 0 mA		I_Q		9.7	18	µA
Shutdown Current	V_{EN} ≤ 0.4 V, V_{IN} = 4.8 V		I_{DIS}		0.01	1	µA
EN Pin Threshold Voltage	EN Input Voltage “H”		V_{ENH}	1.2			V
	EN Input Voltage “L”		V_{ENL}			0.4	
EN Pull Down Current	V_{EN} = 4.8 V		I_{EN}		0.2	0.5	µA
Turn−On Time	C_{OUT} = 1 µF, From assertion of V_{EN} to V_{OUT} = 95% $V_{OUT(NOM)}$				120		µs
Power Supply Rejection Ratio	$V_{OUT(NOM)}$ = 3.3 V, I_{OUT} = 20 mA	f = 100 Hz f = 1 kHz f = 10 kHz f = 100 kHz	PSRR		83 85 80 63		dB
Output Voltage Noise	f = 10 Hz to 100 kHz	I_{OUT} = 20 mA	V_N		8.5		μV_{RMS}
Thermal Shutdown Threshold	Temperature rising		T_{SDH}		160		°C
	Temperature falling		T_{SDL}		140		°C
Active output discharge resistance	V_{EN} < 0.4 V, Version A only		R_{DIS}		280		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Respect SOA.
6. Dropout voltage is characterized when V_{OUT} falls 100 mV below $V_{OUT(NOM)}$.

TYPICAL CHARACTERISTICS

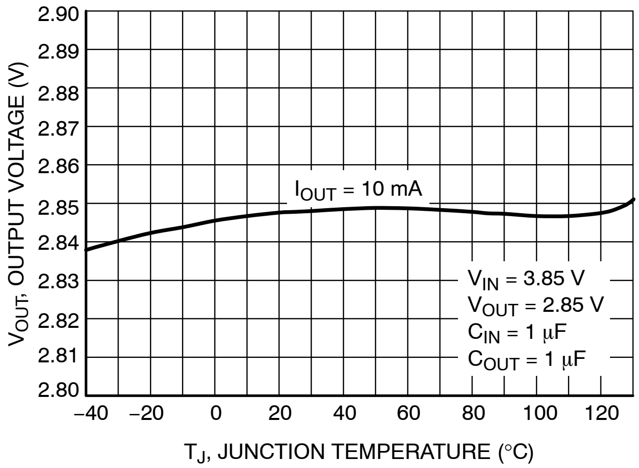


Figure 3. Output Voltage vs. Temperature – V_{OUT} = 2.85 V

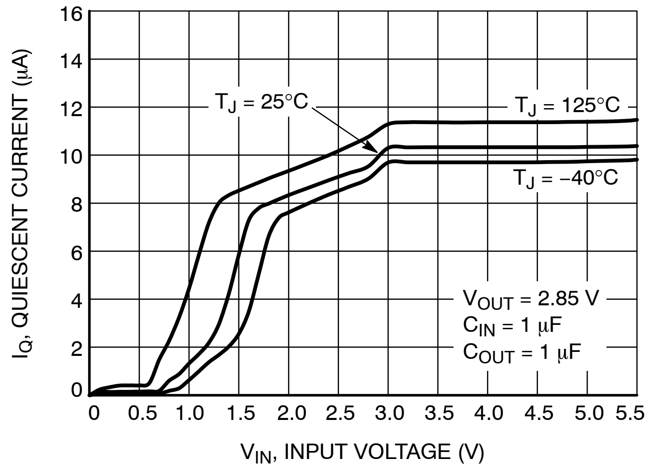


Figure 4. Quiescent Current vs. Input Voltage

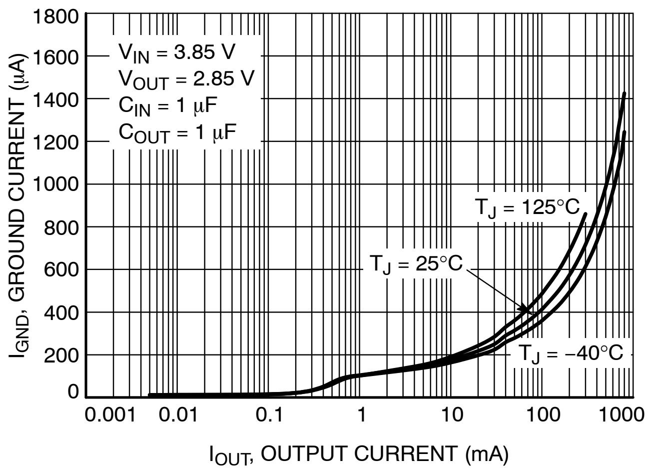


Figure 5. Ground Current vs. Output Current

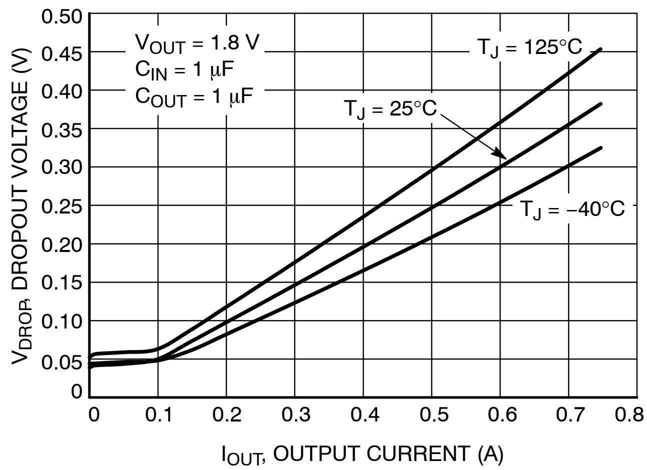


Figure 6. Dropout Voltage vs. Output Current – V_{OUT} = 1.8 V

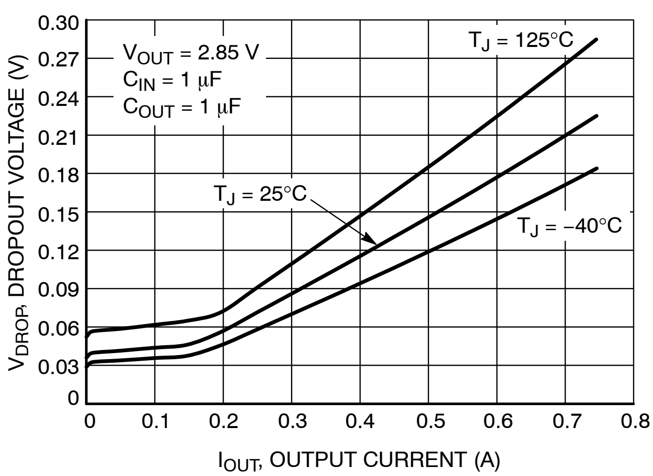


Figure 7. Dropout Voltage vs. Output Current – V_{OUT} = 2.85 V

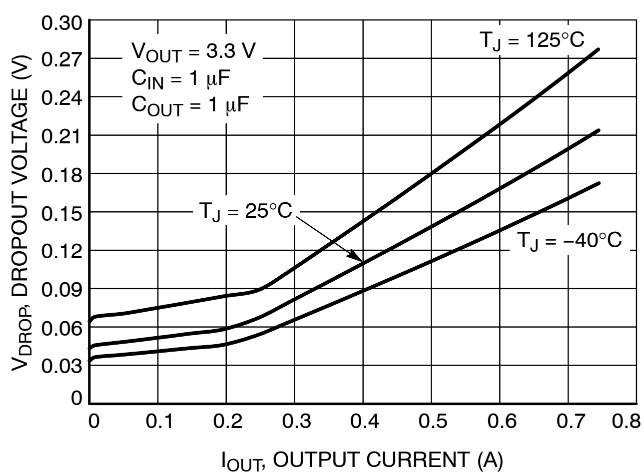


Figure 8. Dropout Voltage vs. Output Current – V_{OUT} = 3.3 V

TYPICAL CHARACTERISTICS

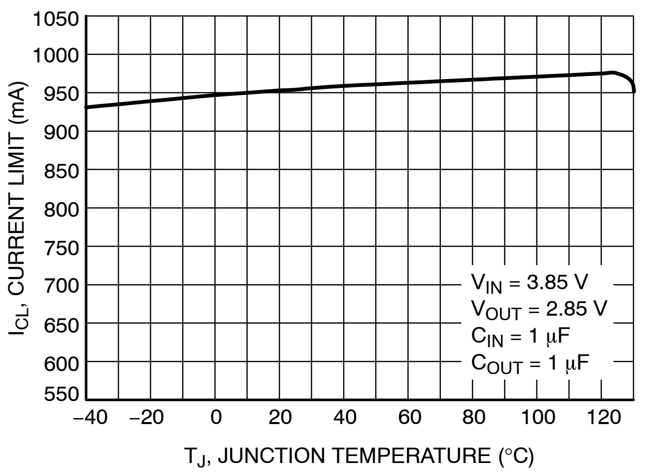


Figure 9. Current Limit vs. Temperature

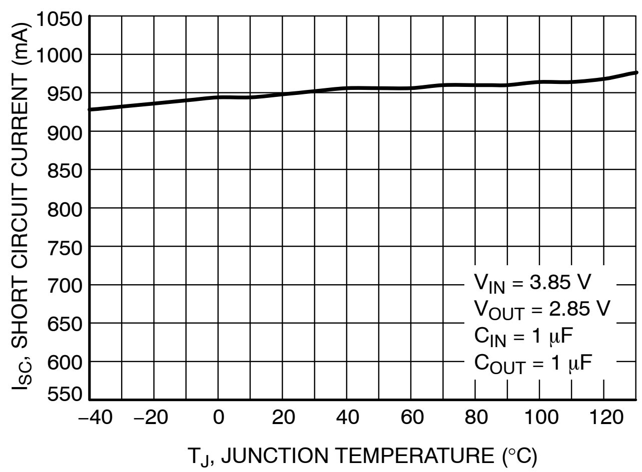


Figure 10. Short Circuit Current vs. Temperature

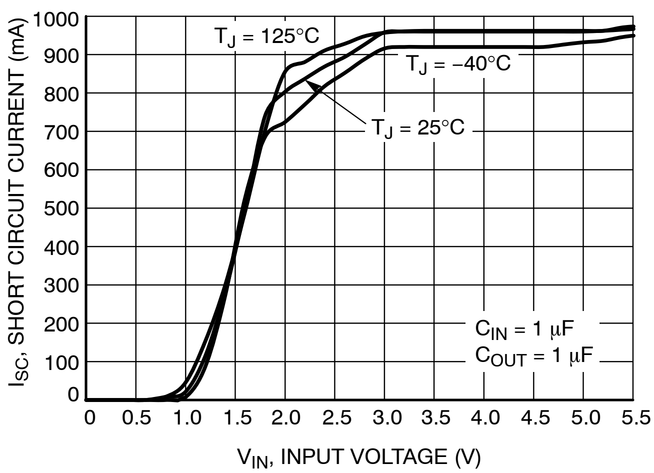


Figure 11. Short Circuit Current vs. Input Voltage

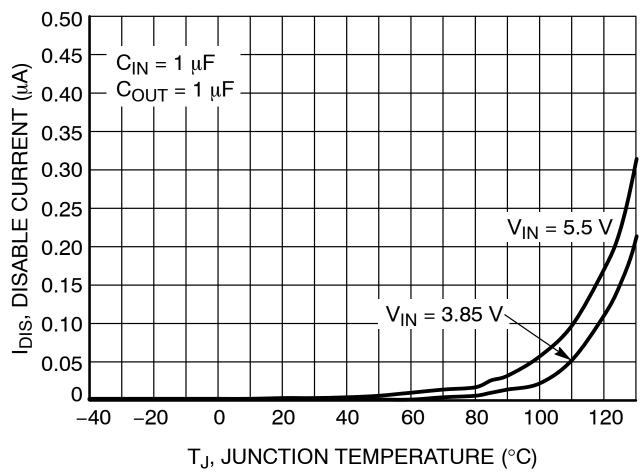


Figure 12. Disable Current vs. Temperature

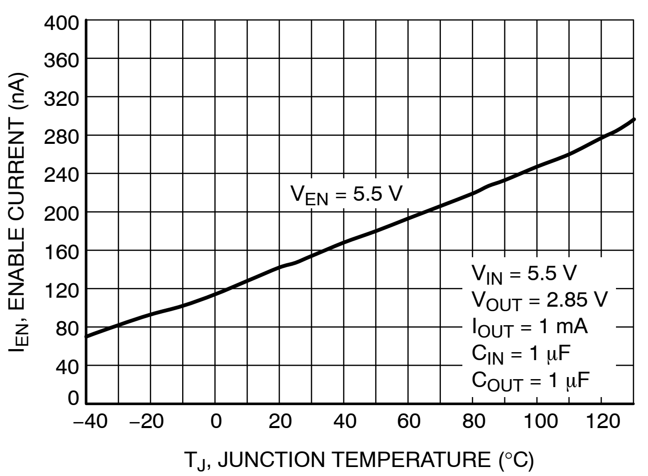


Figure 13. Current to Enable Pin vs. Temperature

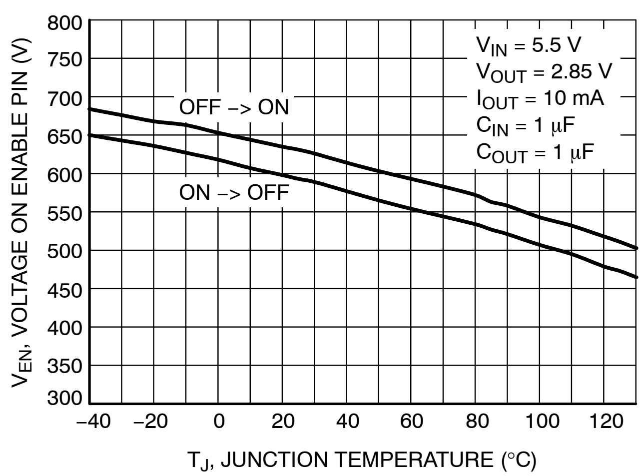


Figure 14. Enable Voltage Threshold vs. Temperature

TYPICAL CHARACTERISTICS

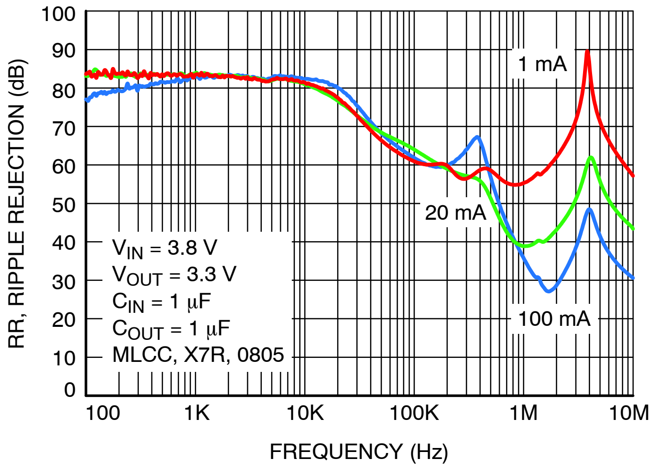


Figure 15. Power Supply Rejection Ratio vs. Current, V_{DROP} = 0.5 V, C_{OUT} = 1 µF

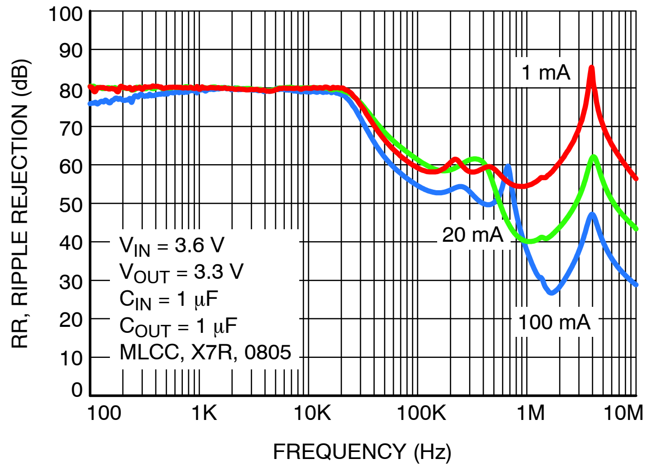


Figure 16. Power Supply Rejection Ratio vs. Current, V_{DROP} = 0.3 V, C_{OUT} = 1 µF

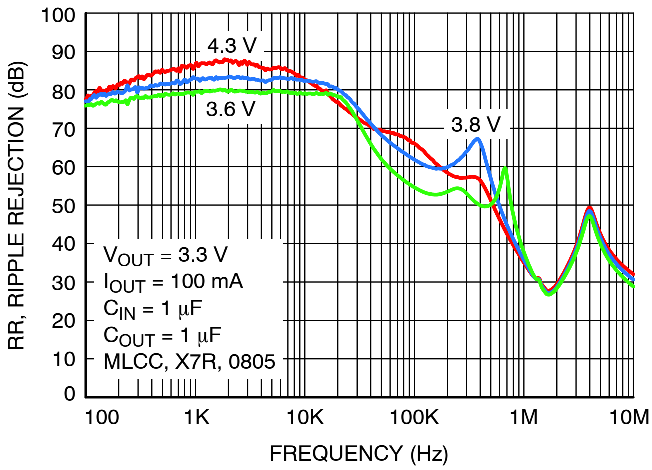


Figure 17. Power Supply Rejection Ratio vs. Input Voltage, I_{OUT} = 100 mA, C_{OUT} = 1 µF

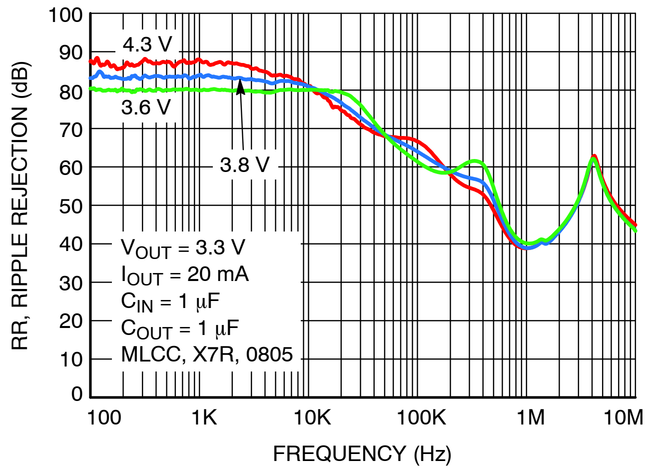


Figure 18. Power Supply Rejection Ratio vs. Input Voltage, I_{OUT} = 20 mA, C_{OUT} = 1 µF

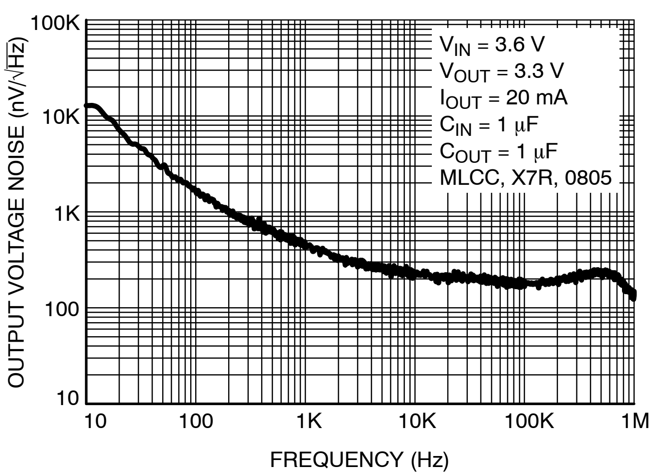


Figure 19. Output Voltage Noise Spectral Density for V_{OUT} = 3.3 V, I_{OUT} = 20 mA, C_{OUT} = 1 µF

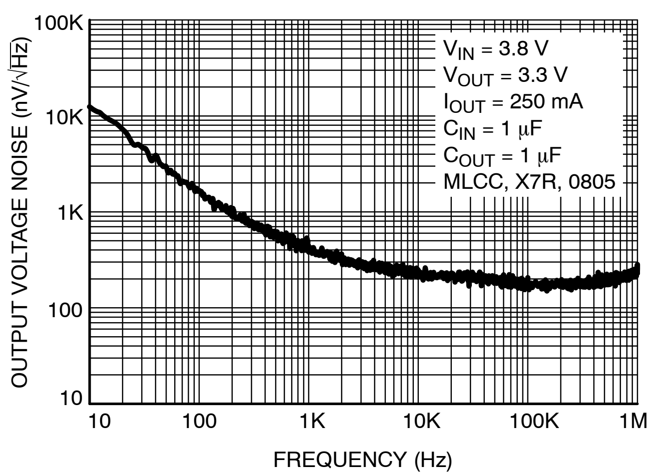


Figure 20. Output Voltage Noise Spectral Density for V_{OUT} = 3.3 V, I_{OUT} = 250 mA, C_{OUT} = 1 µF

APPLICATIONS INFORMATION

General

The NCV8165 is an ultra−low noise 500 mA low dropout regulator designed to meet the requirements of RF applications and high performance analog circuits. The NCV8165 device provides very high PSRR and excellent dynamic response. In connection with low quiescent current this device is well suitable for battery powered application such as cell phones, tablets and other. The NCV8165 is fully protected in case of current overload, output short circuit and overheating.

Input Capacitor Selection (C_{IN})

Input capacitor connected as close as possible is necessary for ensure device stability. The X7R or X5R capacitor should be used for reliable performance over temperature range. The value of the input capacitor should be 1 μF or greater to ensure the best dynamic performance. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes.

Output Decoupling (C_{OUT})

The NCV8165 requires an output capacitor connected as close as possible to the output pin of the regulator. The recommended capacitor value is 1 μF and X7R or X5R dielectric due to its low capacitance variations over the specified temperature range. The NCV8165 is designed to remain stable with minimum effective capacitance of 0.7 μF to account for changes with temperature, DC bias and package size. Especially for small package size capacitors such as 0201 the effective capacitance drops rapidly with the applied DC bias. Please refer Figure 21.

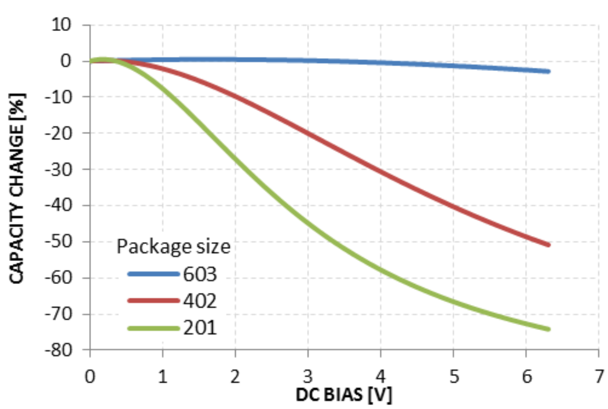


Figure 21. Capacity vs DC Bias Voltage

There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 1.7 Ω. Larger output capacitors and lower ESR could improve the load transient response or high frequency PSRR. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature.

Enable Operation

The NCV8165 uses the EN pin to enable/disable its device and to deactivate/activate the active discharge function. If the EN pin voltage is <0.4 V the device is guaranteed to be disabled. The pass transistor is turned−off so that there is virtually no current flow between the IN and OUT. The active discharge transistor is active so that the output voltage V_{OUT} is pulled to GND through a 280 Ω resistor. In the disable state the device consumes as low as typ. 10 nA from the V_{IN}. If the EN pin voltage >1.2 V the device is guaranteed to be enabled. The NCV8165 regulates the output voltage and the active discharge transistor is turned−off. The EN pin has internal pull−down current source with typ. value of 200 nA which assures that the device is turned−off when the EN pin is not connected. In the case where the EN function isn’t required the EN should be tied directly to IN.

Output Current Limit

Output Current is internally limited within the IC to a typical 1000 mA. The NCV8165 will source this amount of current measured with a voltage drops on the 90% of the nominal V_{OUT}. If the Output Voltage is directly shorted to ground (V_{OUT} = 0 V), the short circuit protection will limit the output current to 1050 mA (typ.). The current limit and short circuit protection will work properly over whole temperature range and also input voltage range. There is no limitation for the short circuit duration.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold (T_{SD} = 160°C typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold (T_{SDU} = 140°C typical). Once the IC temperature falls below the 140°C the LDO is enabled again. The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

Power Supply Rejection Ratio

The NCV8165 features very high Power Supply Rejection ratio. If desired the PSRR at higher frequencies in the range 100 kHz – 10 MHz can be tuned by the selection of C_{OUT} capacitor and proper PCB layout.

Turn−On Time

The turn−on time is defined as the time period from EN assertion to the point in which V_{OUT} will reach 98% of its nominal value. This time is dependent on various application conditions such as $V_{OUT(NOM)}$, C_{OUT}, T_A.

Power Dissipation

As power dissipated in the NCV8165 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. For reliable operation junction temperature should be limited to +125°C. The maximum power dissipation the NCV8165 can handle is given by:

$$P_{D(MAX)} = \frac{\left[125°C - T_A\right]}{\theta_{JA}} \qquad \text{(eq. 1)}$$

The power dissipated by the NCV8165 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN} \cdot I_{GND} + I_{OUT}\left(V_{IN} - V_{OUT}\right) \qquad \text{(eq. 2)}$$

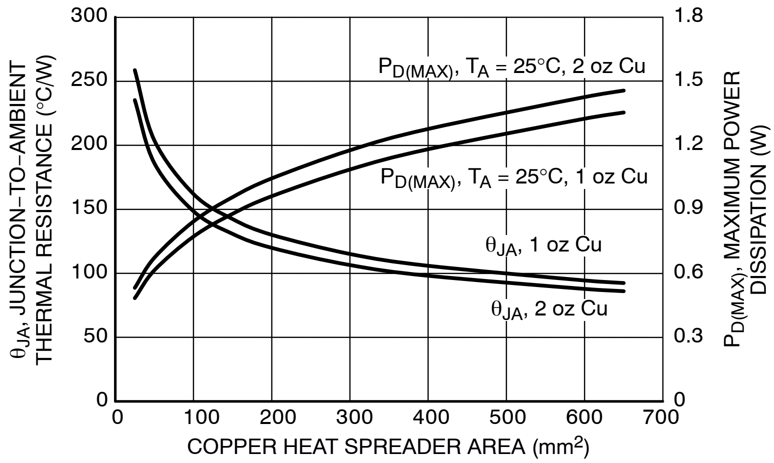


Figure 22. θ_{JA} and $P_{D(MAX)}$ vs. Copper Area (DFNW8)

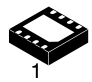
PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place C_{IN} and C_{OUT} capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size, use 0402 or 0201 capacitors with appropriate capacity. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Equation 2). Expose pad can be tied to the GND pin for improvement power dissipation and lower device temperature.

ORDERING INFORMATION

Device	Nominal Output Voltage	Description	Marking	Package	Shipping†
NCV8165ML330TBG	3.3 V	500 mA, Active Discharge	8165L 330	DFNW8 (Pb−Free)	3000 / Tape & Reel
NCV8165ML330TCG	3.3 V	500 mA, Active Discharge	8165L 330		

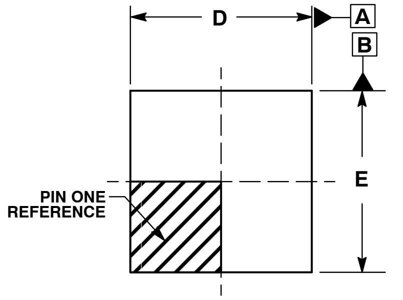
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



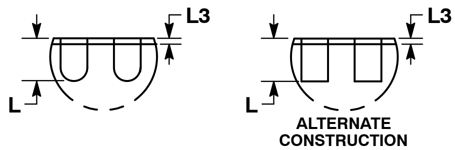
SCALE 2:1

DFNW8 3x3, 0.65P
CASE 507AD
ISSUE A

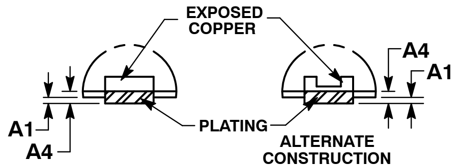
DATE 15 JUN 2018



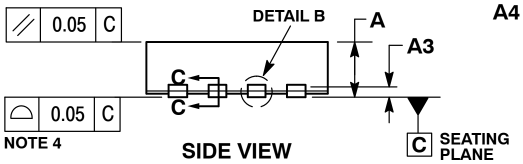
TOP VIEW



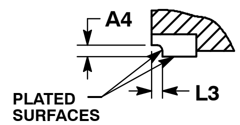
DETAIL A



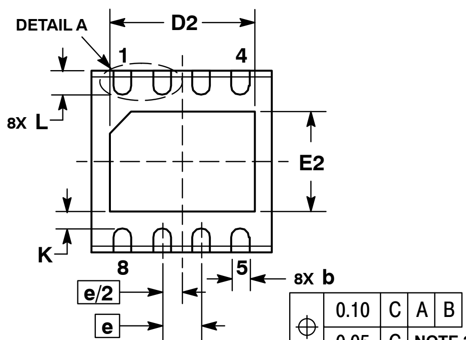
DETAIL B



SIDE VIEW

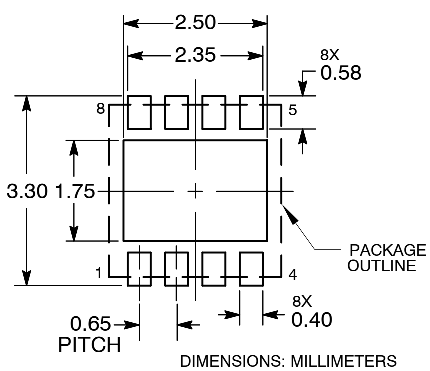


SECTION C−C



BOTTOM VIEW

RECOMMENDED SOLDERING FOOTPRINT*

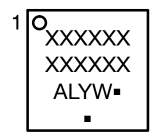


*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURE TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	---	---	0.05
A3	0.20 REF		
A4	0.10	---	---
b	0.25	0.30	0.35
D	2.90	3.00	3.10
D2	2.30	2.40	2.50
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
e	0.65 BSC		
K	0.28 REF		
L	0.30	0.40	0.50
L3	0.05 REF		

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DFNW8 3x3, 0.65P**	**PAGE 1 OF 1**

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