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# Voltage Regulator – Low Dropout, Enable, Low $I_q$

# NCV4266-2C

## 150 mA

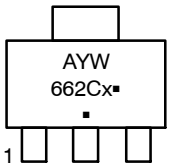
SOT−223
ST SUFFIX
CASE 318E

The NCV4266−2C is a 150 mA output current integrated low dropout, low quiescent current regulator family designed for use in harsh automotive environments. It includes wide operating temperature and input voltage ranges. The device is offered with fixed voltage versions of 3.3 V and 5.0 V available in 2% output voltage accuracy. It has a high peak input voltage tolerance and reverse input voltage protection. It also provides overcurrent protection, overtemperature protection and enable function for control of the state of the output voltage. The NCV4266−2C is available in SOT−223 surface mount package. The output is stable over a wide output capacitance and ESR range. The NCV4266−2C has improved startup behavior during input voltage transients.

**Features**

- Output Voltage Options: 3.3 V, 5.0 V
- Output Voltage Accuracy: ±2.0%
- Output Current: up to 150 mA
- Low Quiescent Current (typ. 40 μA @ 100 μA)
- Low Dropout Voltage (typ. 250 mV @ 100 mA)
- Enable Input
- Fault Protection
  - +45 V Peak Transient Voltage
  - −42 V Reverse Voltage
  - Short Circuit
  - Thermal Overload
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

**MARKING DIAGRAM**




| | |
|---|---|
| A | = Assembly Location |
| Y | = Year |
| W | = Work Week |
| x | = Voltage Option<br>3.3 V (x = 3)<br>5.0 V (x = 5) |
| ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

**ORDERING INFORMATION**

See detailed ordering and shipping information in the ordering information section on page 10 of this data sheet.

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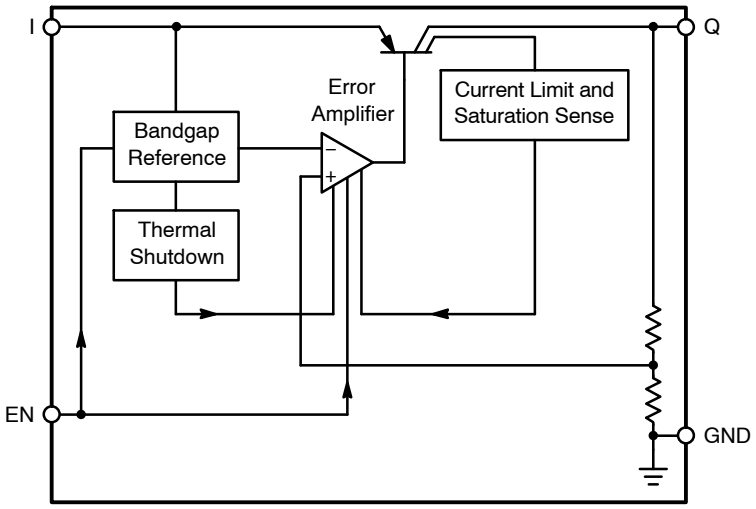


**Figure 1. Block Diagram**

## PIN FUNCTION DESCRIPTION

| Pin No. DFN8 | Pin No. | Symbol | Description |
|---|---|---|---|
| 1 | 1 | I | Input; Battery Supply Input Voltage. |
| 3 | 2 | EN | Enable Input; Low level disables the IC. |
| 4 | 3 | Q | Output; Bypass with a capacitor to GND. |
| 8 | 4 | GND | Ground. |

## MAXIMUM RATINGS

| Symbol | Rating | Min | Max | Unit |
|---|---|---|---|---|
| $V_I$ | Input Voltage | −42 | 45 | V |
| $V_I$ | Input Peak Transient Voltage | – | 45 | V |
| $V_{EN}$ | Enable Input Voltage | −42 | 45 | V |
| $V_Q$ | Output Voltage | −0.3 | 32 | V |
| $I_q$ | Ground Current | – | 100 | mA |
| $V_I$ | Input Voltage Operating Range | $V_Q$ + 0.5 V or 4.5 (Note 1) | 45 | V |
| – | ESD Susceptibility (Human Body Model) | 3.0 | – | kV |
| $T_J$ | Junction Temperature | −40 | 150 | °C |
| $T_{stg}$ | Storage Temperature | −50 | 150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Minimum $V_I$ = 4.5 V or ($V_Q$ + 0.5 V), whichever is higher.

## LEAD TEMPERATURE SOLDERING REFLOW AND MSL (Note 2)

| Symbol | Rating | Min | Max | Unit |
|---|---|---|---|---|
| $T_{SLD}$ | Lead Temperature Soldering<br>Reflow (SMD styles only), Leaded, 60−150 s above 183, 30 s max at peak<br>Reflow (SMD styles only), Free, 60−150 s above 217, 40 s max at peak<br>Wave Solder (through hole styles only), 12 sec max | <br>–<br>–<br>– | <br>240<br>265<br>310 | °C |
| MSL | Moisture Sensitivity Level | 3 | | – |

2. Per IPC / JEDEC J−STD−020C.

## THERMAL RESISTANCE

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $R_{\theta JA}$ | Junction−to−Ambient SOT−223 | | – | 109 (Note 3) | °C/W |
| $R\psi_{JT}$ | Junction−to−Tab SOT−223 | | – | 10.9 | °C/W |

3. 1 oz copper, 100 $mm^2$ copper area, FR4.

## ELECTRICAL CHARACTERISTICS (−40°C < $T_J$ < 150°C, $V_I$ = 13.5 V, $V_{EN}$ = 5 V; unless otherwise noted.)

| Symbol | Characteristic | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | |
| $V_Q$ | Output Voltage (5.0 V Version) | 100 μA < $I_Q$ < 150 mA, 6.0 V < $V_I$ < 28 V | 4.9 | 5.0 | 5.1 | V |
| $V_Q$ | Output Voltage (3.3 V Version) | 100 μA < $I_Q$ < 150 mA, 4.5 V < $V_I$ < 28 V | 3.234 | 3.3 | 3.366 | V |
| $I_Q$ | Output Current Limitation | $V_Q$ = 90% $V_{QTYP}$ | 150 | 390 | 500 | mA |
| $I_q$ | Quiescent Current (Sleep Mode) $I_q = I_I - I_Q$ | $V_{EN}$ = 0 V, $T_J$ = −40°C to 100°C | – | 0 | 1.0 | μA |
| $I_q$ | Quiescent Current, $I_q = I_I - I_Q$ | $I_Q$ = 100 μA, $T_J$ < 85°C | – | 40 | 60 | μA |
| $I_q$ | Quiescent Current, $I_q = I_I - I_Q$ | $I_Q$ = 100 μA | – | 40 | 70 | μA |
| $I_q$ | Quiescent Current, $I_q = I_I - I_Q$ | $I_Q$ = 50 mA | – | 0.55 | 4.0 | mA |
| $V_{DR}$ | Dropout Voltage (5.0 V Version) | $I_Q$ = 100 mA, $V_{DR} = V_I - V_Q$ (Note 4) | – | 230 | 500 | mV |
| $\Delta V_{Q,LO}$ | Load Regulation (5.0 V Version) | $I_Q$ = 1.0 mA to 100 mA | – | 3.5 | 90 | mV |
| $\Delta V_{Q,LO}$ | Load Regulation (3.3 V Version) | $I_Q$ = 1.0 mA to 100 mA | – | 0.5 | 60 | mV |
| $\Delta V_Q$ | Line Regulation (5.0 V Version) | $\Delta V_I$ = 6.0 V to 28 V, $I_Q$ = 1.0 mA | – | 1.0 | 30 | mV |
| $\Delta V_Q$ | Line Regulation (3.3 V Version) | $\Delta V_I$ = 4.5 V to 28 V, $I_Q$ = 1.0 mA | – | 0.5 | 20 | mV |
| PSRR | Power Supply Ripple Rejection | $f_r$ = 100 Hz, $V_r$ = 0.5 $V_{PP}$ | – | 68 | – | dB |
| **ENABLE INPUT** | | | | | | |
| $V_{EN}$ | Enable Voltage, Output High | $V_Q \geq V_{QMIN}$ | – | 2.0 | 2.7 | V |
| $V_{EN}$ | Enable Voltage, Output Low (Off) | $V_Q \leq$ 0.1 V | 0.8 | 1.8 | – | V |
| $I_{EN}$ | Enable Input Current | $V_{EN}$ = 5.0 V | – | 4.0 | 8.0 | μA |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SD}$ | Thermal Shutdown Temperature* | | 150 | – | 200 | °C |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*Guaranteed by design, not tested in production.

4. Measured when the output voltage $V_Q$ has dropped 100 mV from the nominal value obtained at V = 13.5 V.

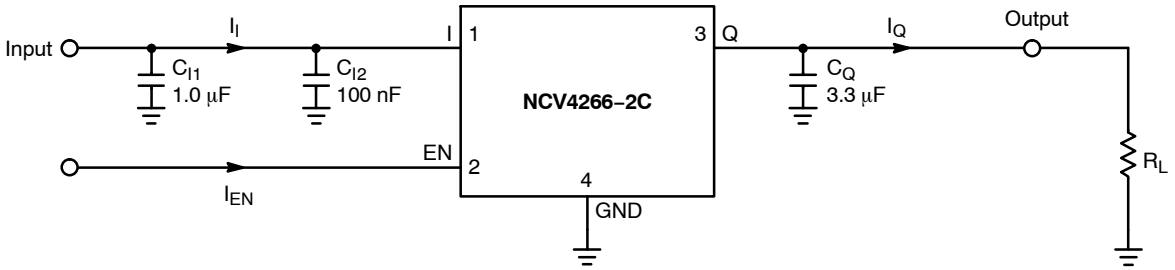


**Figure 2. Applications Circuit**

## TYPICAL CHARACTERISTICS CURVES − 5 V VERSION

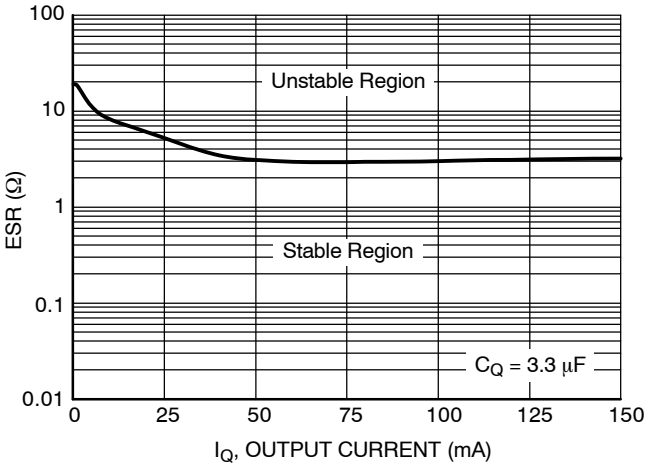


**Figure 3. Output Stability with Output Capacitor ESR**

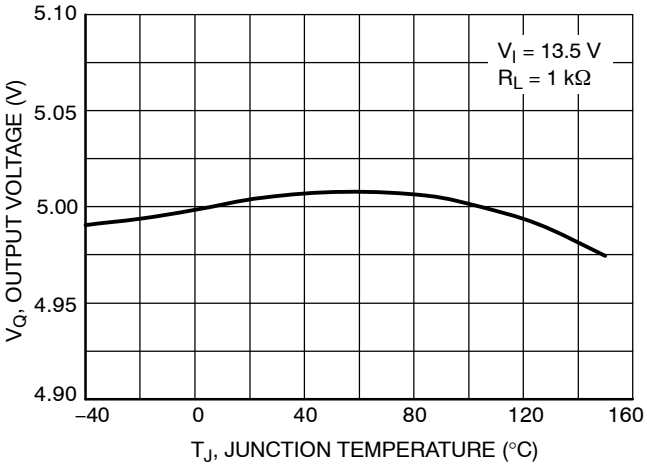


**Figure 4. Output Voltage vs. Junction Temperature**

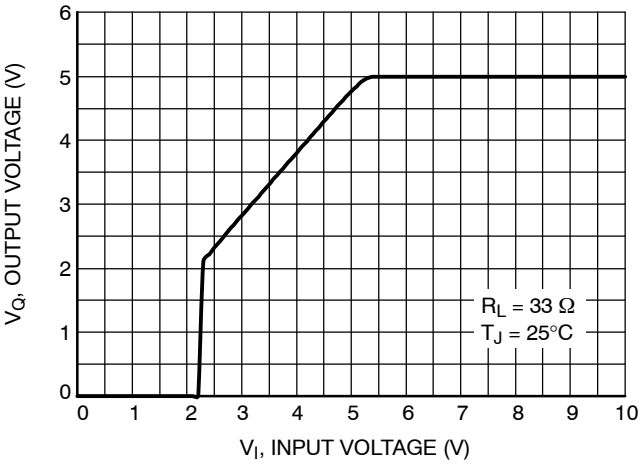


**Figure 5. Output Voltage vs. Input Voltage**

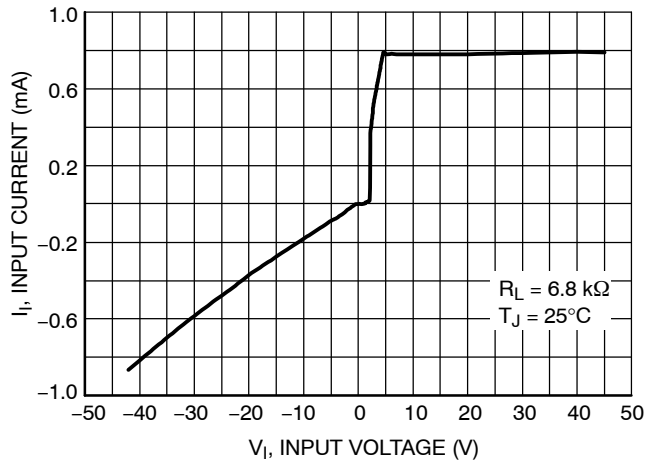


**Figure 6. Input Current vs. Input Voltage**

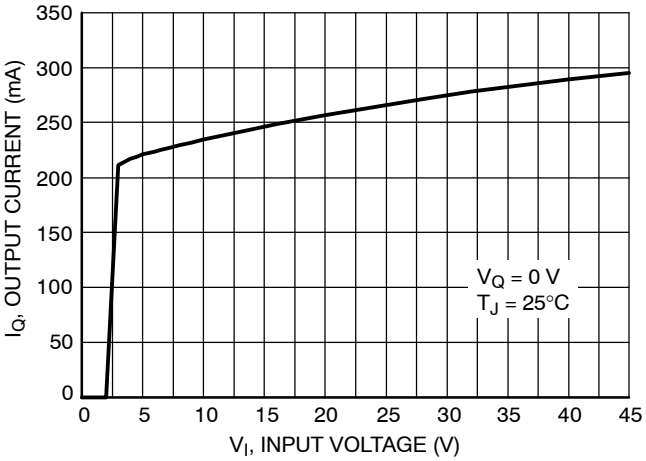


**Figure 7. Maximum Output Current vs. Input Voltage**

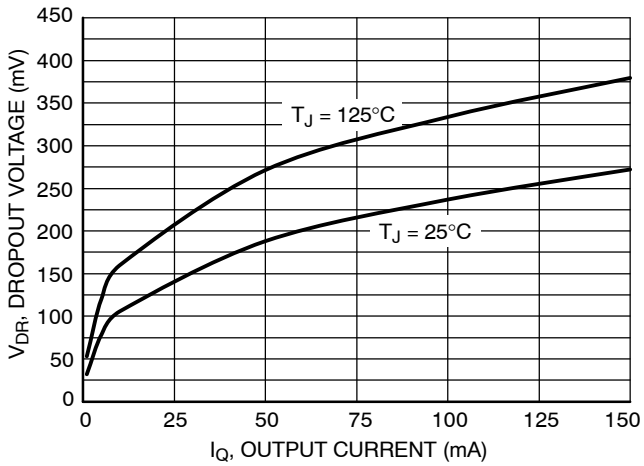


**Figure 8. Dropout Voltage vs. Output Current**

## TYPICAL CHARACTERISTICS CURVES − 5 V VERSION (continued)

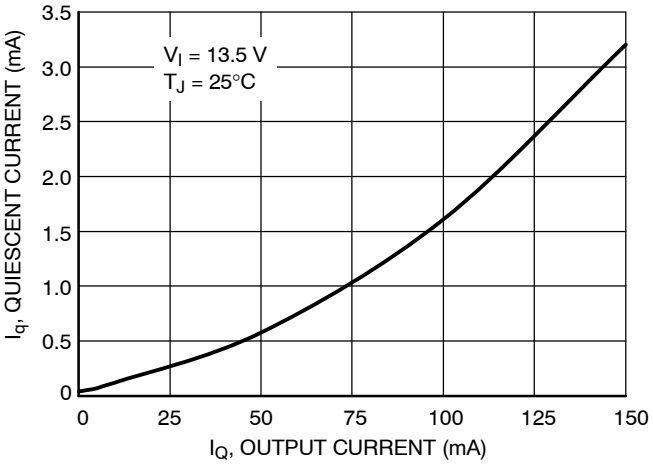


**Figure 9. Quiescent Current vs. Output Current (High Load)**

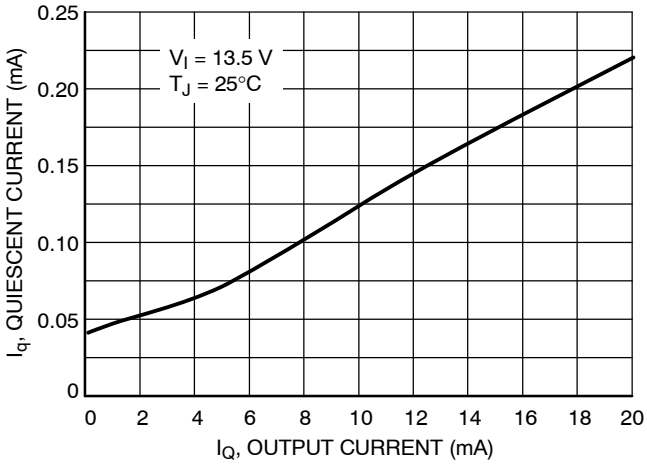


**Figure 10. Quiescent Current vs. Output Current (Low Load)**

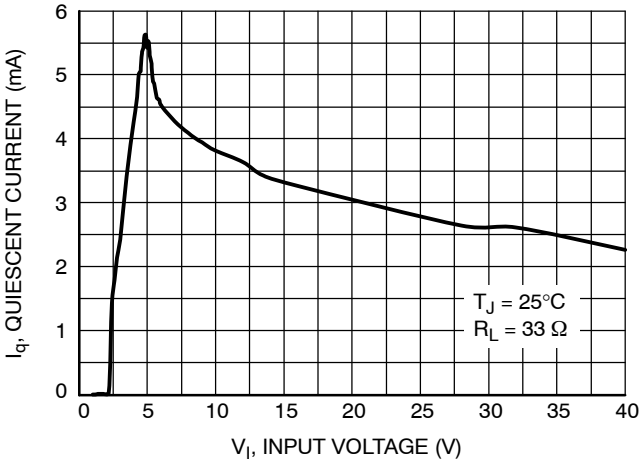


**Figure 11. Quiescent Current vs. Input Voltage**

## TYPICAL CHARACTERISTICS CURVES − 3.3 V VERSION

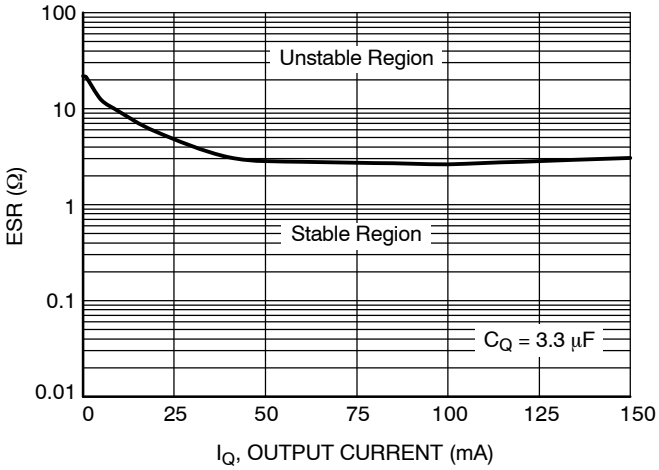


**Figure 12. Output Stability with Output Capacitor ESR**

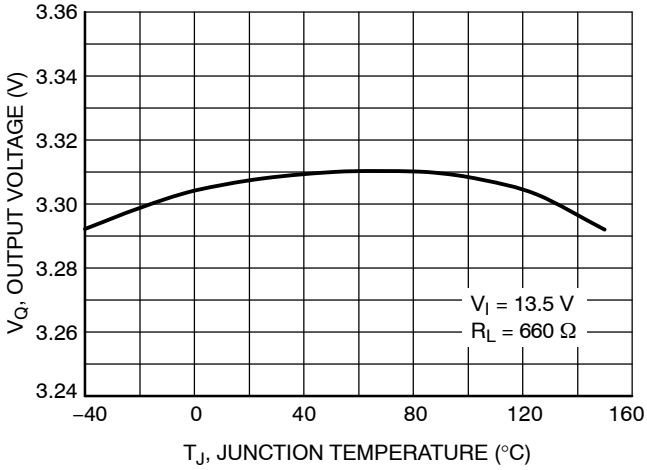


**Figure 13. Output Voltage vs. Junction Temperature**

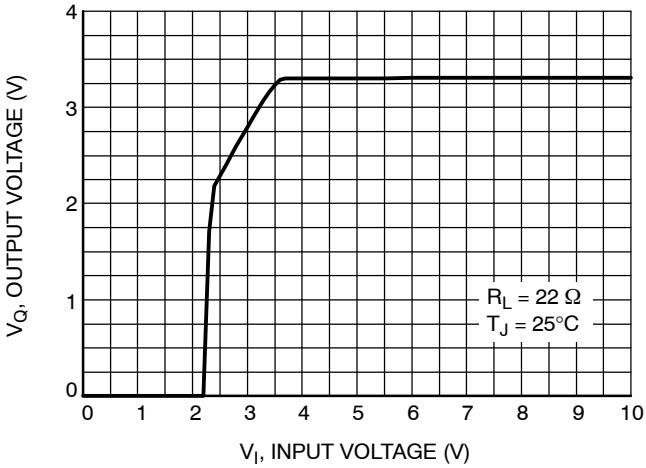


**Figure 14. Output Voltage vs. Input Voltage**

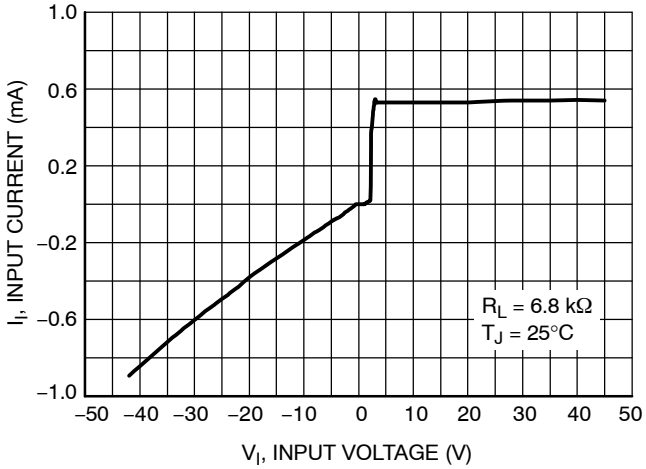


**Figure 15. Input Current vs. Input Voltage**

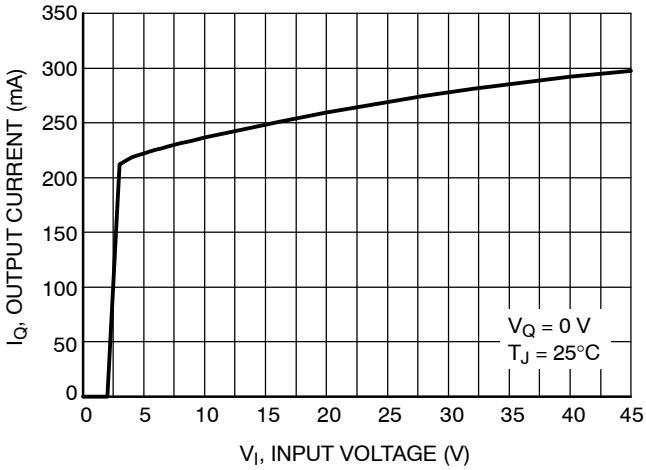


**Figure 16. Maximum Output Current vs. Input Voltage**

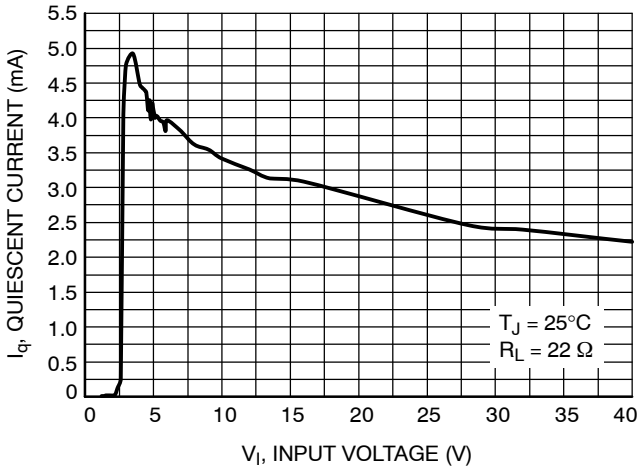


**Figure 17. Quiescent Current vs. Input Voltage**

## TYPICAL CHARACTERISTICS CURVES − 3.3 V VERSION (continued)

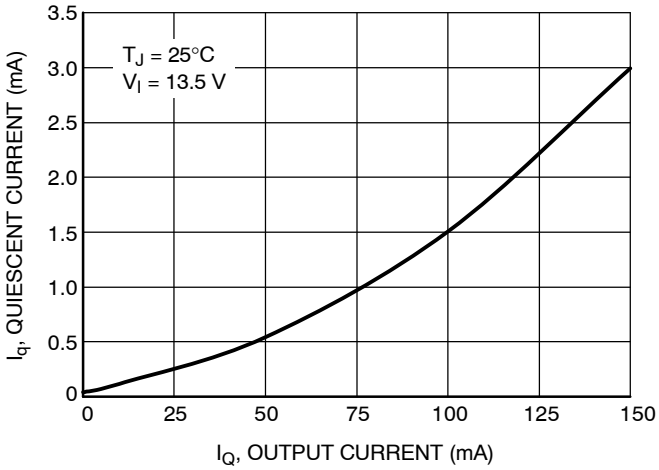


**Figure 18. Quiescent Current vs. Output Current (High Load)**

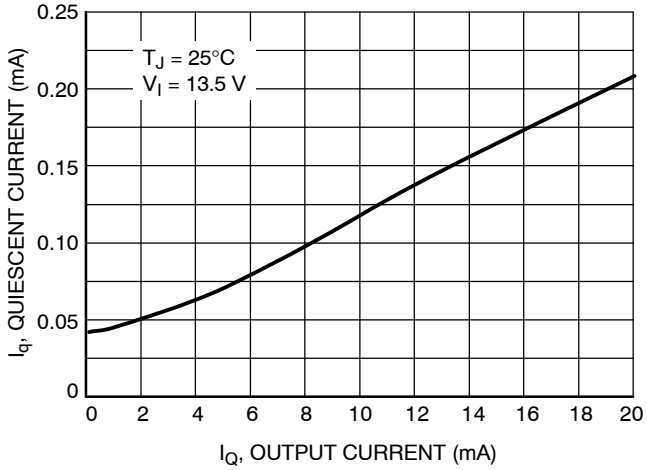


**Figure 19. Quiescent Current vs. Output Current (Low Load)**

## CIRCUIT DESCRIPTION

The NCV4266−2C is an integrated low dropout regulator that provides a regulated voltage at 150 mA to the output. It is enabled with an input to the enable pin. The regulator voltage is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference, which gives it the lowest possible dropout voltage. The output current capability is 150 mA, and the base drive quiescent current is controlled to prevent oversaturation when the input voltage is low or when the output is overloaded. The regulator is protected by both current limit and thermal shutdown. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

## REGULATOR

The error amplifier compares the reference voltage to a sample of the output voltage ($V_Q$) and drives the base of a PNP series pass transistor via a buffer. The reference is a bandgap design to give it a temperature−stable output. Saturation control of the PNP is a function of the load current and input voltage. Oversaturation of the output power device is prevented, and quiescent current in the ground pin is minimized. See Figure 2, Test Circuit, for circuit element nomenclature illustration.

## REGULATOR STABILITY CONSIDERATIONS

The input capacitors ($C_{I1}$ and $C_{I2}$) are necessary to stabilize the input impedance to avoid voltage line influences. Using a resistor of approximately 1.0 Ω in series with $C_{I2}$ can stop potential oscillations caused by stray inductance and capacitance.

The output capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information.

The value for the output capacitor $C_Q$, shown in Figure 2, should work for most applications; see also Figures 3 and 12 for output stability at various load and Output Capacitor ESR conditions. Stable region of ESR in Figures 3 and 12 shows ESR values at which the LDO output voltage does not have any permanent oscillations at any dynamic changes of output load current. Marginal ESR is the value at which the output voltage waving is fully damped during five periods after the load change and no oscillation is further observable.

ESR characteristics were measured with ceramic capacitors and additional series resistors to emulate ESR. Low duty cycle pulse load current technique has been used to maintain junction temperature close to ambient temperature.

## ENABLE INPUT

The enable pin is used to turn the regulator on or off. By holding the pin down to a voltage less than 0.8 V, the output of the regulator will be turned off. When the voltage on the enable pin is greater than 2.7 V, the output of the regulator will be enabled to power its output to the regulated output voltage. The enable pin may be connected directly to the input pin to give constant enable to the output regulator.

## CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 20) is:

$$P_{D(max)} = [V_{I(max)} - V_{Q(min)}]\,I_{Q(max)} + V_{I(max)}I_q \quad \text{(eq. 1)}$$

where

| | |
|---|---|
| $V_{I(max)}$ | is the maximum input voltage, |
| $V_{Q(min)}$ | is the minimum output voltage, |
| $I_{Q(max)}$ | is the maximum output current for the application, |
| $I_q$ | is the quiescent current the regulator consumes at $I_{Q(max)}$. |

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^{o}C - T_A}{P_D} \quad \text{(eq. 2)}$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$ less than the calculated value in Equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

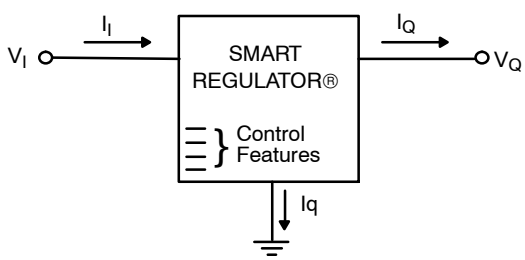


**Figure 20. Single Output Regulator with Key Performance Parameters Labeled**

## HEATSINKS

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad \text{(eq. 3)}$$

where

| | |
|---|---|
| $R_{\theta JC}$ | is the junction−to−case thermal resistance, |
| $R_{\theta CS}$ | is the case−to−heatsink thermal resistance, |
| $R_{\theta SA}$ | is the heatsink−to−ambient thermal resistance. |

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in data sheets of heatsink manufacturers.

Thermal, mounting, and heatsinking considerations are discussed in the **onsemi** application note AN1040/D.

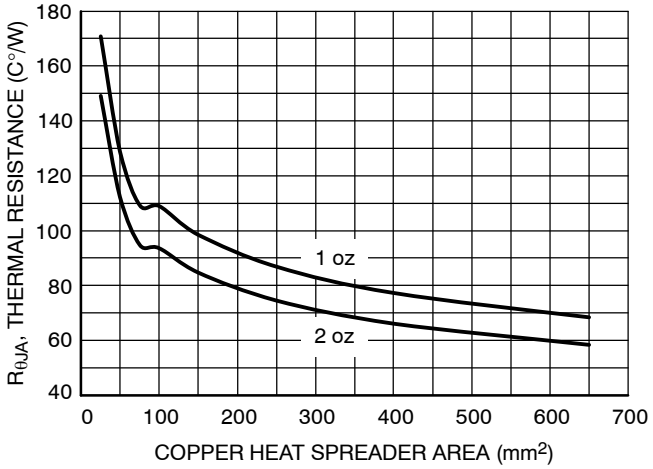


**Figure 21. $R_{\theta JA}$ vs. Copper Spreader Area, SOT−223**

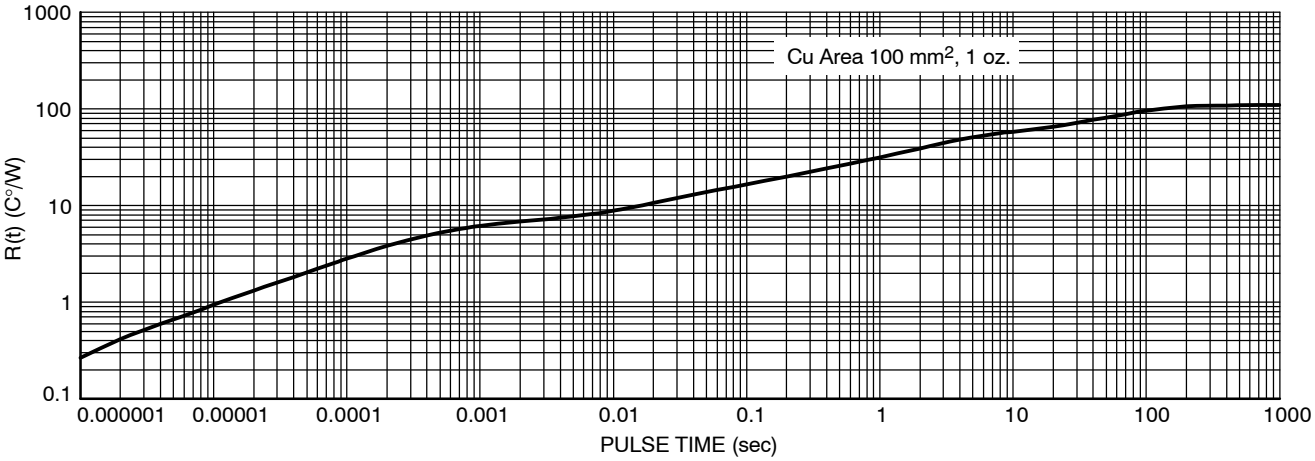


**Figure 22. Single−Pulse Heating Curve, SOT−223**

## ORDERING INFORMATION

| Device* | Output Voltage | Package | Shipping† |
|---|---|---|---|
| NCV4266−2CST33T3G | 3.3 V | SOT−223 (Pb−Free) | 4000 / Tape & Reel |
| NCV4266−2CST50T3G | 5.0 V | SOT−223 (Pb−Free) | 4000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

SCALE 1:1

**SOT−223 (TO−261)**
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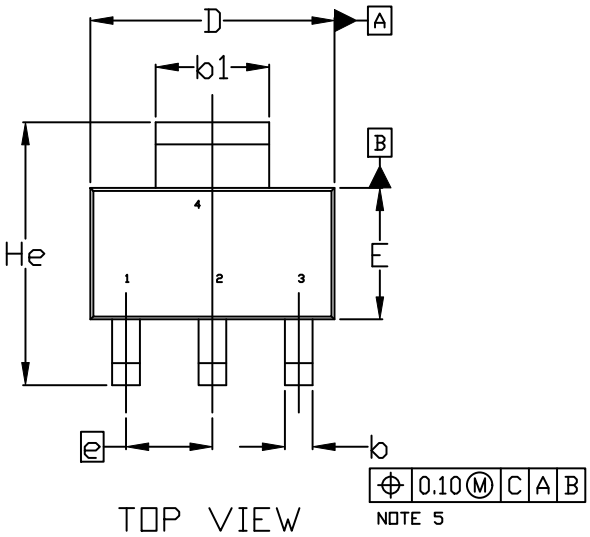
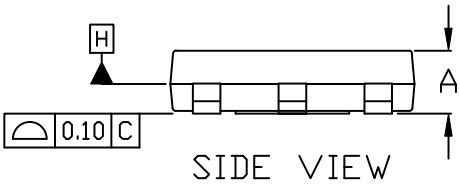
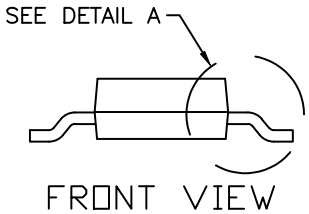
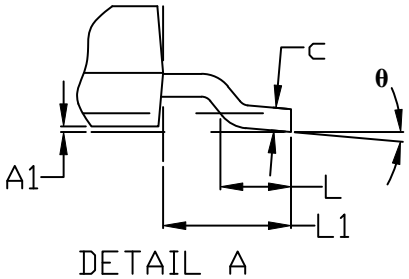
DATE 02 OCT 2018



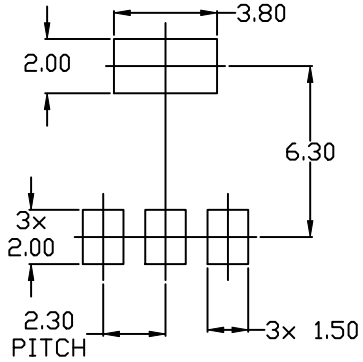




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A | 1.50 | 1.63 | 1.75 |
| A1 | 0.02 | 0.06 | 0.10 |
| b | 0.60 | 0.75 | 0.89 |
| b1 | 2.90 | 3.06 | 3.20 |
| c | 0.24 | 0.29 | 0.35 |
| D | 6.30 | 6.50 | 6.70 |
| E | 3.30 | 3.50 | 3.70 |
| e | 2.30 BSC | | |
| L | 0.20 | --- | --- |
| L1 | 1.50 | 1.75 | 2.00 |
| He | 6.70 | 7.00 | 7.30 |
| θ | 0° | --- | 10° |

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STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

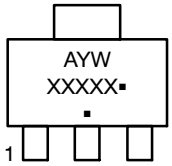
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

**GENERIC**
**MARKING DIAGRAM***




A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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