NCP4624

150 mA, Wide Input Range, LDO Linear Voltage Regulator

The NCP4624 is a CMOS 150 mA LDO linear voltage regulator which features high input voltage range while maintaining low quiescent current 2 μA typically. Several protection features like Current Limiting and Reverse Current Protection Circuit are fully integrated to create a versatile device suitable for the power source being in the standby−mode. A high maximum input voltage (11 V) and wide temperature range (−40°C to 85°C) makes the NCP4624 device with output capacitor as low as 0.1 μF an ideal choice for industrial applications also a portable equipments powered by 2−cell Li−ion battery.

Features

- Operating Input Voltage Range: 2.5 V to Set V_{OUT} + 6.5 V, Max. 11 V
- Output Voltage Range: 1.2 to 5.5 V (available in 0.1 V steps)
- ±2% Output Voltage Accuracy
- Output Current: min. 150 mA
- Line Regulation: 0.02%/V
- Current Limit Circuit
- Available in SOT−23−5, UDFN4 1.0 x 1.0 mm and SC−88A Package
- Built−in Reverse Current Protection Circuit
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Home Appliances, Industrial Equipment
- Cable Boxes, Satellite Receivers, Entertainment Systems
- Car Audio Equipment, Navigation Systems
- Notebook Adaptors, LCD TVs, Cordless Phones and Private LAN Systems
- Battery−Powered Portable Communication Equipments

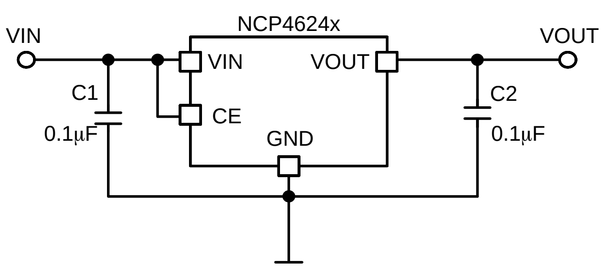

Figure 1. Typical Application Schematic

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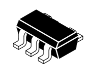
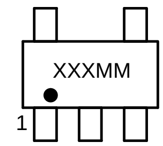
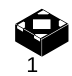
MARKING DIAGRAMS

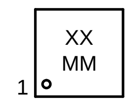


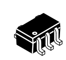
SOT−23−5
CASE 1212



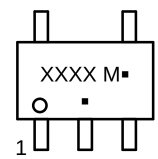


UDFN4
CASE 517BR





SC−88A
(SC−70−5/SOT−353)
CASE 419A



XX, XXX, XXXX	=	Specific Device Code
M, MM	=	Date Code
A	=	Assembly Location
Y	=	Year
W	=	Work Week
▪	=	Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

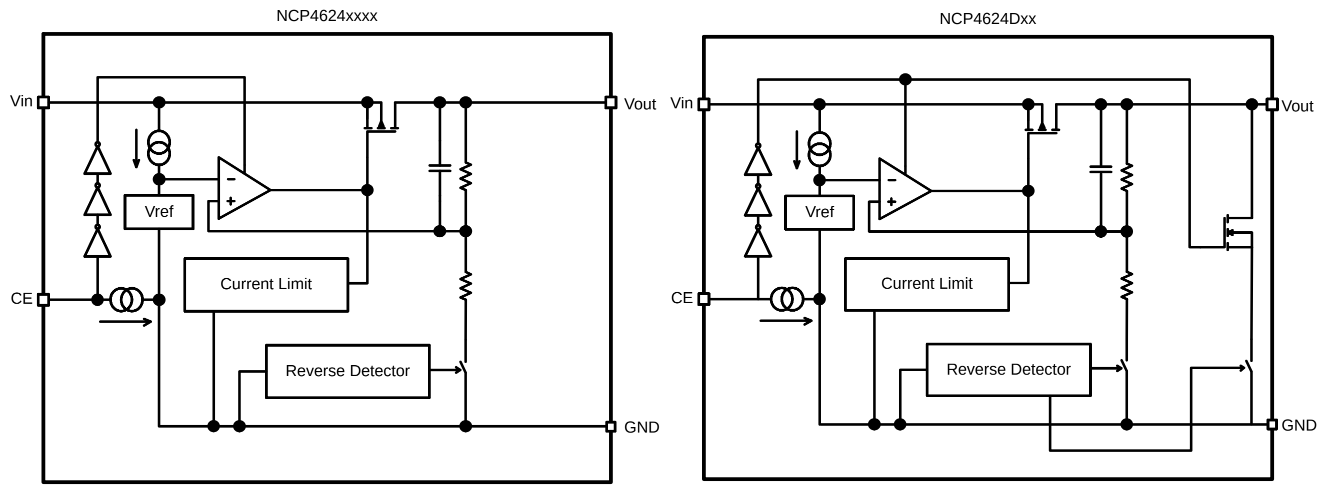


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.			Pin Name	Description
SOT−23−5	SC−88A	UDFN 1x1		
1	5	4	VIN	Input pin
2	3	2	GND	Ground pin
3	1	3	CE	Chip enable pin (“H” active)
4	2		NC	Non connected
5	4	1	VOUT	Output pin
		*EP	EP	Exposed Pad (leave floating or connect to GND)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 to 12	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} ≤ 11	V
Chip Enable Input	V_{CE}	−0.3 to V_{IN} ≤ 11	V
Power Dissipation SOT−23−5	P_D	420	mW
Power Dissipation uDFN 1.0 x 1.0 mm		400	
Power Dissipation SC−88A		380	
Junction Temperature	T_J	−40 to 150	°C
Storage Temperature	T_{STG}	−55 to 125	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to Electrical Characteristics and Application Information for safe operating area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOT−23−5 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	238	°C/W
Thermal Characteristics, uDFN 1x1 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	250	°C/W
Thermal Characteristics, SC−88A Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	263	°C/W

ELECTRICAL CHARACTERISTICS −40°C ≤ T_A ≤ 85°C; C_{IN} = C_{OUT} = 0.1 μF, unless otherwise noted. Typical values are at T_A = +25°C.

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage	1.2 V < V_{OUT} < 4.5 V		V_{IN}	2.5		Vset + 6.5	V
	4.5 V ≤ V_{OUT} < 5.5 V					11	
Output Voltage	Ta = 25°C, V_{OUT} > 1.5 V		V_{OUT}	x0.99		x1.01	V
	−40°C < T_A < 85°C, V_{OUT} > 1.5V			x0.982		x1.018	
	T_A = 25°C, V_{OUT} < 1.5 V			−15		+15	mV
	−40°C < T_A < 85°C, V_{OUT} < 1.5V			−28		+28	
Output Voltage Temp. Coefficient	V_{IN} = V_{OUT} + 2 V, I_{OUT} = 100 μA, T_A = −40 to 105°C				±100		ppm/°C
Line Regulation	Set V_{OUT} + 0.5 V < V_{IN} < V_{IN} max, I_{OUT} = 1 mA		$Line_{Reg}$		0.02	0.20	%/V
Load Regulation	V_{IN} = V_{OUT} + 2 V, 0.1mA < I_{OUT} ≤ 150 mA		$Load_{Reg}$	−35	−3	35	mV
Dropout Voltage	I_{OUT} = 150 mA	1.2 V ≤ V_{OUT} < 1.3 V	V_{DO}		1.68	2.59	V
		1.3 V ≤ V_{OUT} < 1.5 V			1.63	2.49	
		1.5 V ≤ V_{OUT} < 1.8 V			1.48	2.23	
		1.8 V ≤ V_{OUT} < 2.3 V			1.16	2.19	
		2.3 V ≤ V_{OUT} < 3.0 V			0.90	1.47	
		3.0 V ≤ V_{OUT} < 4.0 V			0.61	1.05	
		4.0 V ≤ V_{OUT} ≤ 5.5 V			0.39	0.76	
Output Current			I_{OUT}	150			mA
Short Current Limit	V_{OUT} = 0 V		I_{SC}		45		mA
Quiescent Current	Iout = 0 mA		I_Q		2.0	3.7	μA
Standby Current	V_{IN} = $V_{IN\ max}$, V_{CE} = 0 V		I_{STB}		0.2	0.6	μA
CE Pin Pull−Down Current			I_{PD}		0.3	0.9	μA
CE Pin Threshold Voltage	CE Input Voltage “H”		V_{CEH}	1.7		V_{IN}	V
	CE Input Voltage “L”		V_{CEL}	0		0.8	
Reverse Current	0 V ≤ V_{IN} < 11 V, V_{OUT} > 1.5 V		I_{REV}		0	0.16	μA
Reverse Current Detection Offset	0 V ≤ V_{IN} < 11 V, V_{OUT} > 1.5 V		V_{REV_DET}		55	100	mV
Reverse Current Release Offset	0 V ≤ V_{IN} < 11 V, V_{OUT} > 1.5 V		V_{REV_REL}		70	120	mV
Power Supply Rejection Ratio	V_{IN} = V_{OUT} + 2.5 V, ΔV_{IN_PK-PK} = 0.3 V, I_{OUT} = 50 mA, f = 1 kHz	V_{OUT} = 1.2 V	PSRR		27		dB
		V_{OUT} = 2.5 V			22		
		V_{OUT} = 3.3 V			18		
		V_{OUT} = 5.5 V			15		
Output Noise Voltage	V_{OUT} = 1.2 V, I_{OUT} = 30 mA, f = 100 Hz to 100 kHz		V_{NOISE}		105		μV_{rms}
Autodischarge NMOS Resistance	V_{IN} = 7.0 V, V_{CE} = 0.0 V (D version only)		R_{DSON}		380		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

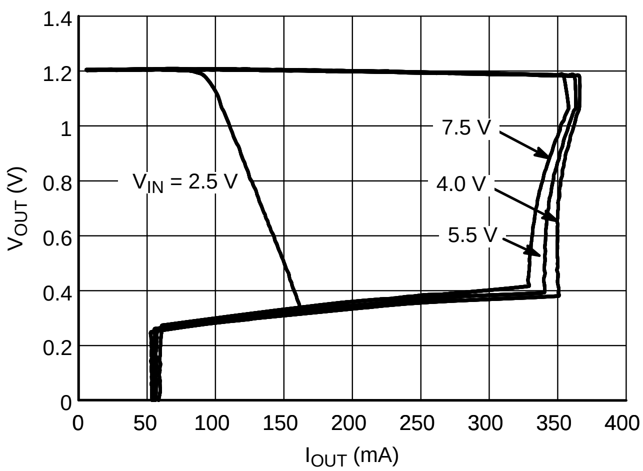


Figure 3. Output Voltage vs. Output Current 1.2 V Version (T_J = 25°C)

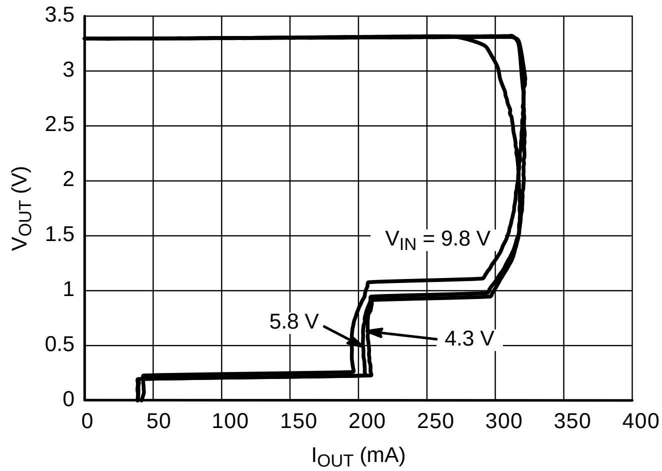


Figure 4. Output Voltage vs. Output Current 3.3 V Version (T_J = 25°C)

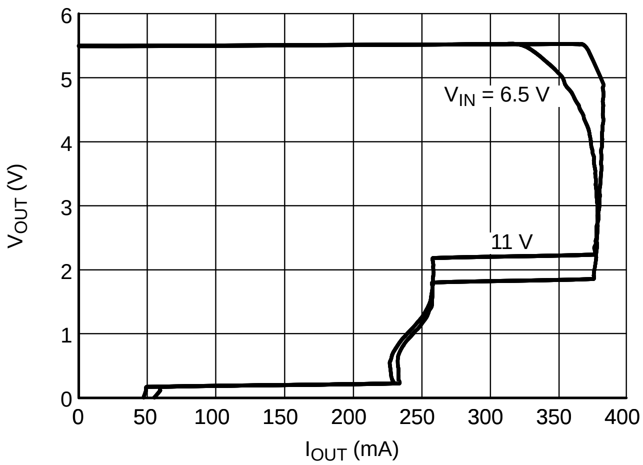


Figure 5. Output Voltage vs. Output Current 5.5 V Version (T_J = 25°C)

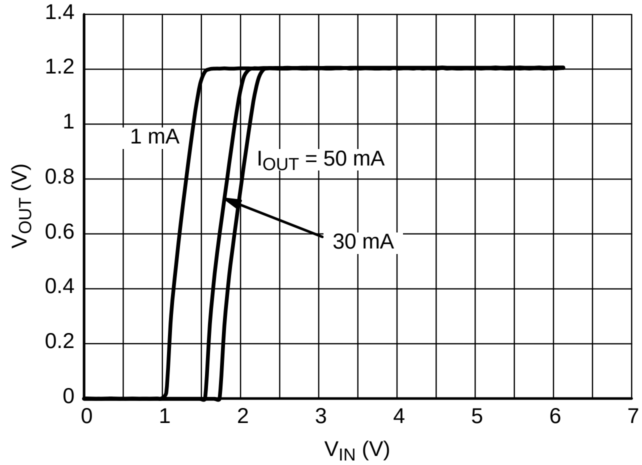


Figure 6. Output Voltage vs. Input Voltage 1.2 V Version

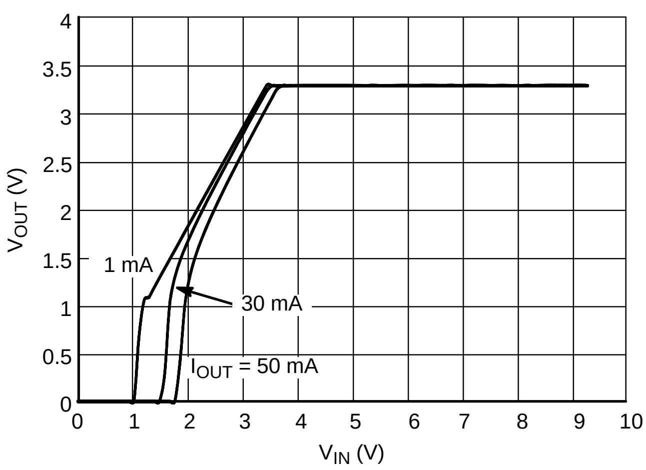


Figure 7. Output Voltage vs. Input Voltage 3.3 V Version

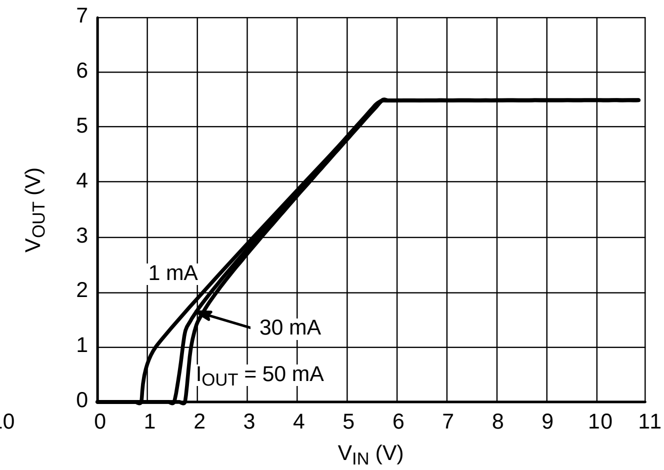


Figure 8. Output Voltage vs. Input Voltage 5.5 V Version

TYPICAL CHARACTERISTICS

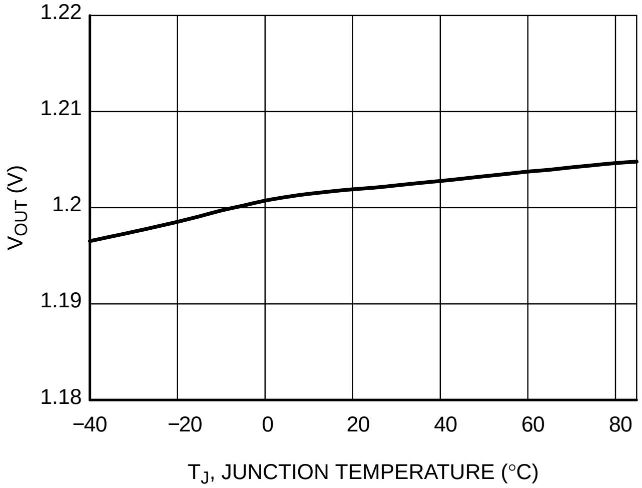


Figure 9. Output Voltage vs. Temperature, 1.2 V Version

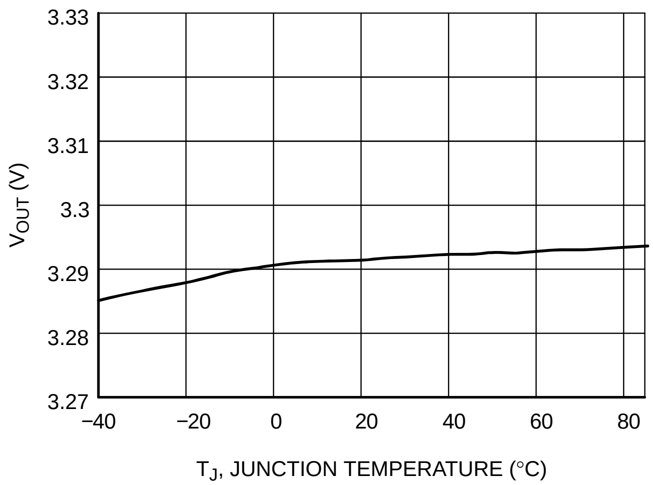


Figure 10. Output Voltage vs. Temperature, 3.3 V Version

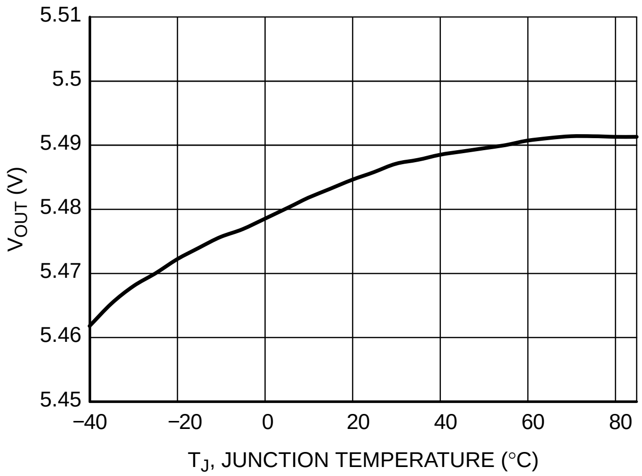


Figure 11. Output Voltage vs. Temperature, 5.5 V Version

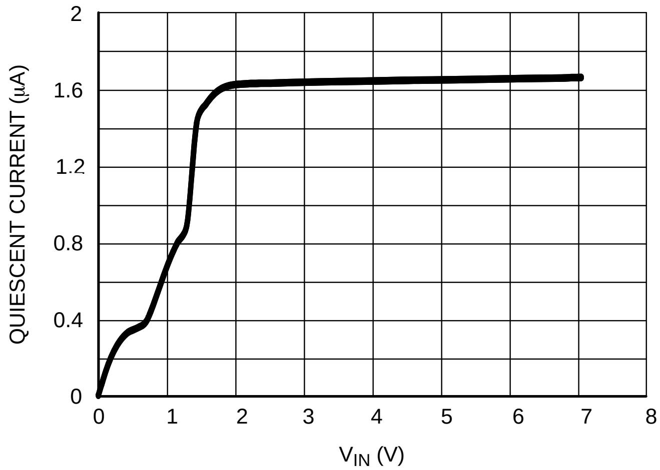


Figure 12. Quiescent Current vs. Input Voltage, 1.2 V Version

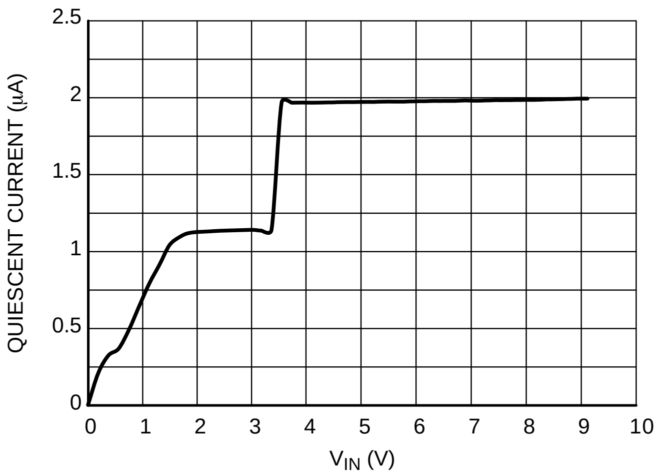


Figure 13. Quiescent Current vs. Input Voltage, 3.3 V Version

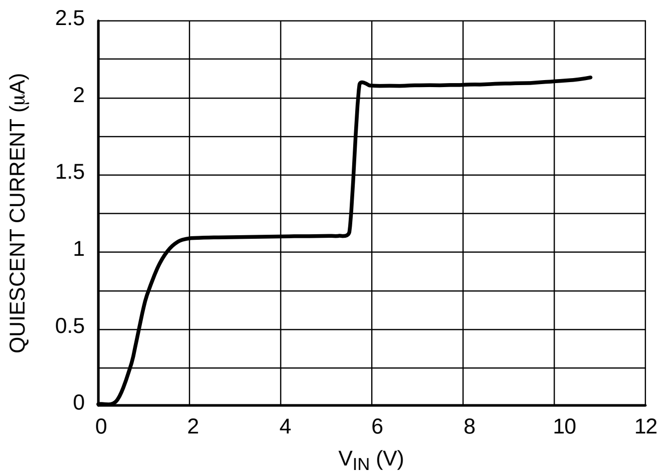


Figure 14. Quiescent Current vs. Input Voltage, 5.5 V Version

TYPICAL CHARACTERISTICS

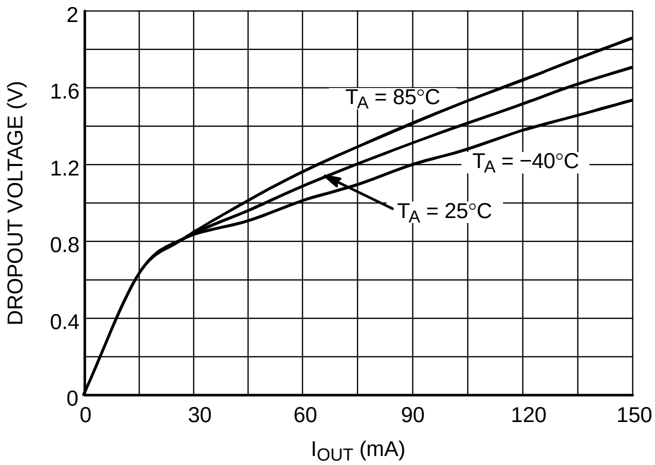


Figure 15. Dropout Voltage vs. Output Current, 1.2 V Version

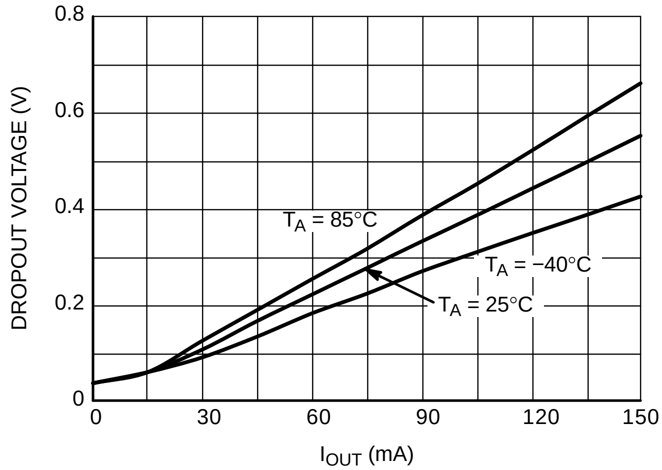


Figure 16. Dropout Voltage vs. Output Current, 3.3 V Version

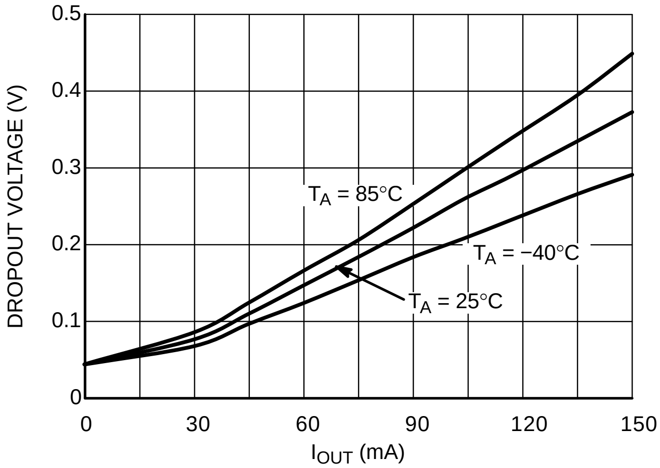


Figure 17. Dropout Voltage vs. Output Current, 5.5 V Version

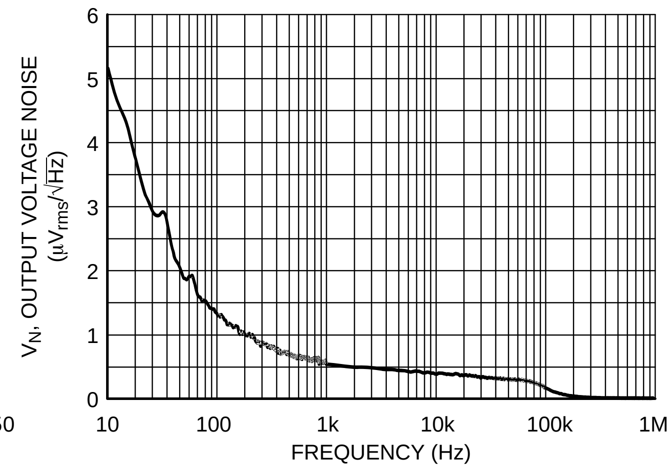


Figure 18. Output Voltage Noise, 1.2 V Version, V_{IN} = 2.5 V, I_{OUT} = 30 mA, C_{in} = C_{out} = 0.1 μF

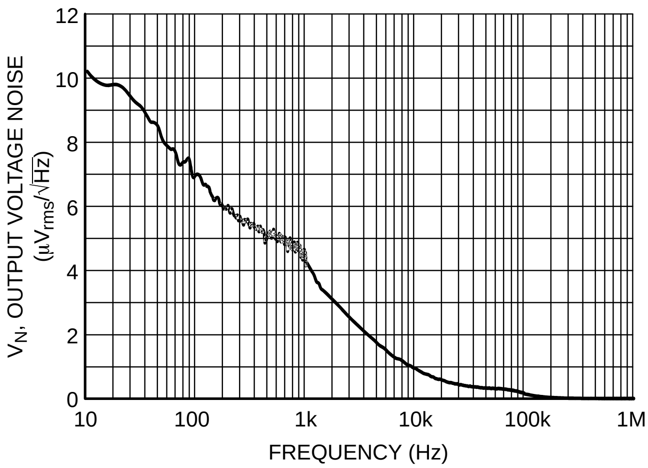


Figure 19. Output Voltage Noise, 3.3 V Version, V_{IN} = 4.3 V, I_{OUT} = 30 mA, C_{in} = C_{out} = 0.1 μF

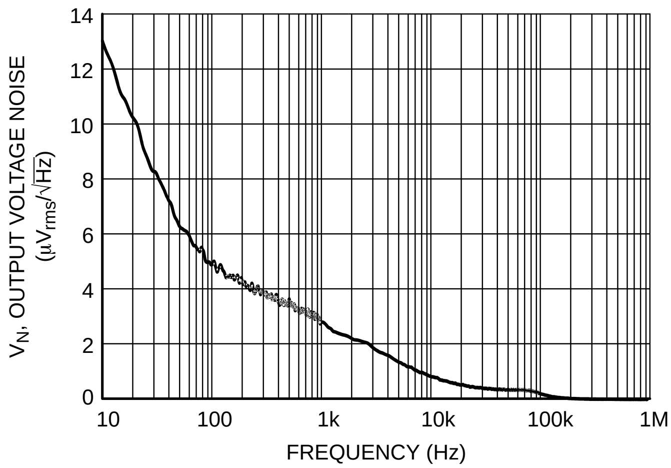


Figure 20. Output Voltage Noise, 5.5 V Version, V_{IN} = 6.5 V, I_{OUT} = 30 mA, C_{in} = C_{out} = 0.1 μF

TYPICAL CHARACTERISTICS

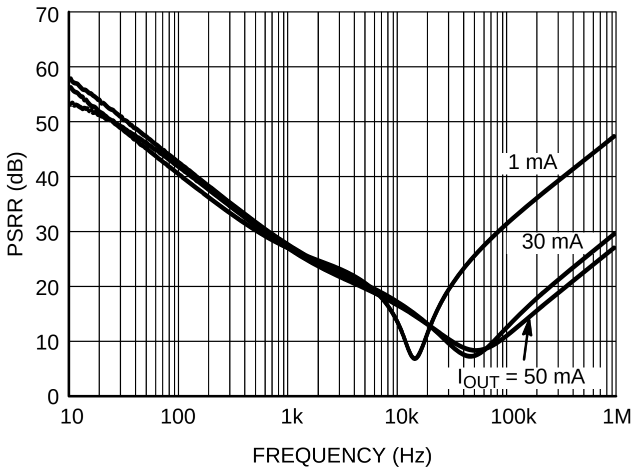


Figure 21. PSRR vs. Frequency, 1.2 V Version

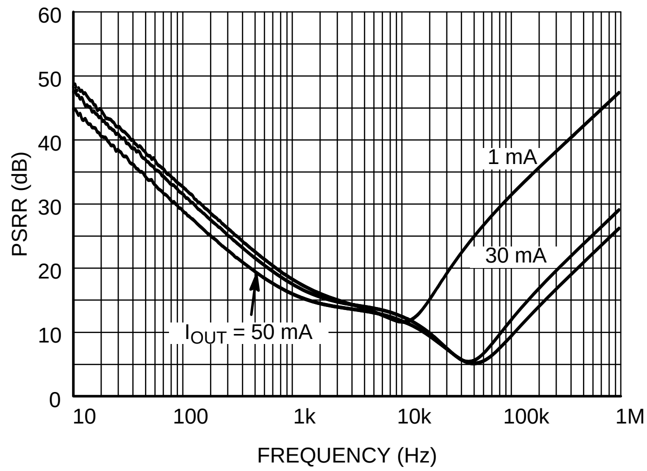


Figure 22. PSRR vs. Frequency, 3.3 V Version

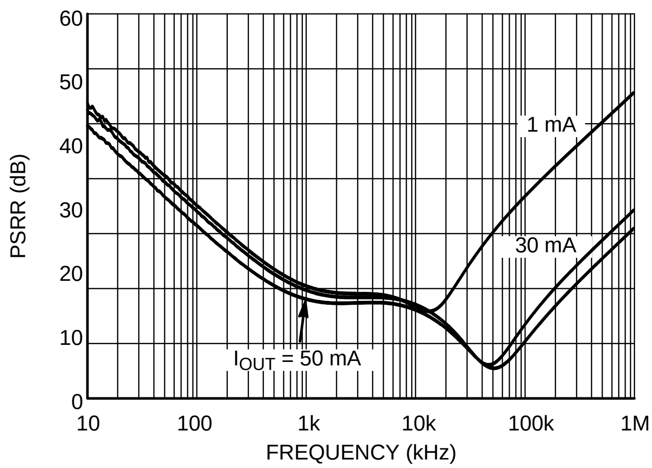


Figure 23. PSRR vs. Frequency, 5.5 V Version

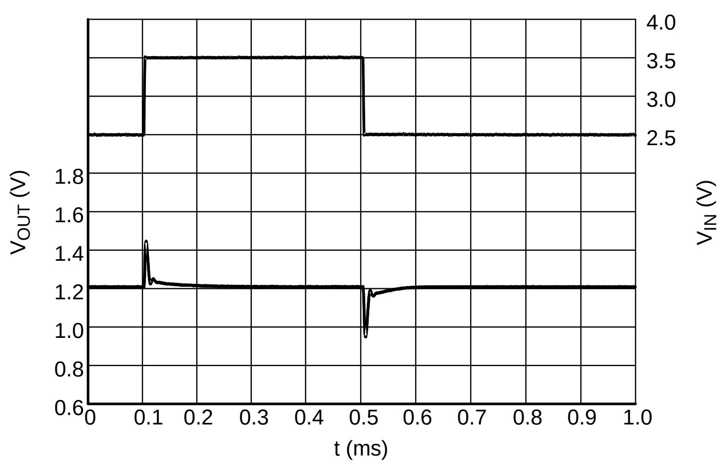


Figure 24. Line Transients, 1.2 V Version, I_{OUT} = 1 mA

TYPICAL CHARACTERISTICS

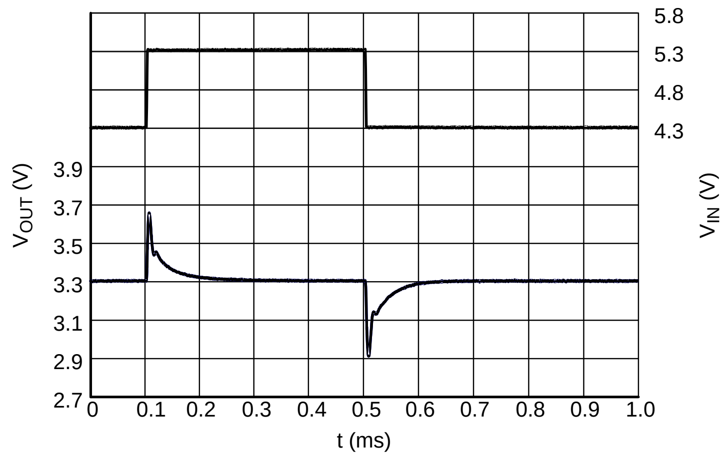


Figure 25. Line Transients, 3.3 V Version, I_{OUT} = 1 mA

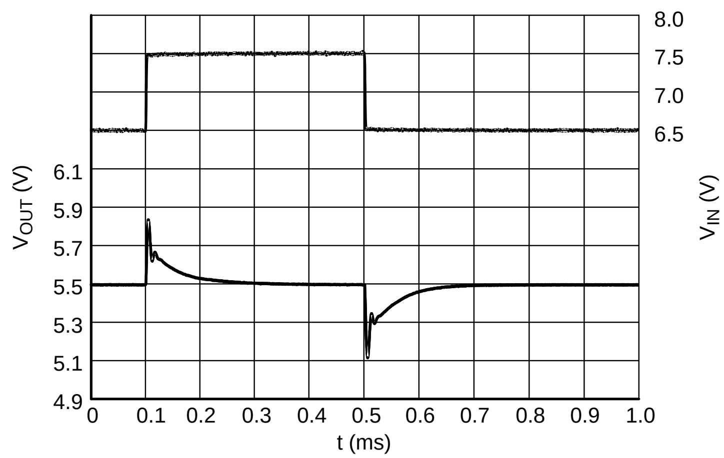


Figure 26. Line Transients, 5.5 V Version, I_{OUT} = 1 mA

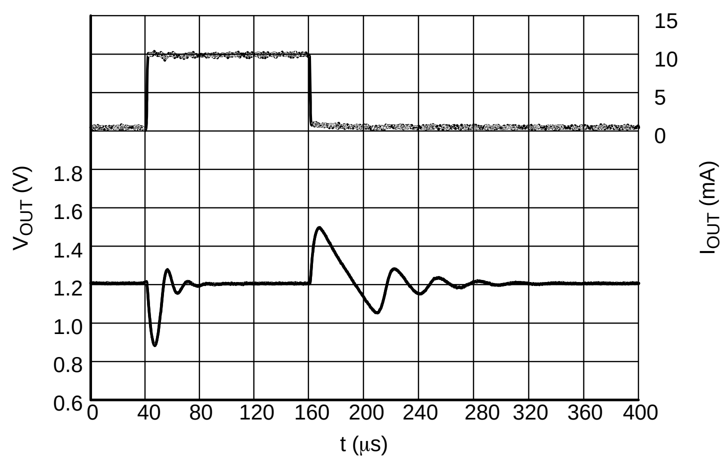


Figure 27. Load Transients, 1.2 V Version, Load Step 1 mA to 10 mA, V_{IN} = 2.5 V

TYPICAL CHARACTERISTICS

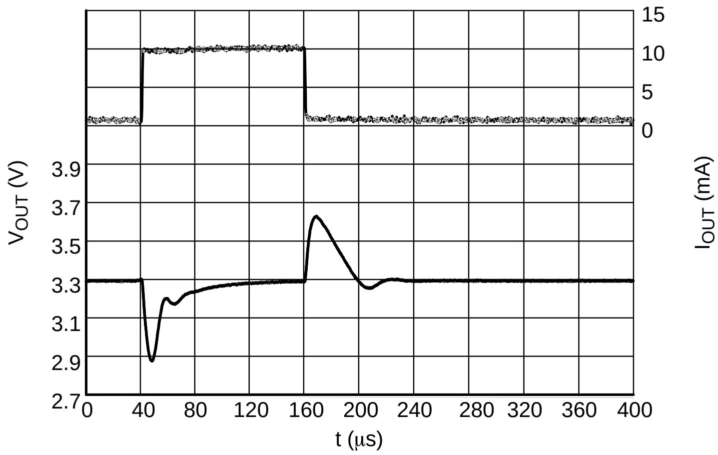


Figure 28. Load Transients, 3.3 V Version, Load Step 1 mA to 10 mA, V_{IN} = 4.3 V

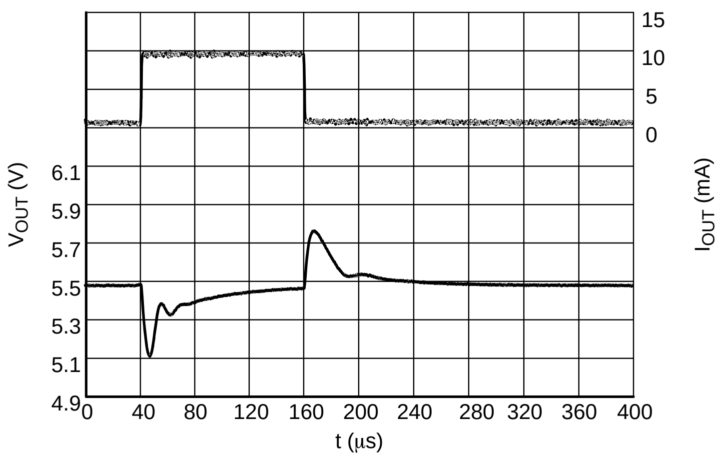


Figure 29. Load Transients, 5.5 V Version, Load Step 1 mA to 10 mA, V_{IN} = 6.5 V

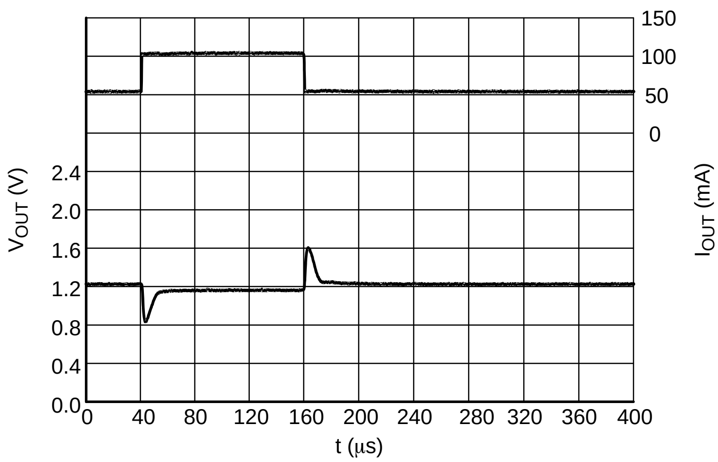


Figure 30. Load Transients, 1.2 V Version, Load Step 50 mA to 100 mA, V_{IN} = 2.5 V

TYPICAL CHARACTERISTICS

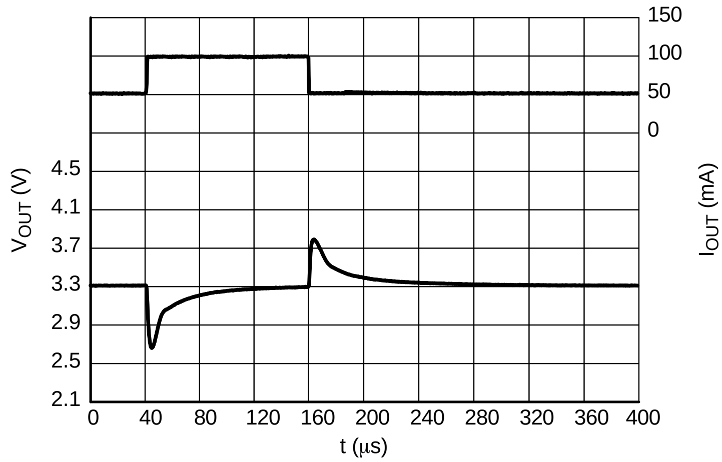


Figure 31. Load Transients, 3.3 V Version, Load Step 50 mA to 100 mA, V_{IN} = 4.3 V

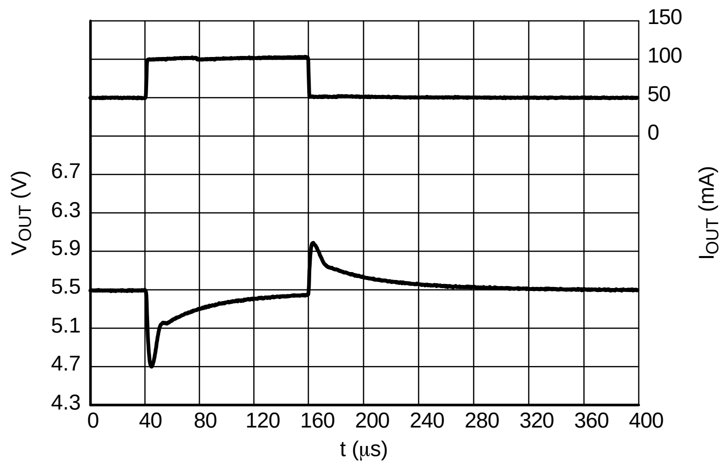


Figure 32. Load Transients, 5.5 V Version, Load Step 50 mA to 100 mA, V_{IN} = 6.5 V

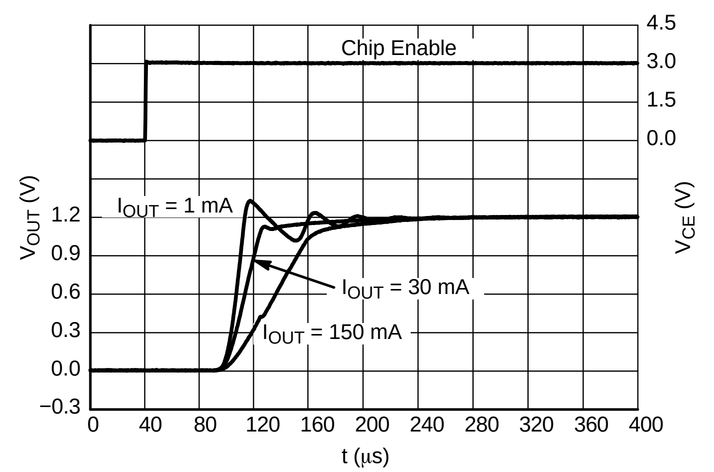


Figure 33. Turn−on Behavior, 1.2 Version, V_{IN} = 3 V

TYPICAL CHARACTERISTICS

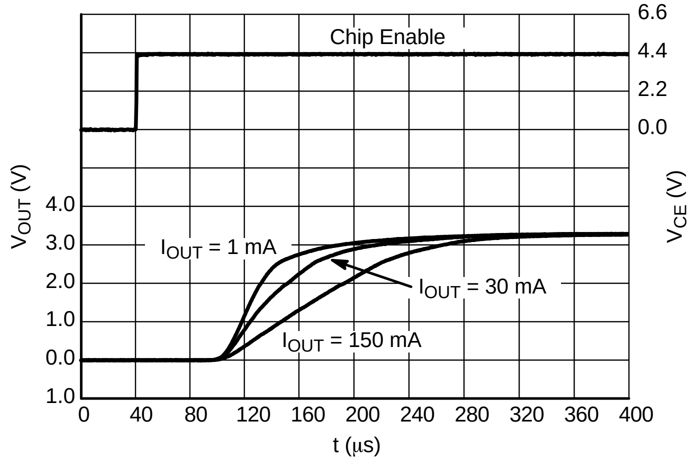


Figure 34. Turn−on Behavior, 3.3 Version, V_{IN} = 4.3 V

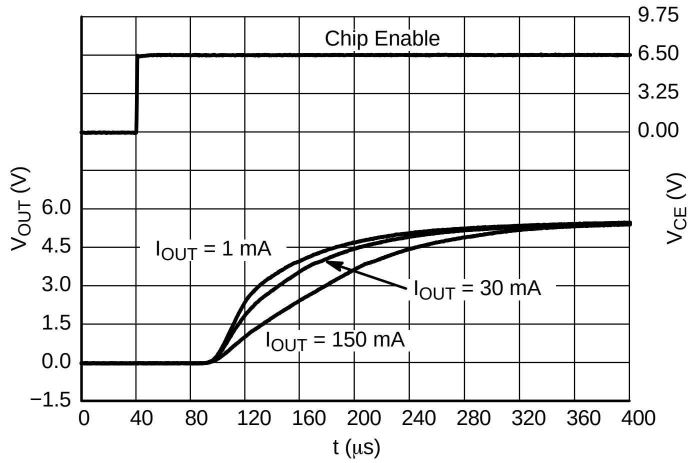


Figure 35. Turn−on Behavior, 5.5 Version, V_{IN} = 6.5 V

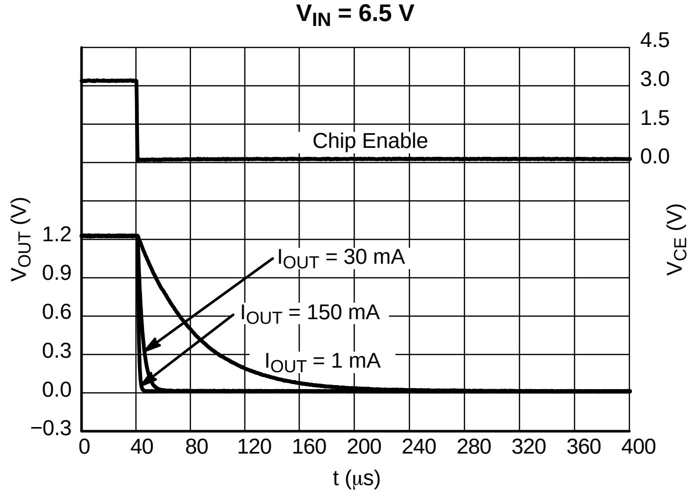


Figure 36. Turn−off Behavior, 1.2 Version, V_{IN} = 3 V

TYPICAL CHARACTERISTICS

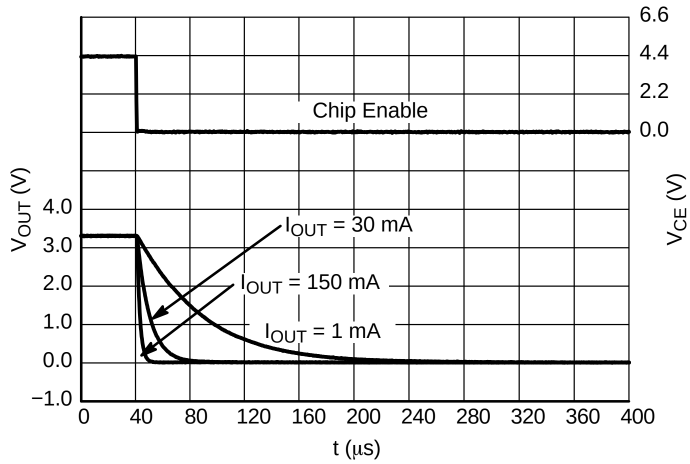


Figure 37. Turn−off Behavior, 3.3 Version, V_{IN} = 4.3 V

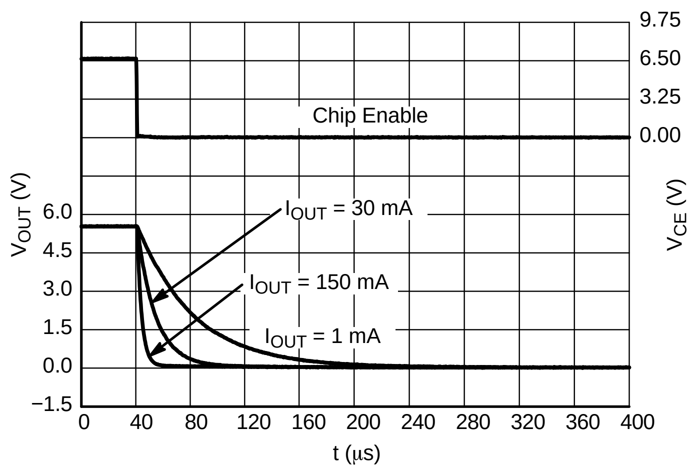


Figure 38. Turn−off Behavior, 5.5 Version, V_{IN} = 6.5 V

APPLICATION INFORMATION

A typical application circuit for NCP4624 series is shown in the Figure 39.

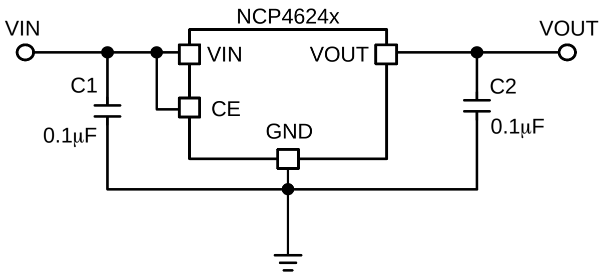


Figure 39. Typical Application Schematic

Input Decoupling Capacitor (C1)

A 100 nF ceramic input decoupling capacitor should be connected as close as possible to the input and ground pin of the NCP4624. Higher values and lower ESR improves line transient response.

Output Decoupling Capacitor (C2)

A 100 nF ceramic output decoupling capacitor is sufficient to achieve stable operation of the IC. If tantalum capacitor is used, and its ESR is high, the loop oscillation may result. The capacitor should be connected as close as possible to the output and ground pin. Larger values and lower ESR improves dynamic parameters.

Enable Operation

The enable pin CE may be used for turning the regulator on and off. The IC is switched on when a high level voltage is applied to the CE pin. The enable pin has an internal pull down current source which assure off state of LDO in case the CE pin will stay floating. If the enable function is not needed connect CE pin to VIN.

The D version of the NCP4624 includes a transistor between VOUT and GND that is used for faster discharging of the output capacitor. This function is activated when the IC goes into disable mode.

Thermal Consideration

As a power across the IC increase, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and also the ambient temperature affect the rate of temperature increase for the part. When the device has good thermal conductivity through the PCB the junction temperature will be relatively low in high power dissipation applications.

Reverse Current Protection Circuit

Internal Reverse Current Circuitry stops the reverse current from VOUT pin to GND pin and VIN pin when V_{OUT} goes higher than V_{IN} voltage or V_{SET} voltage. V_{SET} means voltage given by voltage version. The parasitic diode of PMOS pass device is internally switched to reverse direction before V_{IN} becomes lower than V_{OUT}. The operation coverage of the Reverse Current Protection Circuit is $V_{OUT} > 1.5$ V. In order to avoid unstable behavior a hysteresis is created by different threshold of detecting voltage V_{REV_DET} and releasing voltage V_{REV_REL}. See Figures 40 and 41 for details of configuration.

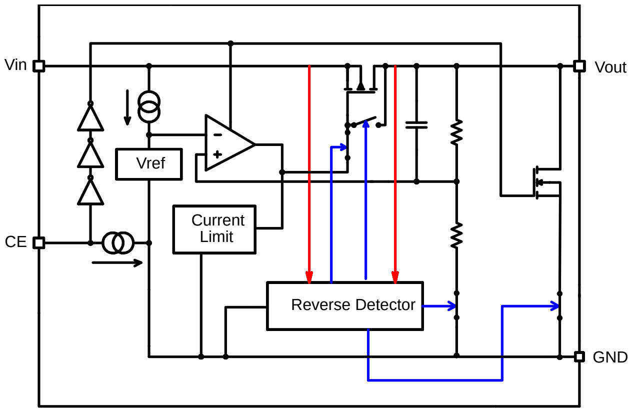


Figure 40. Normal Operating Mode

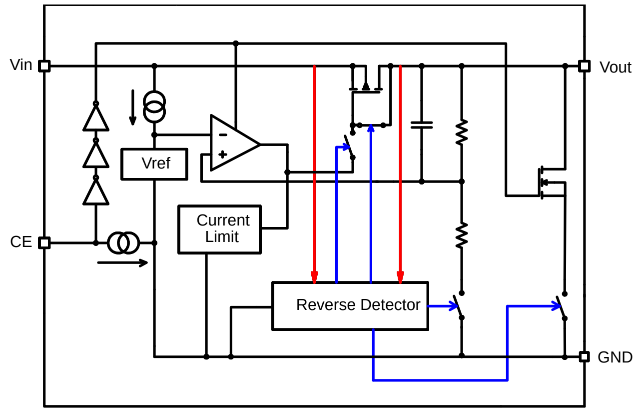


Figure 41. Reverse Current Protection Mode

ESR versus Output Current

When using the NCP4624 devices, consider the following points:

- The relation between Output Current I_{OUT} and ESR of the output capacitor are shown below in Figures 42, 43 and 44.
- The conditions when the device performs stable operation are marked as the hatched area in the charts.

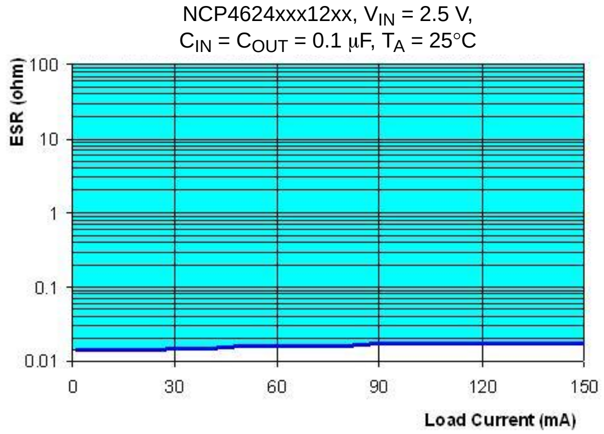


Figure 42. ESR vs. Load Current

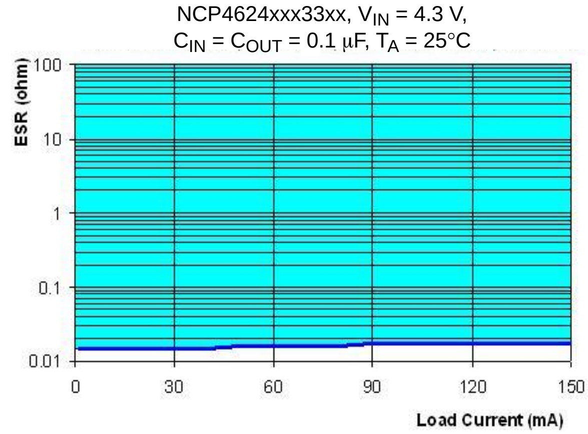


Figure 43. ESR vs. Load Current

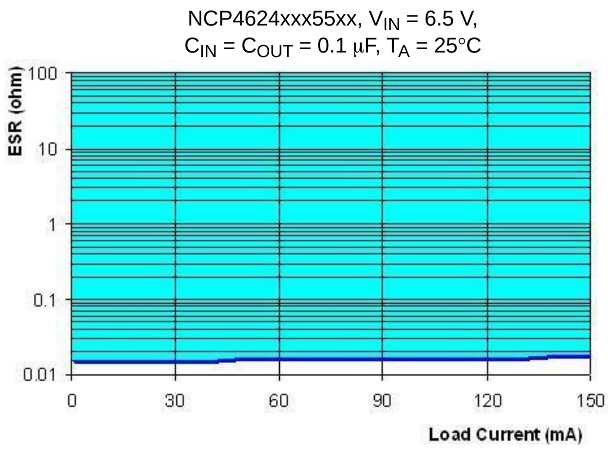


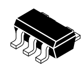
Figure 44. ESR vs. Load Current

ORDERING INFORMATION

Device	Marking	Nominal Output Voltage	Feature	Package	Shipping
NCP4624DMU12TCG	5A	1.2 V	Enable High, Auto discharge	UDFN4 (Pb−Free)	10000 / Tape & Reel
NCP4624DMU30TCG	5X	3.0 V	Enable High, Auto discharge	UDFN4 (Pb−Free)	10000 / Tape & Reel
NCP4624DMU33TCG	6A	3.3 V	Enable High, Auto discharge	UDFN4 (Pb−Free)	10000 / Tape & Reel
NCP4624DMU50TCG	6T	5.0 V	Enable High, Auto discharge	UDFN4 (Pb−Free)	10000 / Tape & Reel
NCP4624DSN12T1G	F12	1.2 V	Enable High, Auto discharge	SOT−23−5 (Pb−Free)	3000 / Tape & Reel
NCP4624DSN18T1G	F18	1.8 V	Enable High, Auto discharge	SOT−23−5 (Pb−Free)	3000 / Tape & Reel
NCP4624DSN33T1G	F33	3.3 V	Enable High, Auto discharge	SOT−23−5 (Pb−Free)	3000 / Tape & Reel
NCP4624DSN50T1G	F50	5.0 V	Enable High, Auto discharge	SOT−23−5 (Pb−Free)	3000 / Tape & Reel
NCP4624DSQ12T1G	AT12	1.2. V	Enable High, Auto discharge	SC−88A (Pb−Free)	3000 / Tape & Reel
NCP4624DSQ33T1G	AT33	3.3 V	Enable High, Auto discharge	SC−88A (Pb−Free)	3000 / Tape & Reel

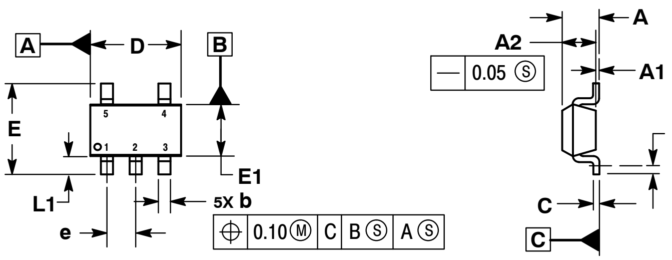
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SOT−23 5−LEAD
CASE 1212−01
ISSUE A



SCALE 2:1

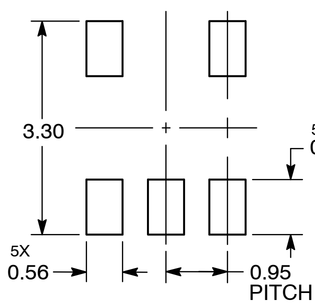
DATE 28 JAN 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DATUM C IS THE SEATING PLANE.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	---	1.45
A1	0.00	0.10
A2	1.00	1.30
b	0.30	0.50
c	0.10	0.25
D	2.70	3.10
E	2.50	3.10
E1	1.50	1.80
e	0.95 BSC	
L	0.20	---
L1	0.45	0.75

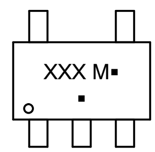
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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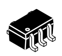
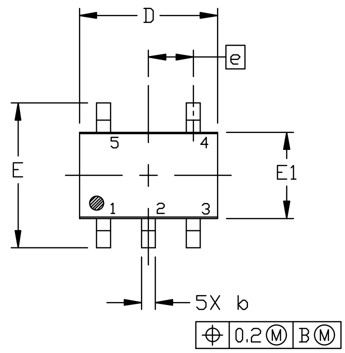
DESCRIPTION:	SOT−23 5−LEAD	PAGE 1 OF 1

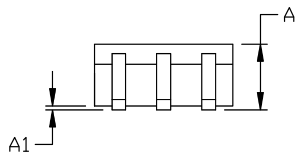


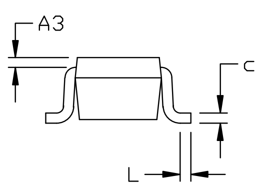
SCALE 2:1

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE M

DATE 11 APR 2023

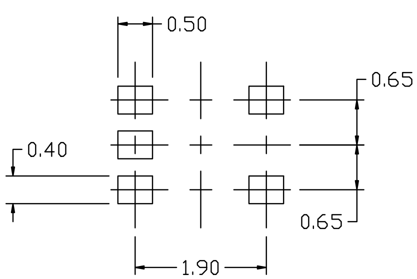






NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

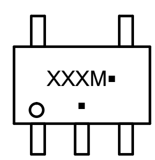
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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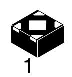
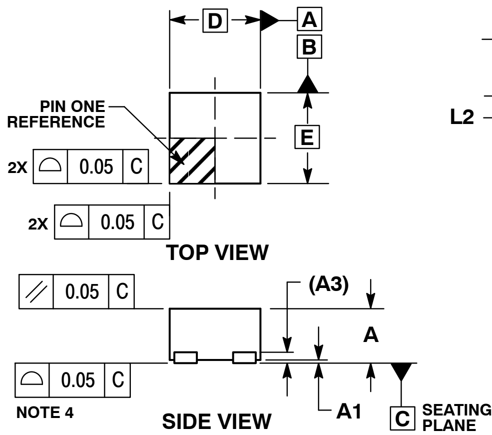
DESCRIPTION:	SC−88A (SC−70−5/SOT−353)	PAGE 1 OF 1



SCALE 4:1

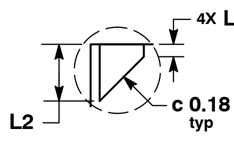
UDFN4 1.0x1.0, 0.65P
CASE 517BR−01
ISSUE O

DATE 27 OCT 2010

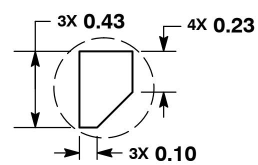


TOP VIEW

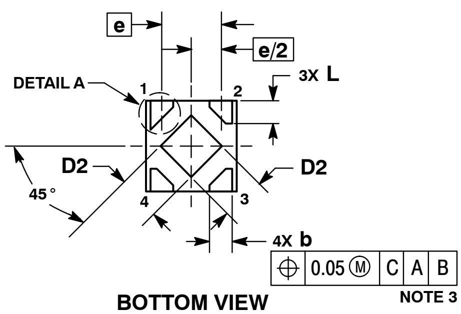
SIDE VIEW



DETAIL A



DETAIL B

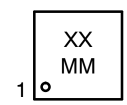


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.60
A1	0.00	0.05
A3	0.10 REF	
b	0.20	0.30
D	1.00 BSC	
D2	0.43	0.53
E	1.00 BSC	
e	0.65 BSC	
L	0.20	0.30
L2	0.27	0.37
L3	0.02	0.12

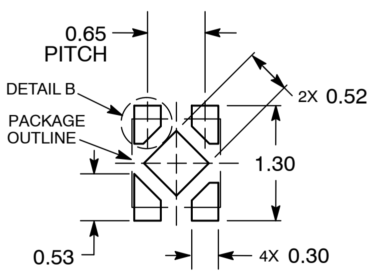
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
MM = Date Code

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	UDFN4, 1.0X1.0, 0.65P	PAGE 1 OF 1

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