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NCP4623

150 mA, Wide Input Voltage Range, Low Dropout Regulator

The NCP4623 is a CMOS Linear Voltage Regulator designed for wide input voltage range. The maximum operating input voltage is up to 24 V with a minimum voltage starting from 2 V. The Chip Enable (CE) pin allows the device to lower standby current to 0.1 μA typ. The NCP4623 features many protections for any current or thermal sensitive devices with current fold−back protection, thermal shutdown protection, and peak and short current protection. This device is available in adjustable and fixed voltage output in 0.1 V steps. They are available in very thin XDFN6 1.6x1.6x0.4 mm in size and the very popular SOT23−5 and SOT89−5 packages. Please contact your local sales office for additional output voltage options.

Features

- Maximum Operating Input Voltage: 24 V
- Output Voltage Range: 2.5 V to 12.0 V (available in 0.1 V steps)
  2.5 V to 24.0 V (adjustable version)
- Output Voltage Accuracy: ±2.0%
- Supply Current: 5 μA
- Stable with Ceramic Capacitors: 1 μF or more
- Current Fold Back Protection
- Peak and Short Current Protection
- Thermal Shutdown Protection
- Available in XDFN6 1.6 x 1.6 mm, SOT23−5, SOT89−5 Packages
- These are Pb−Free Devices

Typical Applications

- Battery−powered Equipment
- Networking and Communication Equipment
- Cameras, DVRs, STB and Camcorders
- Home Appliances

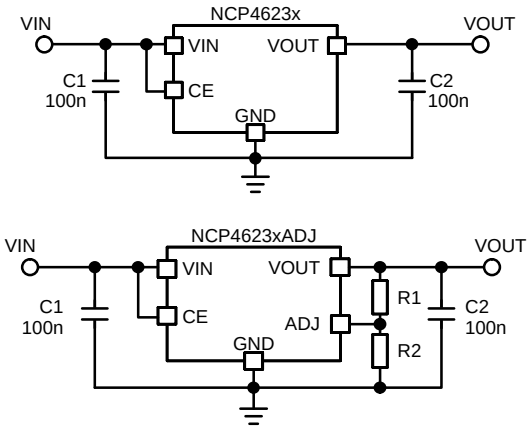

Figure 1. Typical Application Schematics

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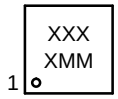
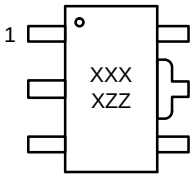
MARKING DIAGRAMS

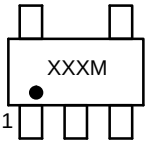
XDFN6
CASE 711AC



SOT−89 5
CASE 528AB



SOT−23−5
CASE 1212



XXX, XXXX = Specific Device Code
M, MM = Date Code
ZZ = Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

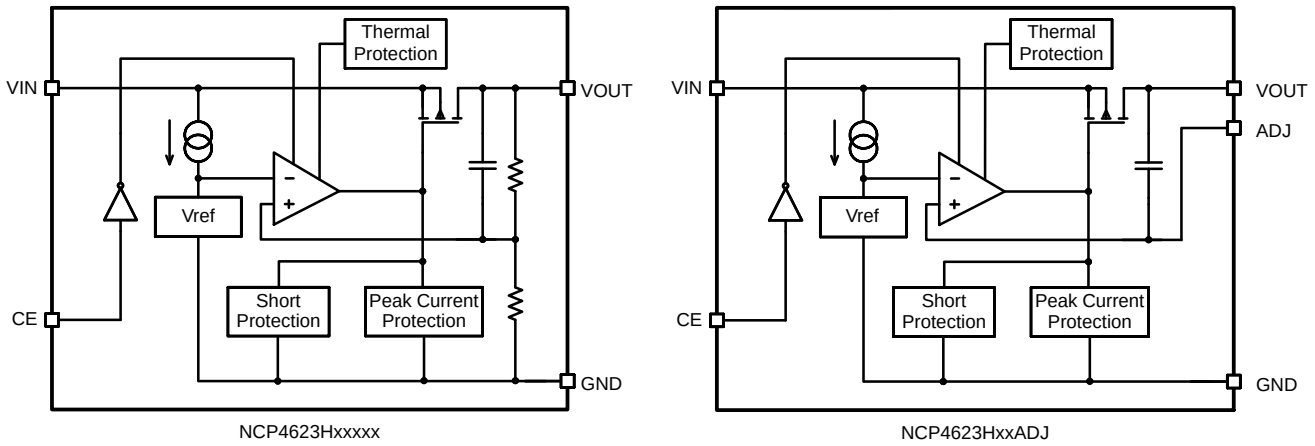


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. XDFN (Note 1)	Pin No. SOT89−5	Pin No. SOT23	Pin Name	Description
3	1	1	V_{OUT}	Output pin
6	2	2	GND	Ground
4	3	5	CE	Chip enable pin (Active “H”)
1	5	3	V_{IN}	Input pin
5	4	4	NC/ADJ	No connection (non ADJ versions) / Reference Voltage of Adjustable Output Pin (ADJ versions)
2	−	−	NC	No connection

1. Tab is connected to GND. Tab should be connected to GND, but leaving it unconnected is also acceptable

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 2)	V_{IN}	26.0	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} + 0.3	V
Chip Enable Input	V_{CE}	−0.3 to V_{IN} + 0.3	V
Reference Input Voltage	V_{ADJ}	−0.3 to V_{IN} + 0.3	V
Output Current	I_{OUT}	250	mA
Power Dissipation XDFN6−1616	P_D	640	mW
Power Dissipation SOT89−5		900	
Power Dissipation SOT23−5		420	
Junction Temperature	T_J	−40 to 150	°C
Operation Temperature	T_A	−40 to 85	°C
Storage Temperature	T_{STG}	−55 to 125	°C
ESD Capability, Human Body Model (Note 3)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 3)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, XDFN6 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	156	°C/W
Thermal Characteristics, SOT23−5 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	238	°C/W
Thermal Characteristics, SOT89−5 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	111	°C/W

ELECTRICAL CHARACTERISTICS NCP4623Hxxxx, $C_{IN} = C_{OUT} = 0.1\ \mu F$, $T_A = +25°C$

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	2		24	V
Output Voltage	$V_{IN} = V_{OUT(NOM)} + 2.0$ V, $I_{OUT} = 20$ mA		V_{OUT}	x0.98		x1.02	V
Output Voltage Temp. Coefficient	$V_{IN} = V_{OUT(NOM)} + 2.0$ V, $I_{OUT} = 20$ mA, $-40°C \le T_A \le 105ºC$		$\Delta V_{OUT}/\Delta T_A$		±100		ppm/°C
Line Regulation	$V_{OUT(NOM)} + 1\ V \le V_{IN} \le 24$ V, $I_{OUT} = 20$ mA		$Line_{Reg}$		0.05	0.20	%/V
Load Regulation	$V_{IN} = V_{OUT(NOM)} + 2.0$ V, $I_{OUT} = 1$ mA to 40 mA	$2.5\ V \le V_{OUT} \le 3.0$ V	$Load_{Reg}$		20	50	mV
		$3.1\ V \le V_{OUT} \le 5.0$ V			30	75	
		$5.1\ V \le V_{OUT} \le 12.0$ V			40	115	
Dropout Voltage	$I_{OUT} = 20$ mA	$2.5\ V \le V_{OUT} \le 7.0$ V	V_{DO}		0.20	0.40	V
		$7.1\ V \le V_{OUT} \le 10.0$ V			0.25	0.50	
		$10.1\ V \le V_{OUT} \le 12.0$ V			0.30	0.55	
Output Current	$V_{IN} = V_{OUT(NOM)} + 2.0$ V	$2.5\ V \le V_{OUT} \le 2.9$ V	I_{OUT}	140			mA
		$3.0\ V \le V_{OUT} \le 12.0$ V		150			

ELECTRICAL CHARACTERISTICS NCP4623Hxxxx, C_{IN} = C_{OUT} = 0.1 μF, T_A = +25°C

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Short Current Limit	V_{OUT} = 0 V	I_{SC}		45		mA
Quiescent Current	V_{IN} = $V_{OUT(NOM)}$ + 2.0 V, V_{CE} = V_{IN}	I_Q		5	10	μA
Standby Current	V_{IN} = 24 V, V_{CE} = 0 V	I_{STB}		0.1	1.0	μA
CE Pin Threshold Voltage	CE Input Voltage “H”	V_{CEH}	2.1		V_{IN}	V
	CE Input Voltage “L”	V_{CEL}	0		0.3	
Power Supply Rejection Ratio	V_{OUT} = 3.3V V, V_{IN} = 5.3 V, ΔV_{IN} = 0.2 V_{pk-pk}, I_{OUT} = 30 mA, f = 1 kHz	PSRR		35		dB
Output Noise Voltage	f = 10 Hz to 100 kHz, V_{OUT} = 3.3 V, V_{IN} = 5.3 V, I_{OUT} = 30 mA	V_N		90		μV_{rms}
Thermal Shutdown Temperature		T_{SD}		150		°C
Thermal Shutdown Release Temperature		T_{SR}		125		°C

ELECTRICAL CHARACTERISTICS NCP4623HxxxADJ, V_{ADJ} = V_{OUT}, C_{IN} = C_{OUT} = 0.1 μF, T_A = +25°C

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage		V_{IN}	2		24	V
Output Voltage	V_{IN} = $V_{OUT(NOM)}$ + 2.0 V, I_{OUT} = 20 mA	V_{OUT}	2.45	2.50	2.55	V
Output Voltage Temp. Coefficient	V_{IN} = $V_{OUT(NOM)}$ + 2.0 V, I_{OUT} = 20 mA, −40°C ≤ T_A ≤ 105ºC	$\Delta V_{OUT}/\Delta T_A$		±100		ppm/°C
Line Regulation	$V_{OUT(NOM)}$ + 1 V ≤ V_{IN} ≤ 24 V, I_{OUT} = 20 mA	$Line_{Reg}$		0.05	0.20	%/V
Load Regulation	V_{IN} = $V_{OUT(NOM)}$ + 2.0 V, I_{OUT} = 1 mA to 40 mA	$Load_{Reg}$		20	50	mV
Dropout Voltage	I_{OUT} = 20 mA	V_{DO}		0.20	0.40	V
Output Current	V_{IN} = $V_{OUT(NOM)}$ + 2.0 V	I_{OUT}	140			mA
Short Current Limit	V_{OUT} = 0 V	I_{SC}		45		mA
3 Quiescent Current	V_{IN} = $V_{OUT(NOM)}$ + 2.0 V, V_{CE} = V_{IN}	I_Q		5	10	μA
Standby Current	V_{IN} = 24 V, V_{CE} = 0 V	I_{STB}		0.1	1.0	μA
CE Pin Threshold Voltage	CE Input Voltage “H”	V_{CEH}	2.1		V_{IN}	V
	CE Input Voltage “L”	V_{CEL}	0		0.3	
Power Supply Rejection Ratio	V_{IN} = 4.5 V, V_{OUT} = 2.5 V, ΔV_{IN} = 0.2 V_{pk-pk}, I_{OUT} = 30 mA, f = 1 kHz	PSRR		40		dB
Output Noise Voltage	f = 10 Hz to 100 kHz, V_{OUT} = 2.5 V, V_{IN} = 4.5 V, I_{OUT} = 30 mA	V_N		80		μV_{rms}
Thermal Shutdown Temperature		T_{SD}		150		°C
Thermal Shutdown Release Temperature		T_{SR}		125		°C

TYPICAL CHARACTERISTICS

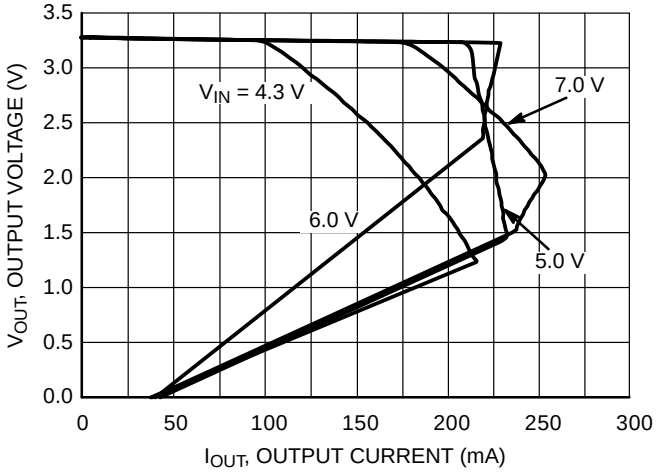


Figure 3. Output Voltage vs. Output Current 3.3 V Version (T_J = 25°C)

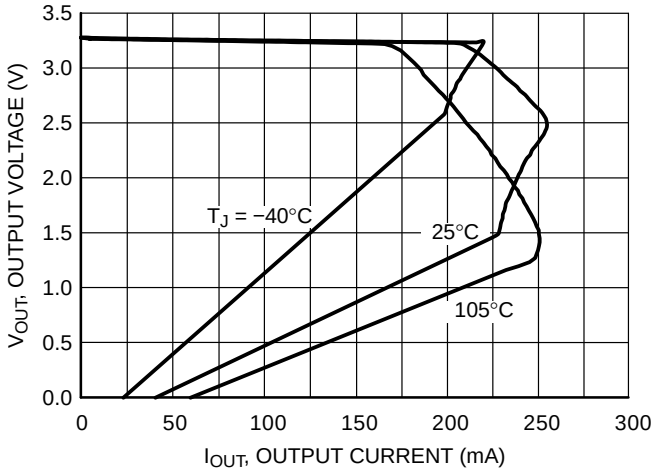


Figure 4. Output Voltage vs. Output Current 3.3 V Version V_{IN} = 5.3 V

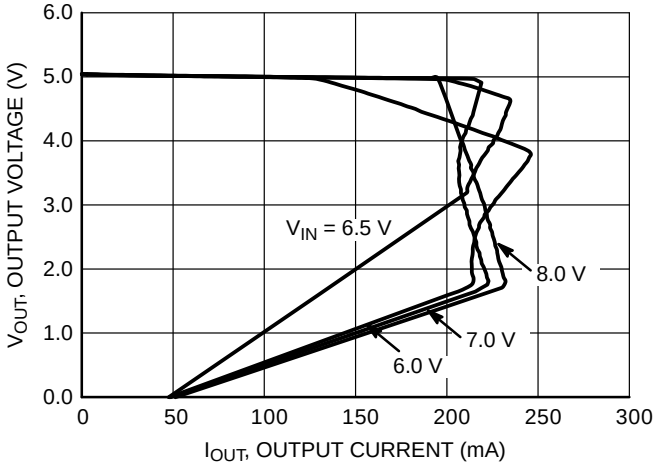


Figure 5. Output Voltage vs. Output Current 5.0 V Version (T_J = 25°C)

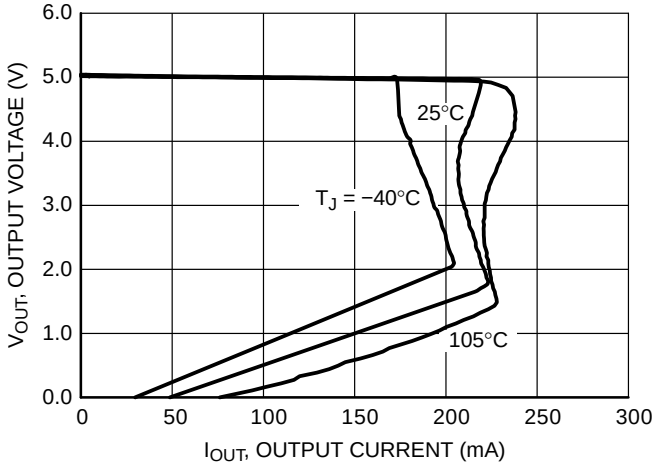


Figure 6. Output Voltage vs. Output Current 5.0 V Version V_{IN} = 7.0 V

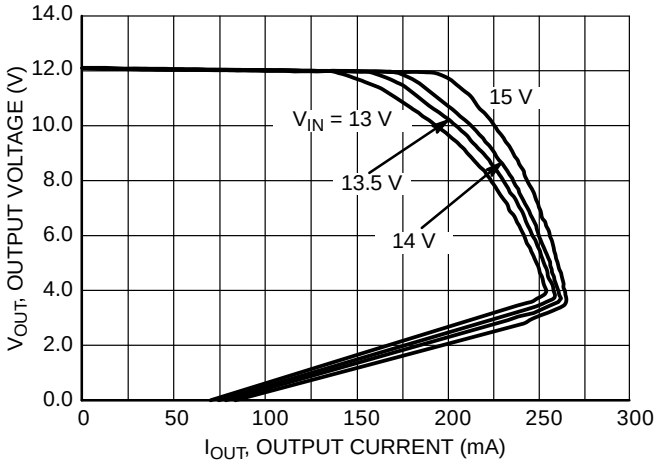


Figure 7. Output Voltage vs. Output Current 12.0 V Version (T_J = 25°C)

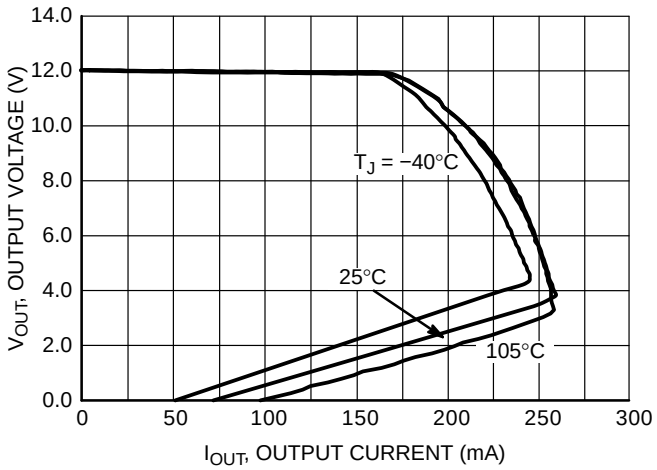


Figure 8. Output Voltage vs. Output Current 12.0 V Version V_{IN} = 14.0 V

TYPICAL CHARACTERISTICS

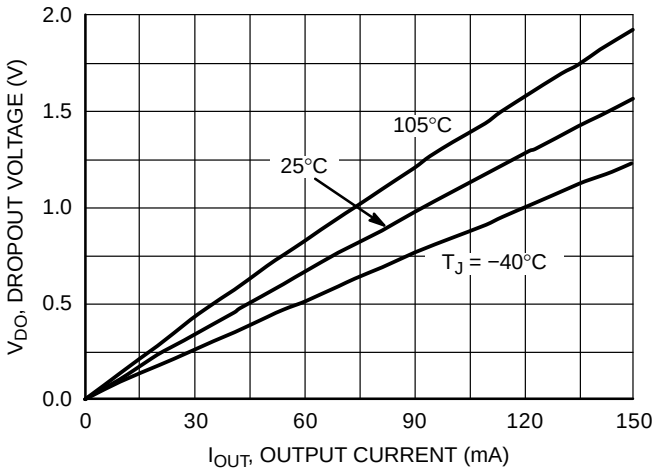


Figure 9. Dropout Voltage vs. Output Current 3.3 V Version

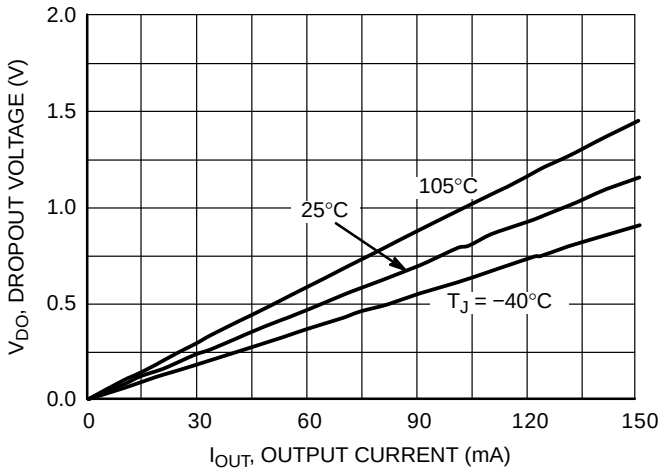


Figure 10. Dropout Voltage vs. Output Current 5.0 V Version

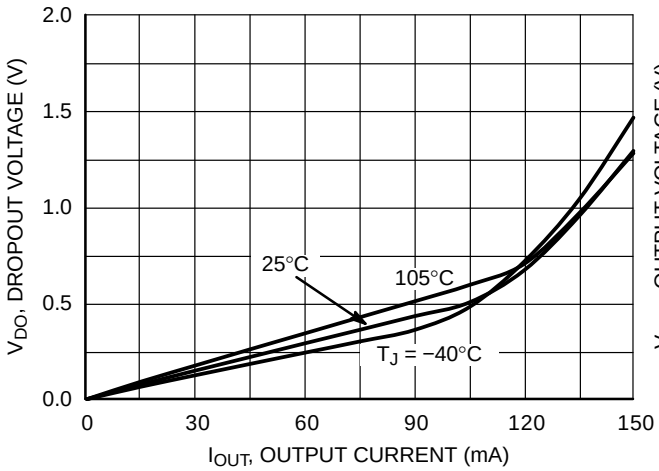


Figure 11. Dropout Voltage vs. Output Current 12.0 V Version

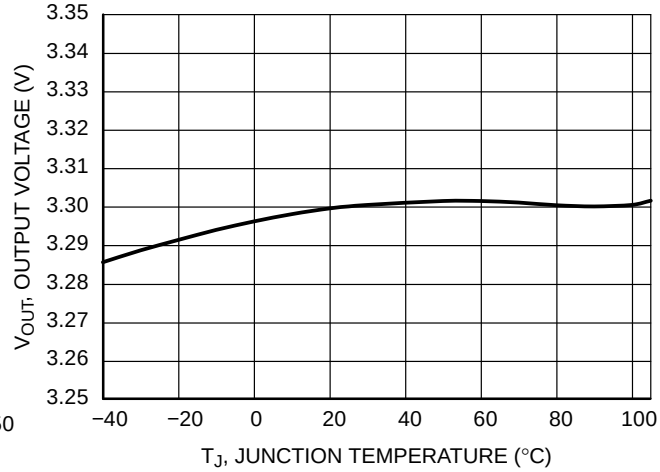


Figure 12. Output Voltage vs. Temperature, 3.3 V Version, V_{IN} = 5.3 V, I_{OUT} = 20 mA

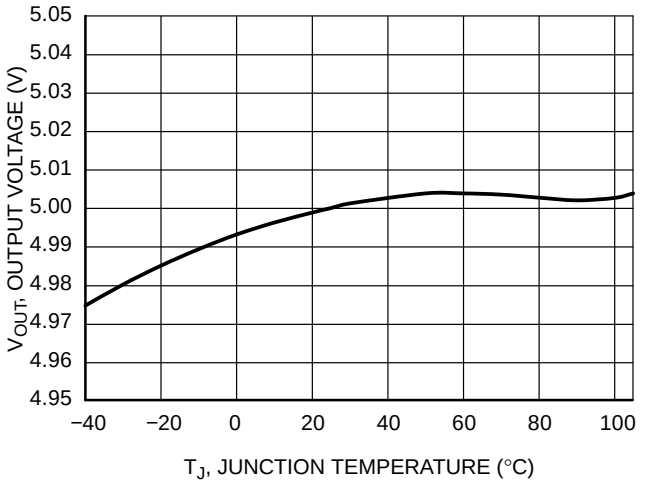


Figure 13. Output Voltage vs. Temperature, 5.0 V Version, V_{IN} = 7.0 V, I_{OUT} = 20 mA

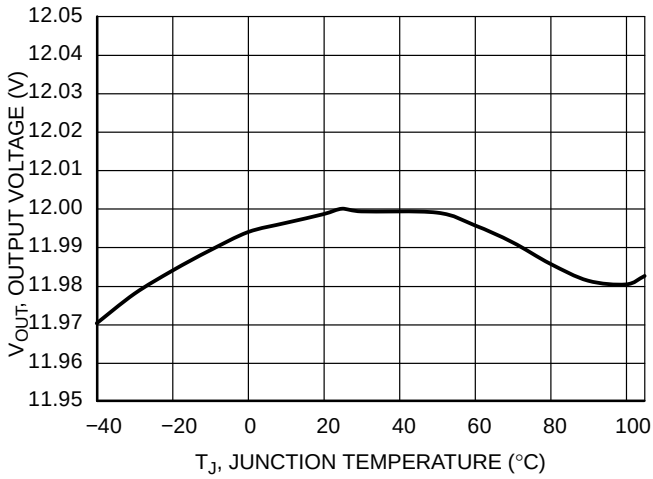


Figure 14. Output Voltage vs. Temperature, 12.0 V Version, V_{IN} = 14.0 V, I_{OUT} = 20 mA

TYPICAL CHARACTERISTICS

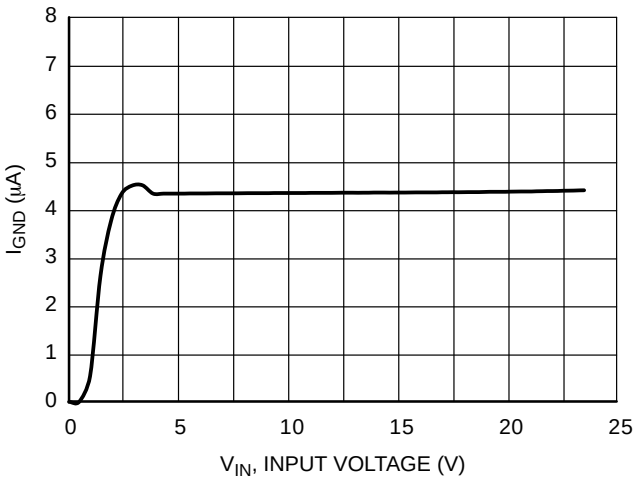


Figure 15. Supply Current vs. Input Voltage, 3.3 V Version

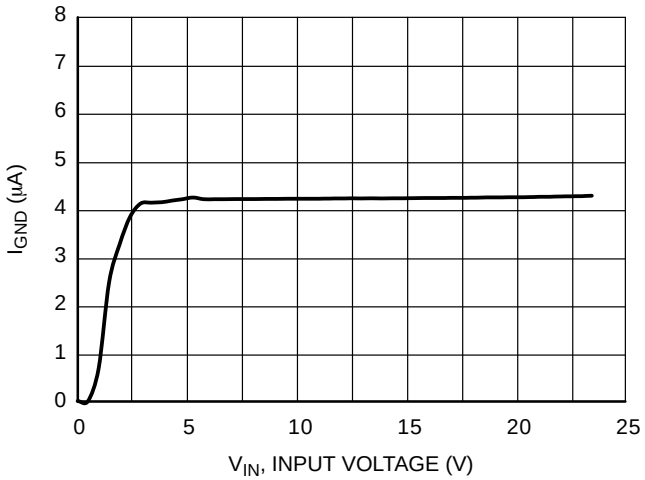


Figure 16. Supply Current vs. Input Voltage, 5.0 V Version

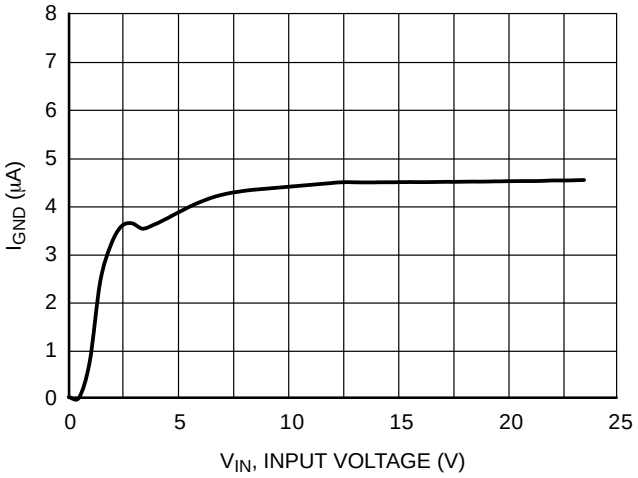


Figure 17. Supply Current vs. Input Voltage, 12.0 V Version

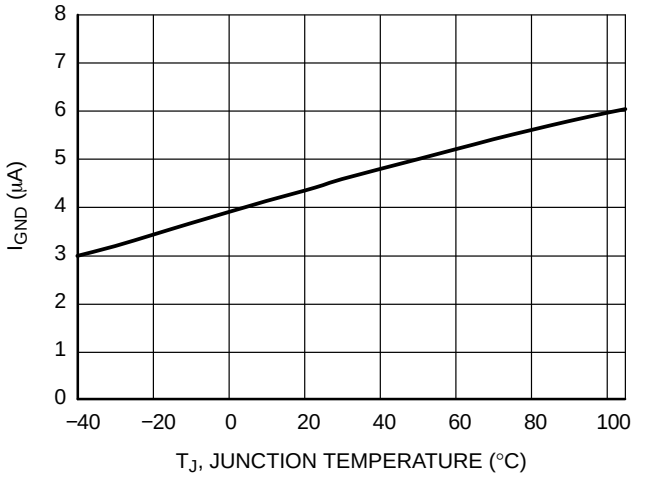


Figure 18. Supply Current vs. Temperature, 3.3 V Version, V_{IN} = 5.3 V

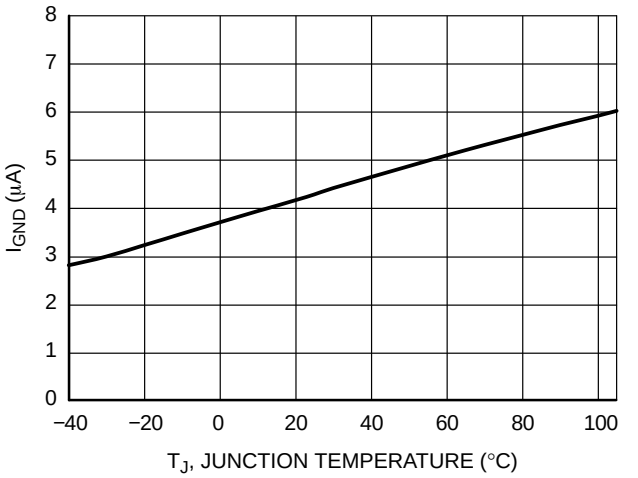


Figure 19. Supply Current vs. Temperature, 5.0 V Version, V_{IN} = 7.0 V

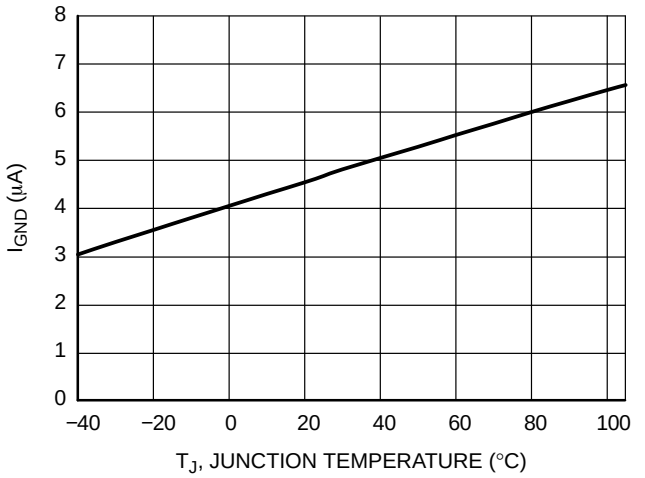


Figure 20. Supply Current vs. Temperature, 12.0 V Version, V_{IN} = 14.0 V

TYPICAL CHARACTERISTICS

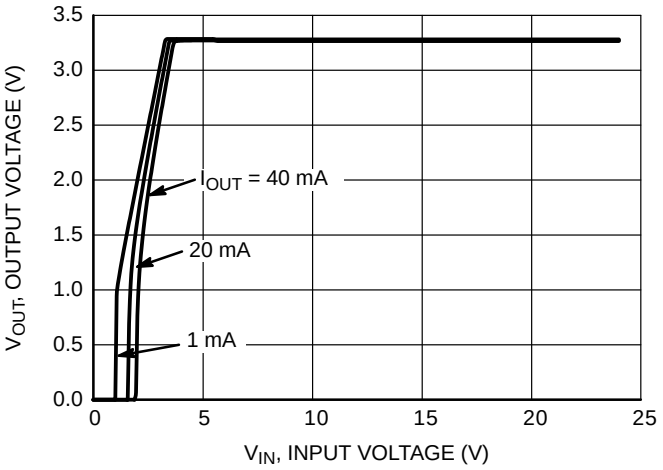


Figure 21. Output Voltage vs. Input Voltage, 3.3 V Version

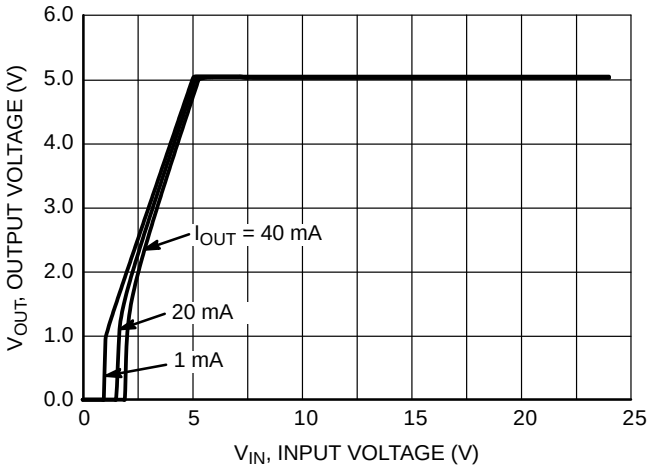


Figure 22. Output Voltage vs. Input Voltage, 5.0 V Version

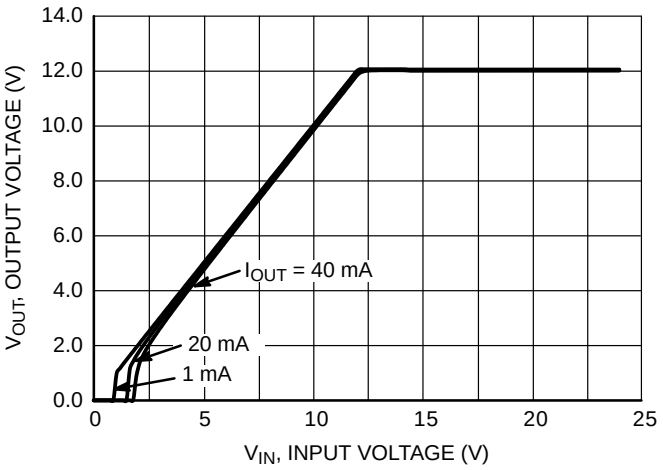


Figure 23. Output Voltage vs. Input Voltage, 12.0 V Version

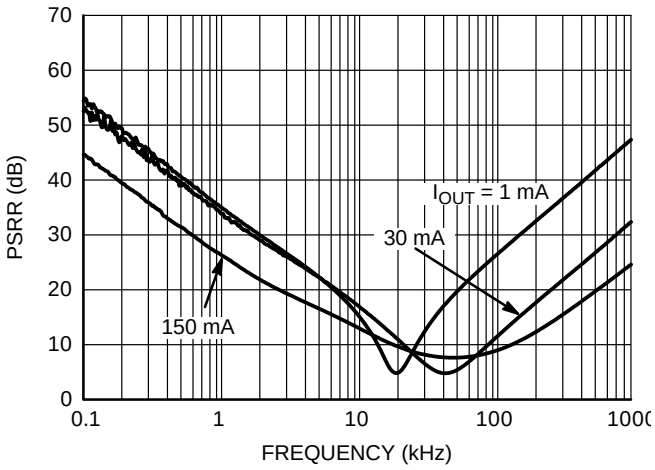


Figure 24. PSRR, 3.3 V Version, V_{IN} = 6.3 V

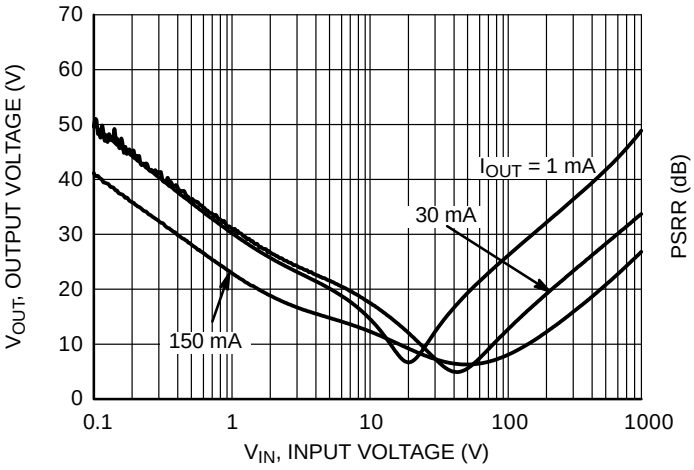


Figure 25. PSRR, 5.0 V Version, V_{IN} = 8.0 V

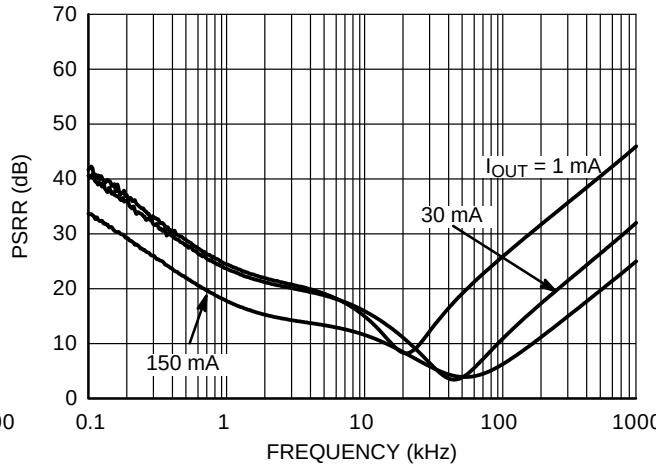


Figure 26. PSRR, 12.0 V Version, V_{IN} = 15.0 V

TYPICAL CHARACTERISTICS

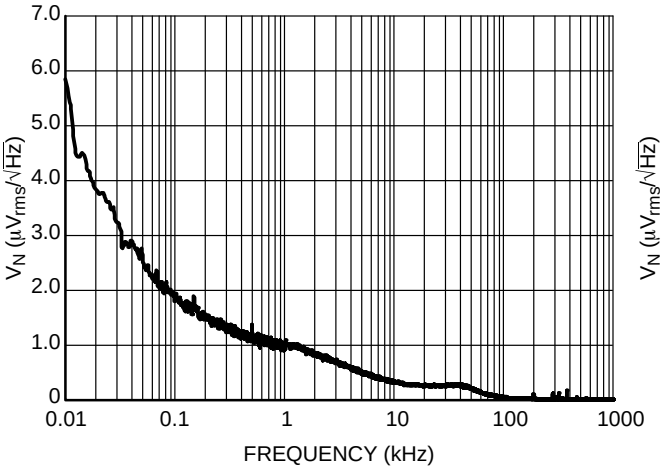


Figure 27. Output Voltage Noise, 3.3 V Version, V_{IN} = 5.3 V, I_{OUT} = 30 mA

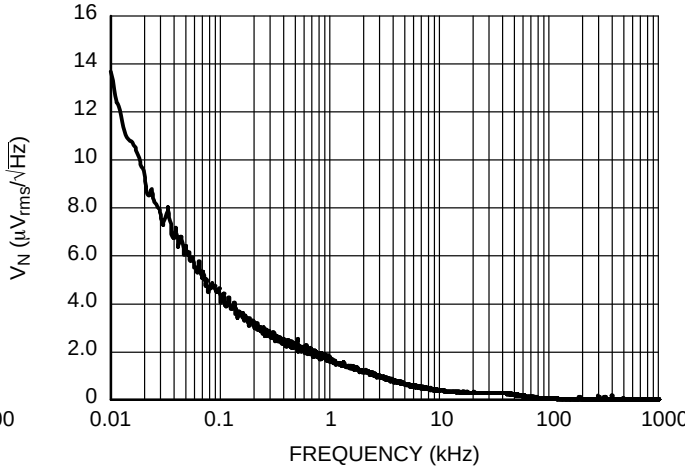


Figure 28. Output Voltage Noise, 5.0 V Version, V_{IN} = 7.0 V, I_{OUT} = 30 mA

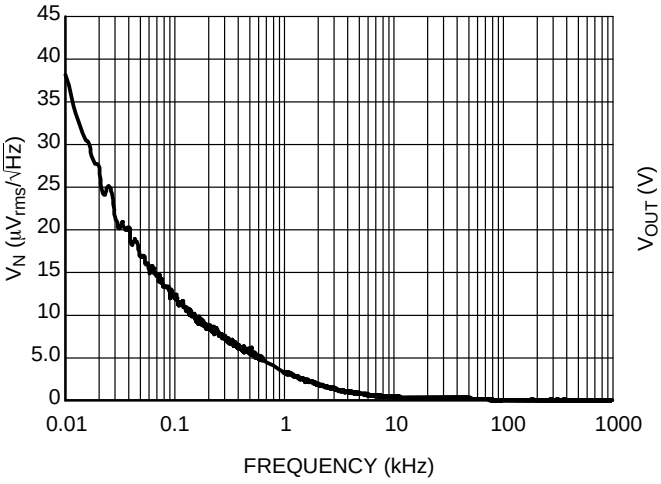


Figure 29. Output Voltage Noise, 12.0 V Version, V_{IN} = 14.0 V, I_{OUT} = 30 mA

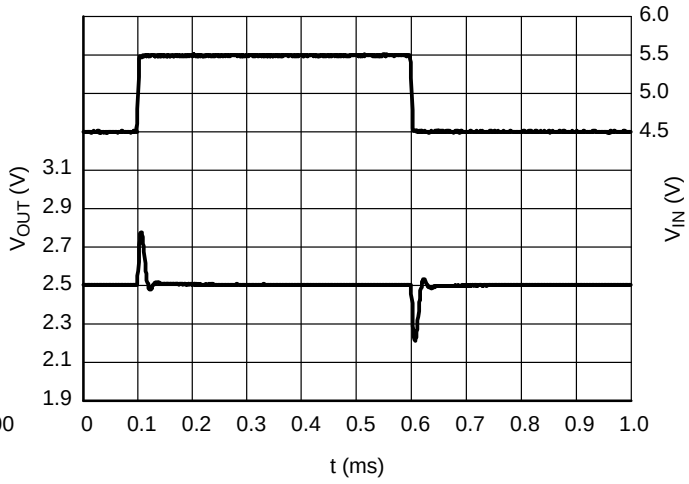


Figure 30. Line Transients, 2.5 V Version, $t_R = t_F$ = 5 μs, I_{OUT} = 30 mA

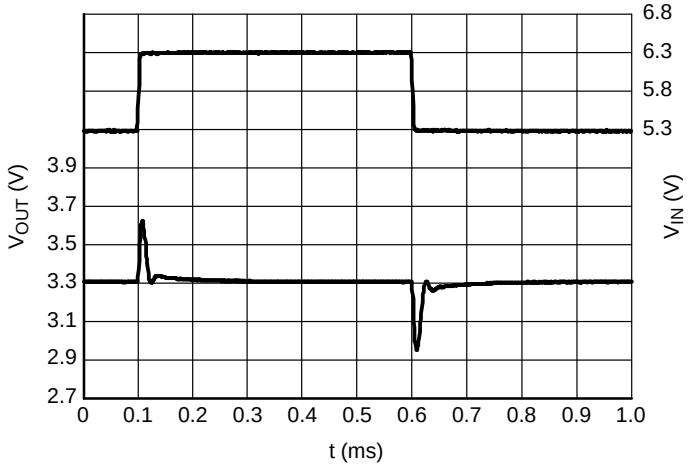


Figure 31. Line Transients, 3.3 V Version, $t_R = t_F$ = 5 μs, I_{OUT} = 30 mA

TYPICAL CHARACTERISTICS

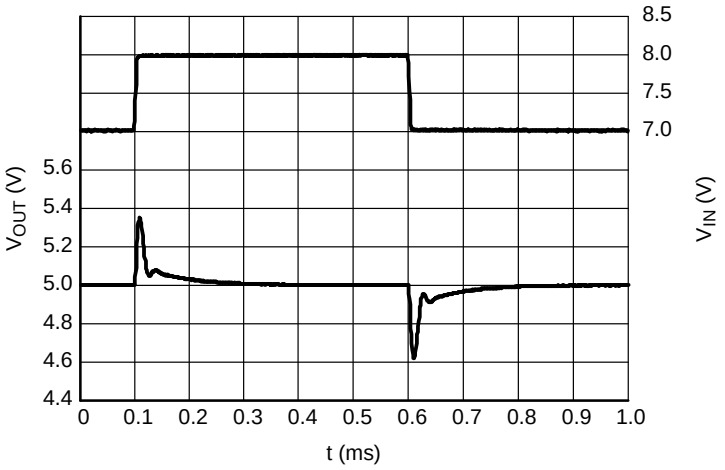


Figure 32. Line Transients, 5.0 V Version, $t_R = t_F = 5$ µs, $I_{OUT} = 30$ mA

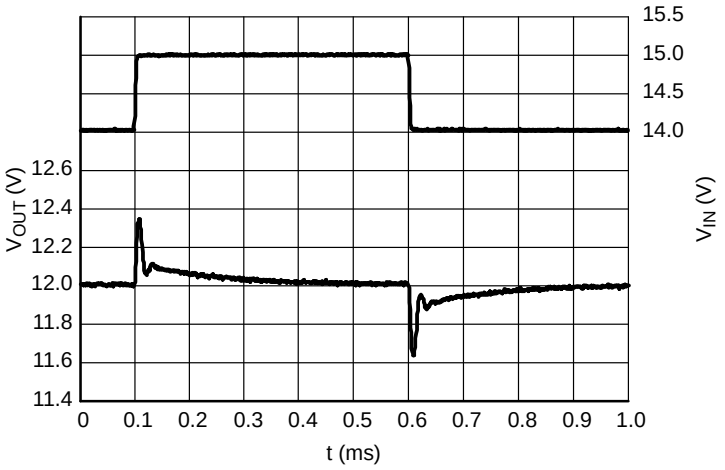
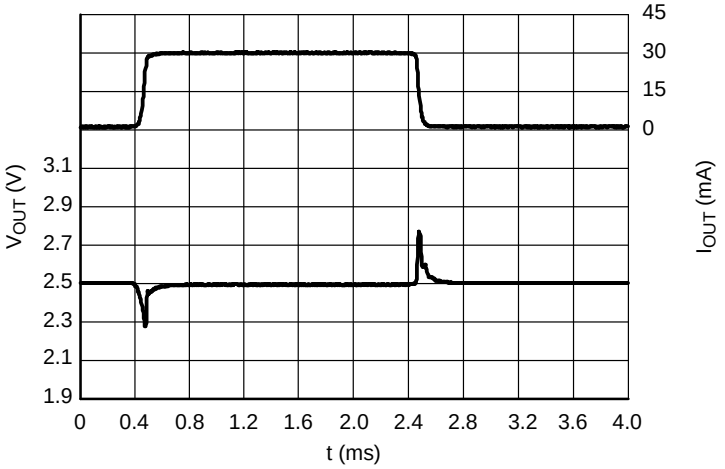


Figure 33. Line Transients, 12.0 V Version, $t_R = t_F = 5$ µs, $I_{OUT} = 30$ mA



Load Transients, 2.5 V Version, $I_{OUT} = 1$ - 30 mA, $t_R = t_F = 50$ µs, $V_{IN} = 4.5$ V

TYPICAL CHARACTERISTICS

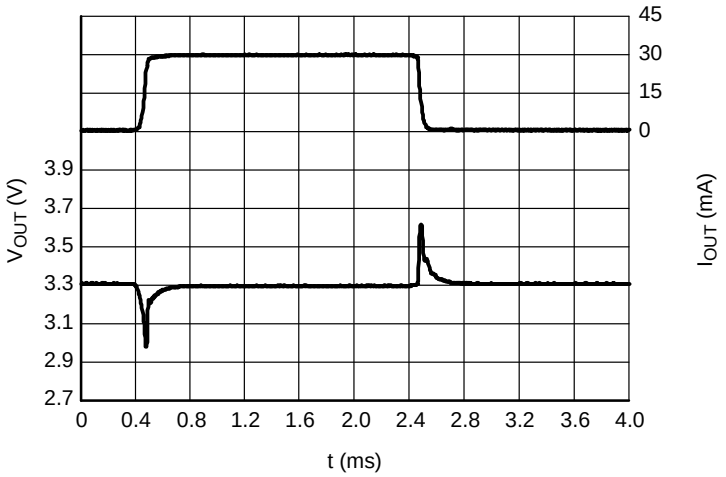


Figure 34 - Load Transients, 3.3 V Version, I_{OUT} = 1 - 30 mA, $t_R = t_F$ = 50 μs, V_{IN} = 5.3 V

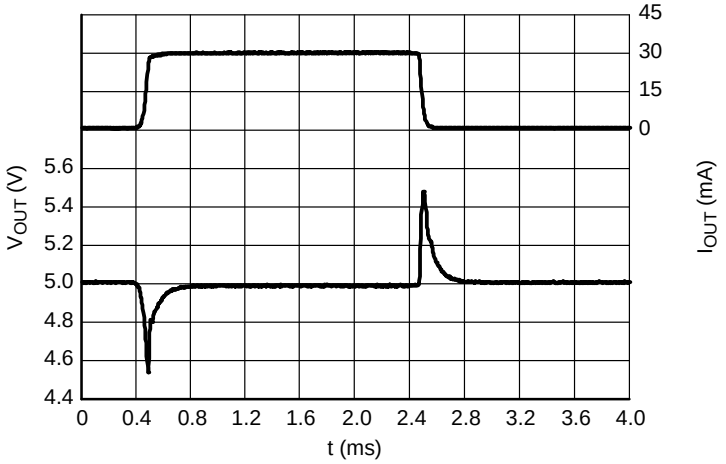


Figure 35. Load Transients, 5.0 V Version, I_{OUT} = 1 − 30 mA, $t_R = t_F$ = 50 μs, V_{IN} = 7.0 V

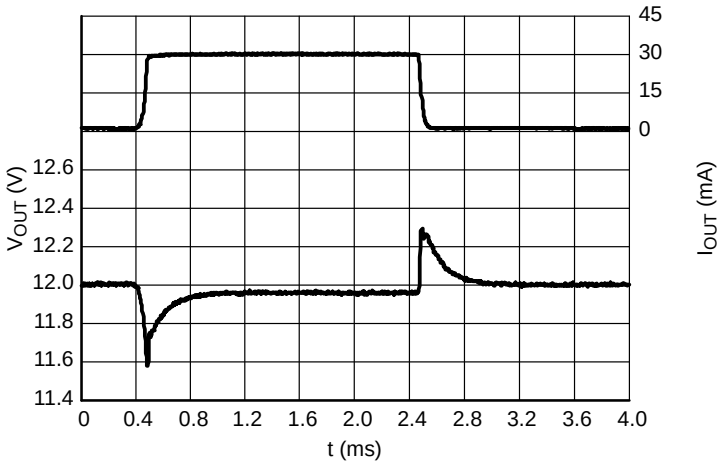


Figure 36. Load Transients, 12.0 V Version, I_{OUT} = 1 − 30 mA, $t_R = t_F$ = 50 μs, V_{IN} = 14.0 V

TYPICAL CHARACTERISTICS

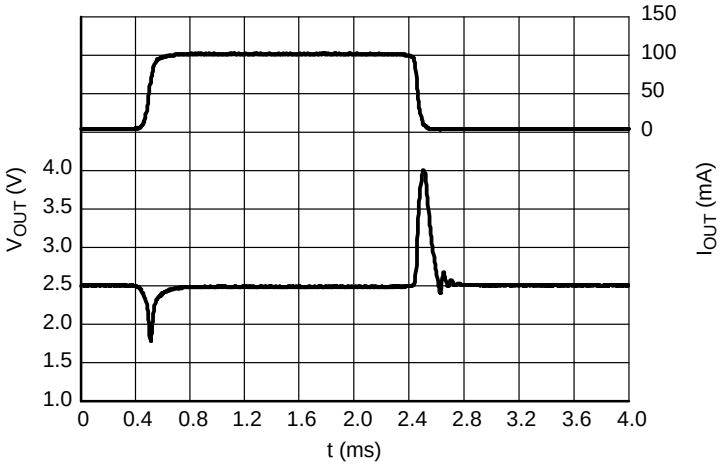


Figure 37. Load Transients, 2.5 V Version, I_{OUT} = 1 − 100 mA, t_R = t_F = 50 μs, V_{IN} = 4.5 V

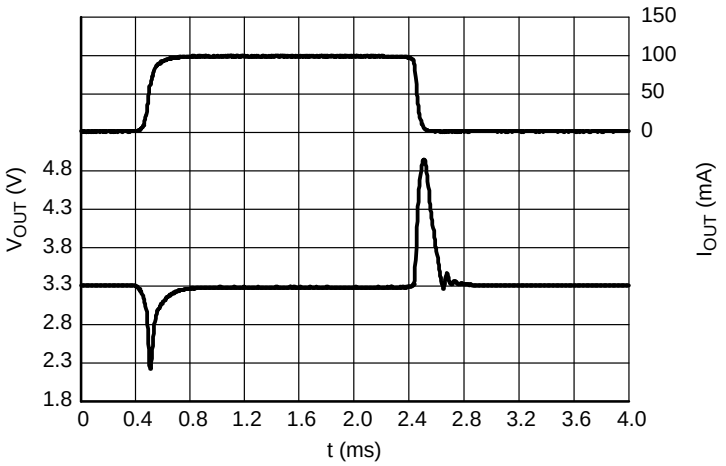


Figure 38. Load Transients, 3.3 V Version, I_{OUT} = 1 − 100 mA, t_R = t_F = 50 μs, V_{IN} = 5.3 V

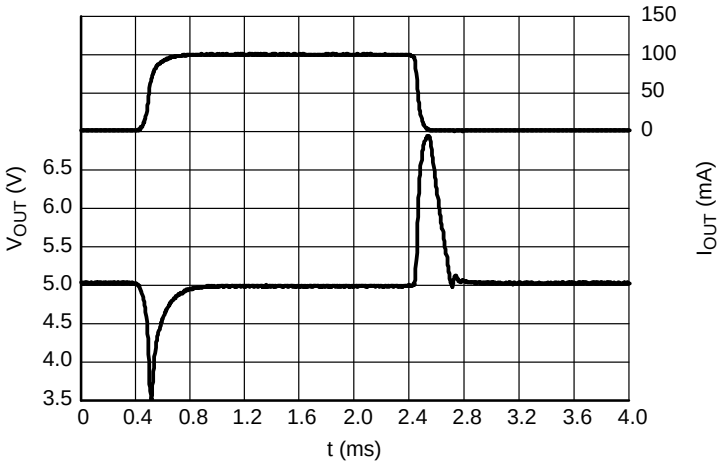


Figure 39. Load Transients, 5.0 V Version, I_{OUT} = 1 − 100 mA, t_R = t_F = 50 μs, V_{IN} = 7.0 V

TYPICAL CHARACTERISTICS

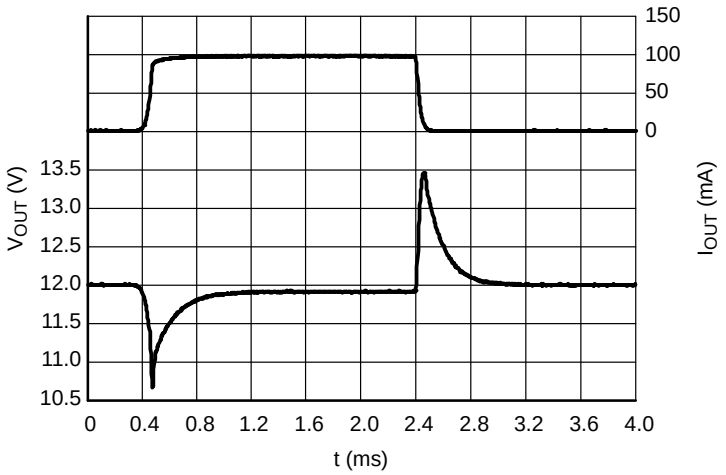


Figure 40. Load Transients, 12.0 V Version, I_{OUT} = 1 − 100 mA, t_R = t_F = 50 µs, V_{IN} = 14.0 V

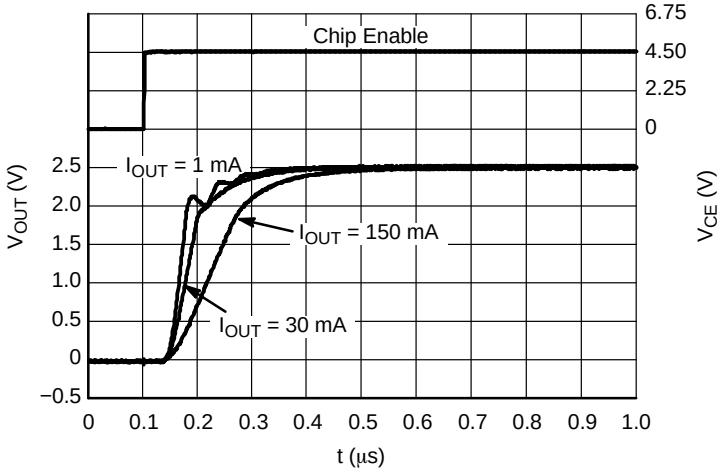


Figure 41. Start−up, 2.5 V Version, V_{IN} = 4.5 V

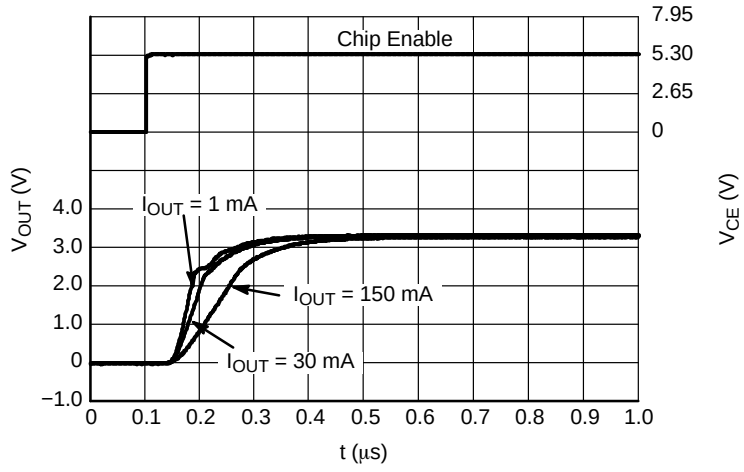


Figure 42. Start−up, 3.3 V Version, V_{IN} = 5.3 V

TYPICAL CHARACTERISTICS

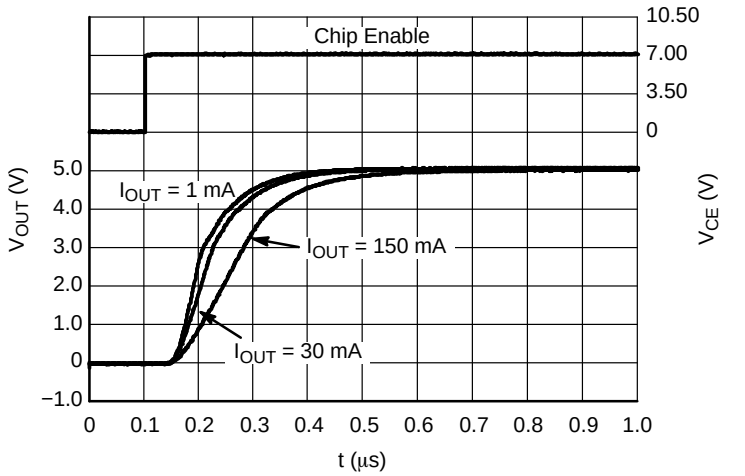


Figure 43. Start−up, 5.0 V Version, V_{IN} = 7.0 V

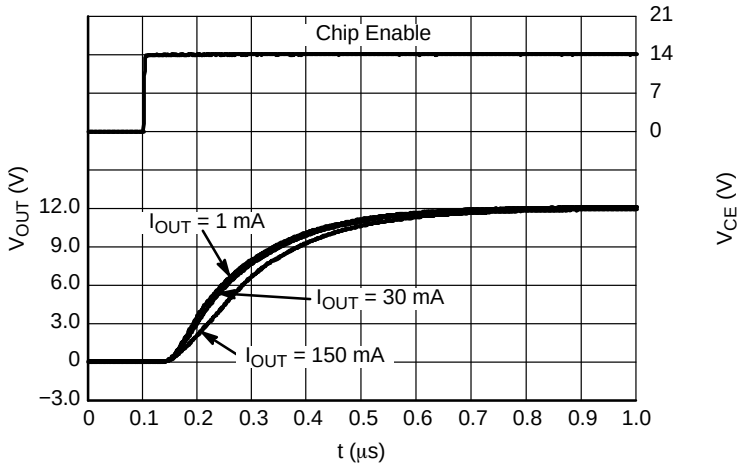


Figure 45. Start−up, 12.0 V Version, V_{IN} = 14.0 V

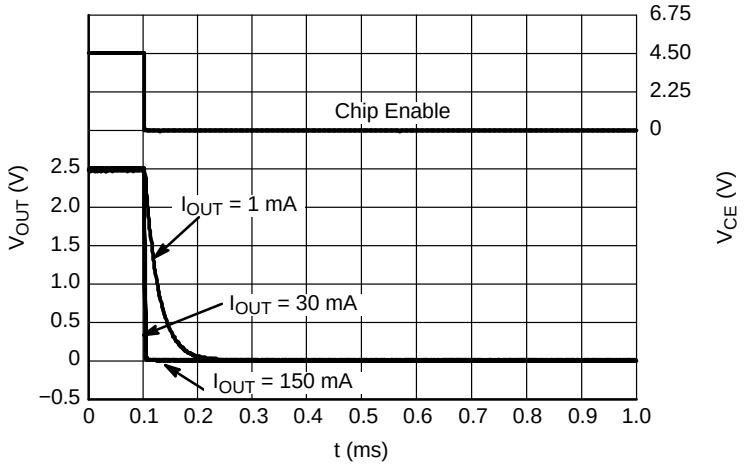


Figure 44. Shutdown, 2.5 V Version, V_{IN} = 4.5 V

TYPICAL CHARACTERISTICS

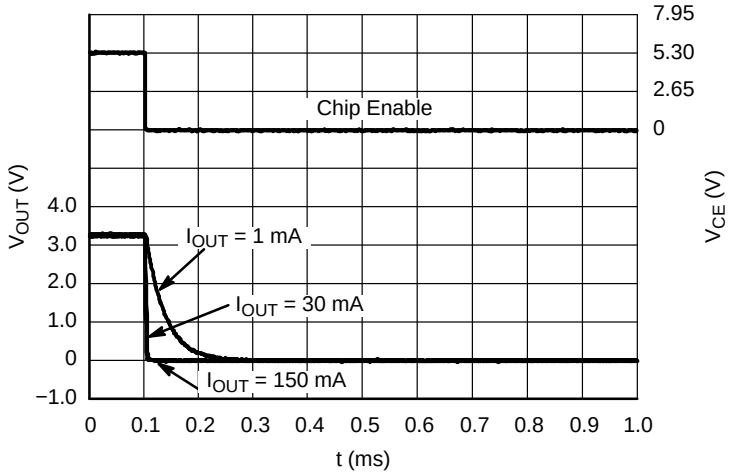


Figure 46. Shutdown, 3.3 V Version, V_{IN} = 5.3 V

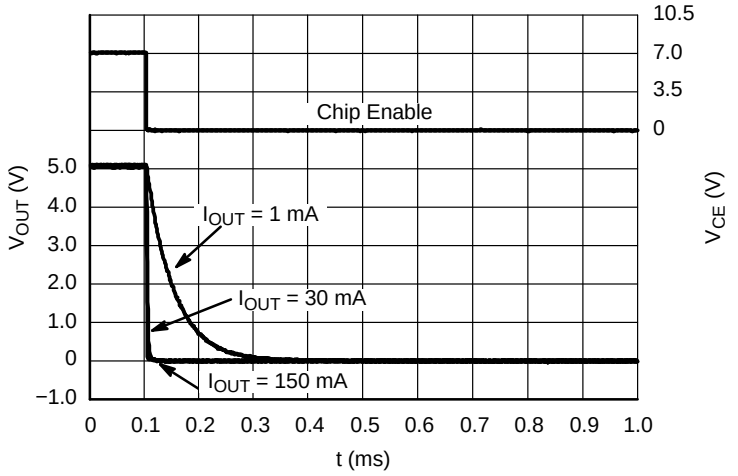


Figure 47. Shutdown, 5.0 V Version, V_{IN} = 7.0 V

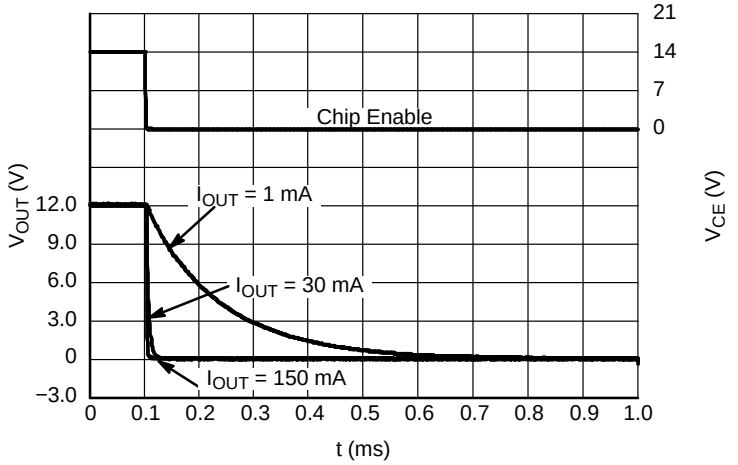


Figure 48. Shutdown, 12.0 V Version, V_{IN} = 14.0 V

APPLICATION INFORMATION

A typical application circuits for NCP4623 series is shown in Figure 49.

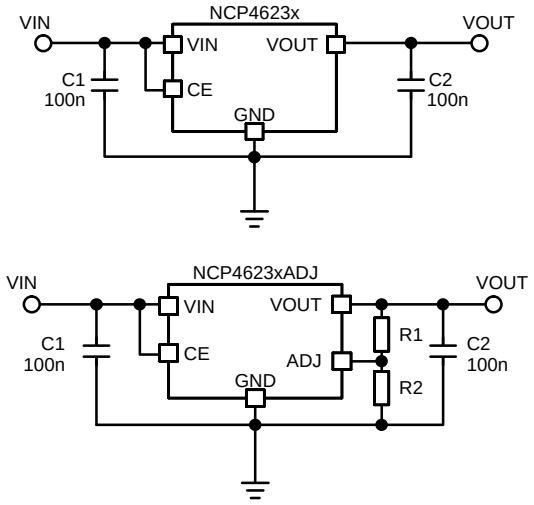


Figure 49. Typical Application Schematics

Input Decoupling Capacitor (C1)

A 0.1 μF ceramic input decoupling capacitor should be connected as close as possible to the input and ground pin of the NCP4623. Higher values and lower ESR improves line transient response.

Output Decoupling Capacitor (C2)

Recommended values of the ceramic output decoupling capacitor is in the range from 0.1 μF to 2.2 μF. Stable operation of the regulator should be achieved within this range. If a tantalum capacitor is used, and its ESR is high, loop oscillation may result. The capacitors should be connected as close as possible to the output and ground pins. Larger values and lower ESR improves dynamic parameters.

Output Voltage Setting (ADJ version)

The output voltage of the adjustable regulator may be set for any output voltage from its voltage reference (2.5 V) up to V_{IN} voltage by an external voltage divider connected between VOUT and GND pins with its center connected to the ADJ pin. The voltage divider is loaded by current into ADJ pin that is typically around 200 nA. This current may cause an error in V_{OUT}, therefore it is good to choose values of voltage divider low enough to achieve cross current around 2 μA to eliminate error. Output voltage can be computed from the equation:

$$V_{OUT} = 2.5\left(1 + \frac{R1}{R2}\right) + R1 \cdot I_{ADJ} \qquad \text{(eq. 1)}$$

Enable Operation

The enable pin CE may be used for turning the regulator on and off. The IC is switched on when a high level voltage is applied to the CE pin. Do not leave the CE pin unconnected or between VCEH and VCEL voltage levels as this may leave the output voltage unstable or cause indefinite and unexpected currents flows internally.

Current Limit

This regulator includes a fold−back type current limit circuit. This type of protection doesn't limit output current up to specified current capability in normal operation, but when an over current occurs, output voltage and current decrease until the over current condition ends. Typical characteristics of this protection type can be observed in the Output Voltage vs. Output Current graphs shown in the typical characteristics section of this datasheet.

Thermal

As power across the IC increase, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and also the ambient temperature affect the rate of temperature increase for the part. When the device has good thermal conductivity through the PCB the junction temperature will be relatively low in high power dissipation applications.

The IC includes internal thermal shutdown circuit that stops operation of regulator, if junction temperature is higher than 150°C. After that, when junction temperature decreases below 125°C, the operation of voltage regulator will resume. During high power dissipation condition, the regulator shuts down and resumes repeatedly protecting itself from overheating.

PCB layout

Make the V_{IN} and GND line as large as practical. If their impedance is high, noise pickup or unstable operation may result. Connect capacitors C1 and C2 as close as possible to the IC, and make wiring as short as possible.

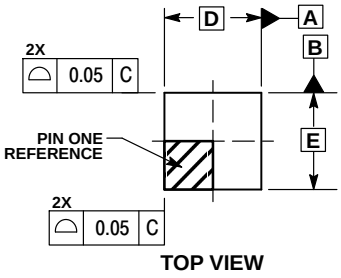
ORDERING INFORMATION

Device	Nominal Output Voltage	Description	Marking	Package	Shipping†
NCP4623HSNADJT1G	Adjustable	Enable high	J24	SOT23−5 (Pb−Free)	3000 / Tape & Reel
NCP4623HSN050T1G	5.0 V	Enable high	J50		
NCP4623HSN100T1G	10.0 V	Enable high	J00		
NCP4623HSN120T1G	12.0 V	Enable high	J20		
NCP4623HMXADJTCG	Adjustable	Enable high	BQ24	XDFN1616−6 (Pb−Free)	5000 / Tape & Reel
NCP4623HMX025TCG	2.5 V	Enable high	BQ25		
NCP4623HMX033TCG	3.3 V	Enable high	BQ33		
NCP4623HMX045TCG	4.5 V	Enable high	BQ45		
NCP4623HMX048TCG	4.8 V	Enable high	BQ48		
NCP4623HMX050TCG	5.0 V	Enable high	BQ50		
NCP4623HMX080TCG	8.0 V	Enable high	BQ80		

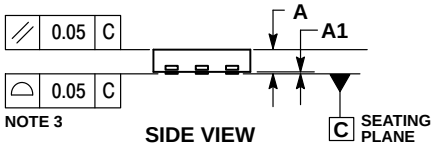
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*To order other package and voltage variants, please contact your ON Semiconductor sales representative.

PACKAGE DIMENSIONS

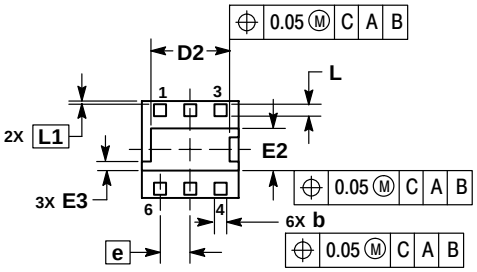
XDFN6 1.6x1.6, 0.5P
CASE 711AC
ISSUE O



TOP VIEW



SIDE VIEW

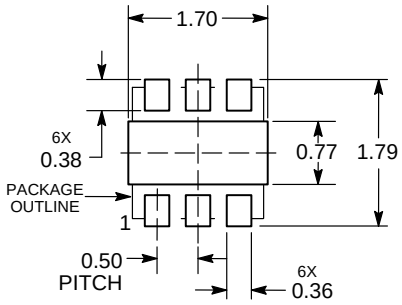


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.60 BSC	
D2	1.25	1.35
E	1.60 BSC	
E2	0.65	0.75
E3	0.15 REF	
e	0.50 BSC	
L	0.15	0.25
L1	0.05 BSC	

RECOMMENDED MOUNTING FOOTPRINT*

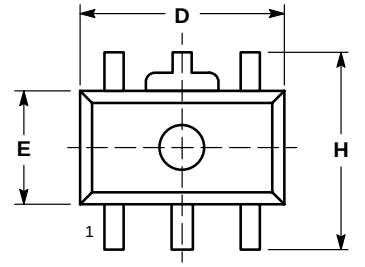


DIMENSIONS: MILLIMETERS

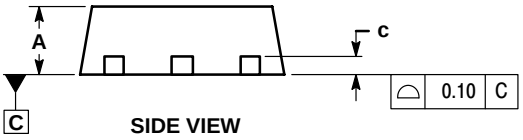
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

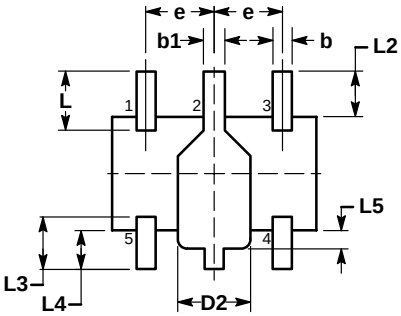
SOT−89, 5 LEAD
CASE 528AB
ISSUE O



TOP VIEW



SIDE VIEW

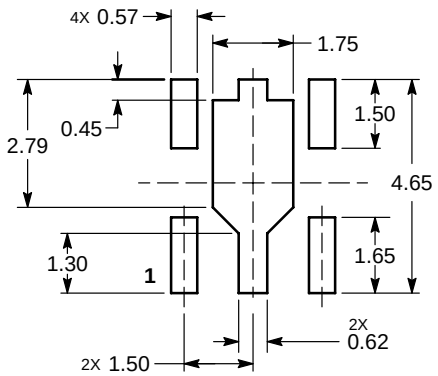


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. LEAD THICKNESS INCLUDES LEAD FINISH.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. DIMENSIONS L, L2, L3, L4, L5, AND H ARE MEASURED AT DATUM PLANE C.

	MILLIMETERS	
DIM	MIN	MAX
A	1.40	1.60
b	0.32	0.52
b1	0.37	0.57
c	0.30	0.50
D	4.40	4.60
D2	1.40	1.80
E	2.40	2.60
e	1.40	1.60
H	4.25	4.45
L	1.10	1.50
L2	0.80	1.20
L3	0.95	1.35
L4	0.65	1.05
L5	0.20	0.60

RECOMMENDED MOUNTING FOOTPRINT*

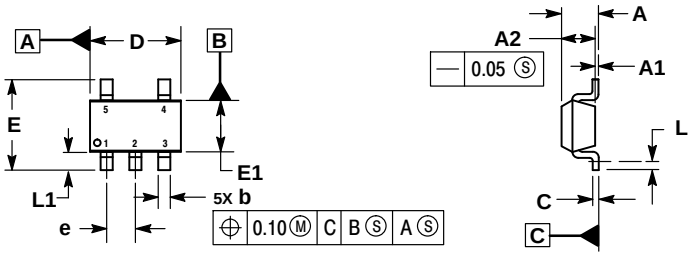


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

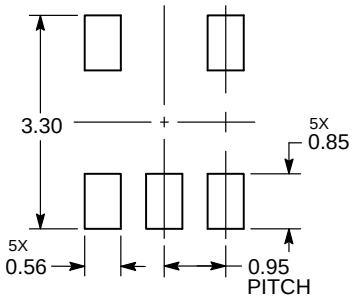
SOT−23 5−LEAD
CASE 1212
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DATUM C IS THE SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.45
A1	0.00	0.10
A2	1.00	1.30
b	0.30	0.50
c	0.10	0.25
D	2.70	3.10
E	2.50	3.10
E1	1.50	1.80
e	0.95 BSC	
L	0.20	---
L1	0.45	0.75

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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