

3.3 V/2.5 V/1.8 V/1.5 V 160 MHz 1:4 LVCMOS/LVTTL Low Skew Over Voltage Tolerant Fanout Buffer

NB3U1548C

Description

The NB3U1548C is an LVCMOS, overvoltage tolerant clock fanout buffer targeted for clock generation in high performance telecommunication, networking and computing applications. The device is optimized for low skew clock distribution in low voltage applications. The input overvoltage tolerance enables using this device in mixed mode voltage applications. An output enable pin controls whether the outputs are in the active or high impedance state. Guaranteed output skew characteristics make the NB3U1548C ideal for those applications demanding well defined performance and repeatability. The NB3U1548C is packaged in a small SOIC-8 and in an TSSOP-8 package.

Features

- Low skew 1:4 Fanout Buffer
- Supports 3.3 V, 2.5 V, 1.8 V and 1.5 V Power Supplies
- LVCMOS Input and Output Levels
- 3.6 V Overvoltage Tolerance at the Clock and Control Inputs
- Supports Clock Frequencies up to 160 MHz
- LVCMOS Compatible Control Input for Output Disable
- Output Disabled to a High Impedance State
- -40°C to 85°C Ambient Operating Temperature
- Available in Pb-Free RoHS Compliant Packages (SOIC-8, TSSOP-8)
- These Devices are Pb-Free and are RoHS Compliant

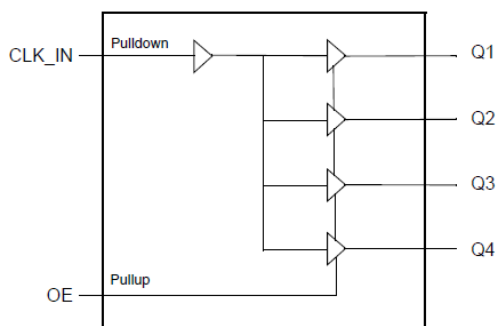
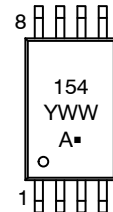
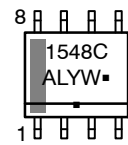


Figure 1. Block Diagram

MARKING DIAGRAMS



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W, WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

NB3U1548C

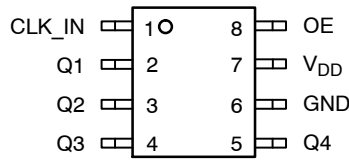


Figure 2. Pin Configuration (Top View)

Table 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	CLK_IN	Input	Pulldown	Single-ended clock input. LVCMOS interface levels.
2	Q1	Output		Single-ended clock output. LVCMOS interface levels.
3	Q2	Output		Single-ended clock output. LVCMOS interface levels.
4	Q3	Output		Single-ended clock output. LVCMOS interface levels.
5	Q4	Output		Single-ended clock output. LVCMOS interface levels.
6	GND	Power		Power supply ground.
7	VDD	Power		Power supply pin.
8	OE	Input	Pullup	Output enable pin. See Table 3. LVCMOS interface levels.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
CIN	Input Capacitance			4		pF
CPD	Power Dissipation Capacitance	$V_{DD} = 3.465\text{ V}$		14		pF
		$V_{DD} = 2.375\text{ V}$		13		pF
		$V_{DD} = 1.95\text{ V}$		13		pF
		$V_{DD} = 1.6\text{ V}$		12		pF
RPULLUP	Input Pullup Resistor			51		k Ω
RPULLDOWN	Input Pulldown Resistor			51		k Ω
ROUT	Output Impedance	$V_{DD} = 3.3\text{ V} \pm 5\%$		9		Ω
		$V_{DD} = 2.5\text{ V} \pm 5\%$		10		Ω
		$V_{DD} = 1.8\text{ V} \pm 0.15\text{ V}$		12		Ω
		$V_{DD} = 1.5 \pm 0.1\text{ V}$		15		Ω

FUNCTION TABLE

Table 3. OE CONFIGURATION TABLE

Input	Operation
OE	
0	Q[4:1] disabled (high-impedance)
1 (default)	Q[4:1] enabled

NOTE: OE is an asynchronous control.

NB3U1548C

Table 4. ABSOLUTE MAXIMUM RATINGS

Item	Rating
Supply Voltage, V_{DD}	4.6 V
Inputs, V_I	3.6 V
Outputs, V_O	-0.5 V to $V_{DD} + 0.5$ V
Package Thermal Impedance, θ_{JA} 8 Lead SOIC 8 Lead TSSOP	102.5°C/W (0 mps) 151.2°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 6 cm² copper area.
2. For additional information, see Application Note AND8003/D.

Table 5. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3$ V \pm 5%, $T_A = -40^\circ$ C to 85° C

V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
I_{DDQ}	Quiescent Power Supply Current	Inputs Open, Outputs Unloaded			1	mA

POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 2.5$ V \pm 5%, $T_A = -40^\circ$ C to 85° C

V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
I_{DDQ}	Quiescent Power Supply Current	Inputs Open, Outputs Unloaded			1	mA

POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 1.8$ V \pm 0.15 V, $T_A = -40^\circ$ C to 85° C

V_{DD}	Power Supply Voltage		1.65	1.8	1.95	V
I_{DDQ}	Quiescent Power Supply Current	Inputs Open, Outputs Unloaded			1	mA

POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 1.5$ V \pm 0.1 V, $T_A = -40^\circ$ C to 85° C

V_{DD}	Power Supply Voltage		1.4	1.5	1.6	V
I_{DDQ}	Quiescent Power Supply Current	Inputs Open, Outputs Unloaded			1	mA

LVC MOS DC CHARACTERISTICS, $V_{DD} = 3.3$ V \pm 5%, $T_A = -40^\circ$ C to 85° C

V_{IH}	Input High Voltage		$0.65 * V_{DD}$		3.6	V
V_{IL}	Input Low Voltage		-0.3		$0.35 * V_{DD}$	V
I_{IH}	Input High Current	CLK_IN	$V_{DD} = V_{IN} = 3.465$ V		165	μ A
		OE	$V_{DD} = V_{IN} = 3.465$ V		5	μ A
I_{IL}	Input Low Current	CLK_IN	$V_{DD} = 3.465$ V, $V_{IN} = 0$ V	-5		μ A
		OE	$V_{DD} = 3.465$ V, $V_{IN} = 0$ V	-150		μ A
V_{OH}	Output High Voltage	Q[4:1]	$I_{OH} = -12$ mA	2.6		V
V_{OL}	Output Low Voltage	Q[4:1]	$I_{OL} = 12$ mA		0.5	V

LVC MOS DC CHARACTERISTICS, $V_{DD} = 2.5$ V \pm 5%, $T_A = -40^\circ$ C to 85° C

V_{IH}	Input High Voltage		$0.65 * V_{DD}$		3.6	V
V_{IL}	Input Low Voltage		-0.3		$0.35 * V_{DD}$	V
I_{IH}	Input High Current	CLK_IN	$V_{DD} = V_{IN} = 2.625$ V		165	μ A
		OE	$V_{DD} = V_{IN} = 2.625$ V		5	μ A
I_{IL}	Input Low Current	CLK_IN	$V_{DD} = 2.625$ V, $V_{IN} = 0$ V	-5		μ A
		OE	$V_{DD} = 2.625$ V, $V_{IN} = 0$ V	-150		μ A

NB3U1548C

Table 5. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
LVC MOS DC CHARACTERISTICS, $V_{DD} = 2.5\text{ V} \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C						
V_{OH}	Output High Voltage	Q[4:1]	$I_{OH} = -12\text{ mA}$	1.8		V
V_{OL}	Output Low Voltage	Q[4:1]	$I_{OL} = 12\text{ mA}$		0.5	V
LVC MOS DC CHARACTERISTICS, $V_{DD} = 1.8\text{ V} \pm 0.15\text{ V}$, $T_A = -40^\circ\text{C}$ to 85°C						
V_{IH}	Input High Voltage			$0.65 * V_{DD}$	3.6	V
V_{IL}	Input Low Voltage			-0.3	$0.35 * V_{DD}$	V
I_{IH}	Input High Current	CLK_IN	$V_{DD} = V_{IN} = 1.95\text{ V}$		165	μA
		OE			5	μA
I_{IL}	Input Low Current	CLK_IN	$V_{DD} = 1.95\text{ V}, V_{IN} = 0\text{ V}$	-5		μA
		OE	$V_{DD} = 1.95\text{ V}, V_{IN} = 0\text{ V}$	-150		μA
V_{OH}	Output High Voltage	Q[4:1]	$I_{OH} = -6\text{ mA}$	$V_{DD} - 0.45$		V
V_{OL}	Output Low Voltage	Q[4:1]	$I_{OL} = 6\text{ mA}$		0.45	V
LVC MOS DC CHARACTERISTICS, $V_{DD} = 1.5\text{ V} \pm 0.1\text{ V}$, $T_A = -40^\circ\text{C}$ to 85°C						
V_{IH}	Input High Voltage			$0.65 * V_{DD}$	3.6	V
V_{IL}	Input Low Voltage			-0.3	$0.35 * V_{DD}$	V
I_{IH}	Input High Current	CLK_IN	$V_{DD} = V_{IN} = 1.6\text{ V}$		165	μA
		OE	$V_{DD} = V_{IN} = 1.6\text{ V}$		5	μA
I_{IL}	Input Low Current	CLK_IN	$V_{DD} = 1.6\text{ V}, V_{IN} = 0\text{ V}$	-5		μA
		OE	$V_{DD} = 1.6\text{ V}, V_{IN} = 0\text{ V}$	-150		μA
V_{OH}	Output High Voltage	Q[4:1]	$I_{OH} = -4\text{ mA}$	$0.75 * V_{DD}$		V
V_{OL}	Output Low Voltage	Q[4:1]	$I_{OL} = 4\text{ mA}$		$0.25 * V_{DD}$	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NB3U1548C

Table 6. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
AC CHARACTERISTICS, $V_{DD} = 3.3 V \pm 5\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$						
f_{OUT}	Output Frequency				160	MHz
t_{PLH}	Propagation Delay (low to high transition); (Notes 4, 8)		0.7		2.1	ns
t_{PHL}	Propagation Delay (high to low transition); (Notes 4, 8)		0.7		2.1	ns
t_{PLZ}, t_{PHZ}	Disable Time, (active to high-impedance)				10	ns
t_{PZL}, t_{PZH}	Enable Time, (high-impedance to active)				10	ns
$tsk(o)$	Output Skew; (Notes 5, 6)				250	ps
$tsk(pp)$	Part-to-Part Skew; (Notes 5, 7)				800	ps
t_{jit}	Buffer Additive Phase Jitter, RMS	25 MHz, Integration Range: 12 kHz – 5 MHz		0.094		ps
t_R / t_F	Output Rise/Fall Time	10% to 90%	0.33		1.2	ns
odc	Output Duty Cycle		48		53	%

AC CHARACTERISTICS, $V_{DD} = 2.5 V \pm 5\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

f_{OUT}	Output Frequency				160	MHz
t_{PLH}	Propagation Delay (low to high transition); (Notes 4, 8)		0.8		2.0	ns
t_{PHL}	Propagation Delay (high to low transition); (Notes 4, 8)		0.8		2.0	ns
t_{PLZ}, t_{PHZ}	Disable Time (active to high-impedance)				10	ns
t_{PZL}, t_{PZH}	Enable Time (high-impedance to active)				10	ns
$tsk(o)$	Output Skew; (Notes 5, 6)				250	ps
$tsk(pp)$	Part-to-Part Skew; (Notes 5, 7)				800	ps
t_{jit}	Buffer Additive Phase Jitter, RMS	25 MHz, Integration Range: 12 kHz – 5 MHz		0.076		ps
t_R / t_F	Output Rise/Fall Time	10% to 90%	0.33		1.2	ns
odc	Output Duty Cycle		45		53	%

AC CHARACTERISTICS, $V_{DD} = 1.8 V \pm 0.15 V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

f_{OUT}	Output Frequency				160	MHz
t_{PLH}	Propagation Delay (low to high transition); (Notes 4, 8)		1.1		2.8	ns
t_{PHL}	Propagation Delay (high to low transition); (Notes 4, 8)		1.1		2.8	ns
t_{PLZ}, t_{PHZ}	Disable Time (active to high-impedance)				10	ns
t_{PZL}, t_{PZH}	Enable Time (high-impedance to active)				10	ns
$tsk(o)$	Output Skew; (Notes 5, 6)				250	ps
$tsk(pp)$	Part-to-Part Skew; (Notes 5, 7)				800	ps
t_{jit}	Buffer Additive Phase Jitter, RMS	25 MHz, Integration Range: 12 kHz – 5MHz		0.193		ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

3. Characterized up to $F_{OUT} \leq 150$ MHz.
4. Measured from the $V_{DD}/2$ of the input to $V_{DD}/2$ of the output.
5. This parameter is defined in accordance with JEDEC Standard 65.
6. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DD}/2$.
7. Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DD}/2$.
8. With rail to rail input clock.

NB3U1548C

Table 6. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
AC CHARACTERISTICS, $V_{DD} = 1.8\text{ V} \pm 0.15\text{ V}$, $T_A = -40^\circ\text{C}$ to 85°C						
t_R / t_F	Output Rise/Fall Time	0.63 V to 1.17 V	0.11		0.6	ns
odc	Output Duty Cycle		47		53	%
AC CHARACTERISTICS, $V_{DD} = 1.5\text{ V} \pm 0.1\text{ V}$, $T_A = -40^\circ\text{C}$ to 85°C						
f_{OUT}	Output Frequency				160	MHz
t_{PLH}	Propagation Delay (low to high transition); (Notes 4, 8)		1.5		3.5	ns
t_{PHL}	Propagation Delay (high to low transition); (Notes 4, 8)		1.5		3.5	ns
t_{PLZ} , t_{PHZ}	Disable Time (active to high-impedance)				10	ns
t_{PZL} , t_{PZH}	Enable Time (high-impedance to active)				10	ns
tsk(o)	Output Skew; (Notes 5, 6)				250	ps
tsk(pp)	Part-to-Part Skew; (Notes 5, 7)				800	ps
tjit	Buffer Additive Phase Jitter, RMS	25 MHz, Integration Range: 12 kHz – 5 MHz		0.266		ps
t_R / t_F	Output Rise/Fall Time	0.525 V to 0.975 V	0.11		0.6	ns
odc	Output Duty Cycle		47		53	%

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

3. Characterized up to $F_{OUT} \leq 150\text{ MHz}$.
4. Measured from the $V_{DD}/2$ of the input to $V_{DD}/2$ of the output.
5. This parameter is defined in accordance with JEDEC Standard 65.
6. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DD}/2$.
7. Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DD}/2$.
8. With rail to rail input clock.

PARAMETER MEASUREMENT INFORMATION

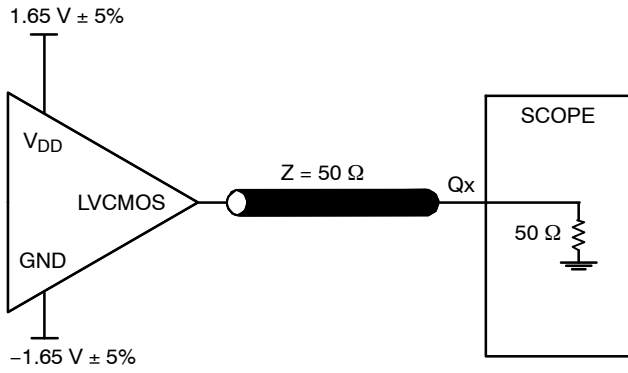


Figure 3. 3.3 V Output Load AC Test Circuit

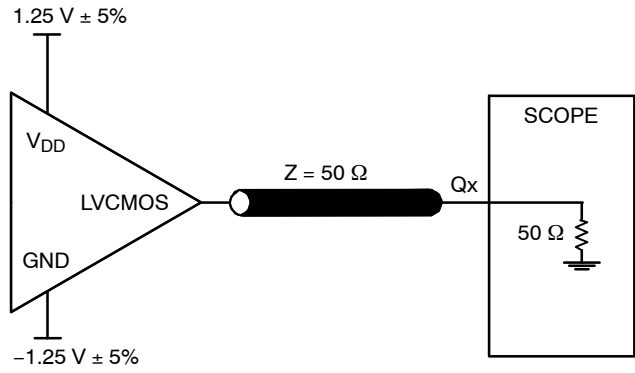


Figure 4. 2.5 V Output Load AC Test Circuit

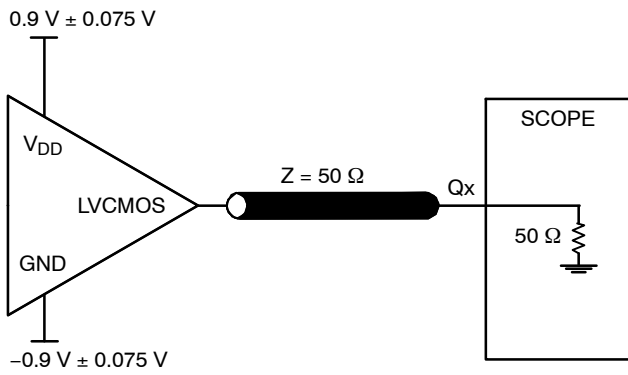


Figure 5. 1.8 V Output Load AC Test Circuit

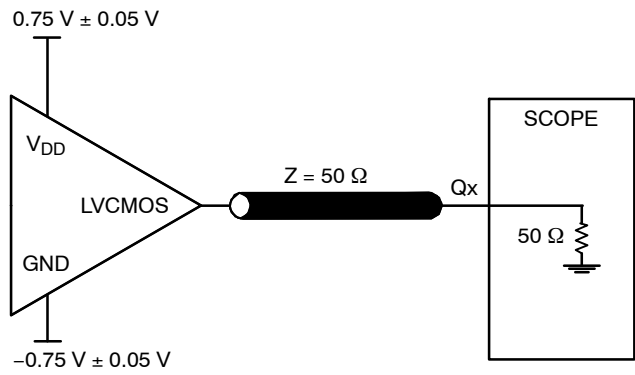


Figure 6. 1.5 V Output Load AC Test Circuit

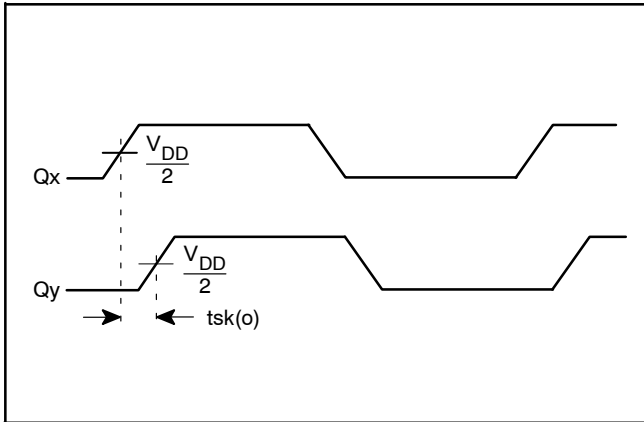


Figure 7. Output Skew

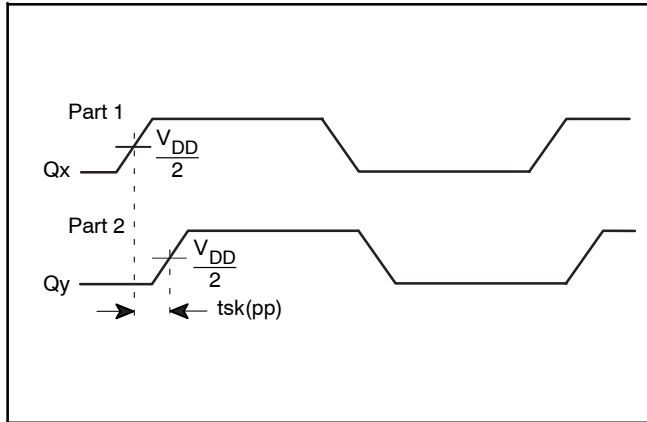


Figure 8. Part-to-Part Skew

PARAMETER MEASUREMENT INFORMATION, (CONTINUED)

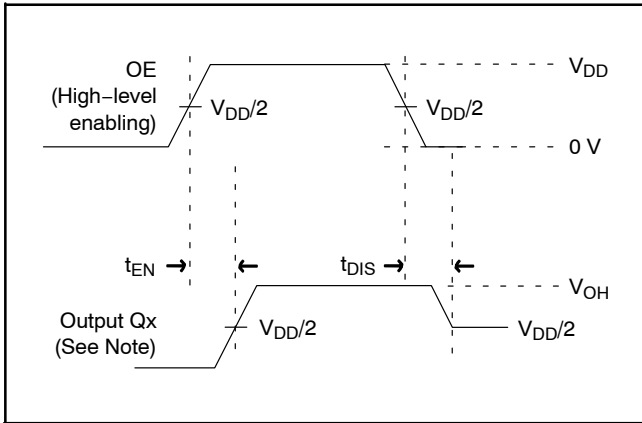


Figure 9. Output Enable/Disable Time

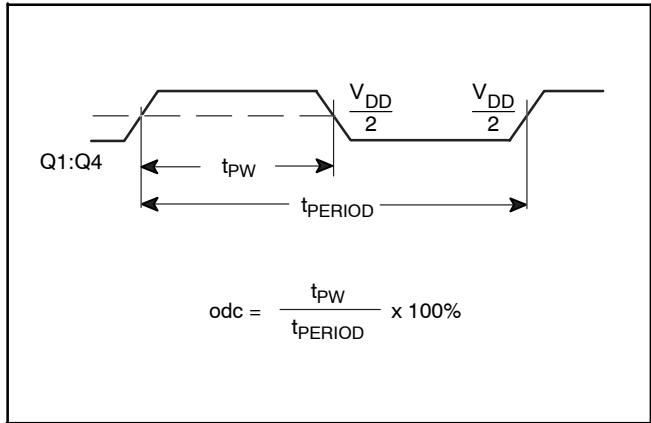


Figure 10. Output Duty Cycle/Pulse Width/Period

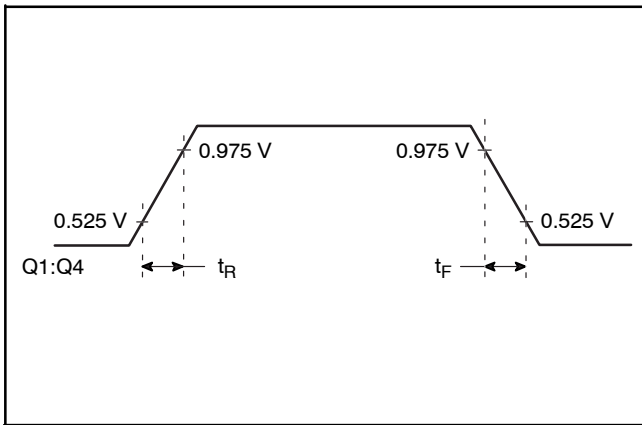


Figure 11. 1.5 V Output Rise/Fall Time

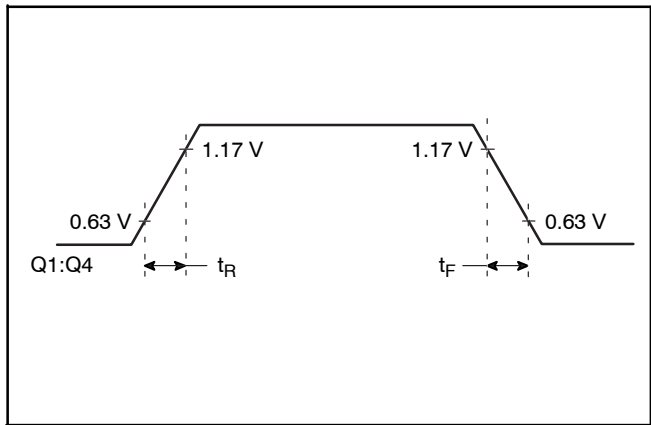


Figure 12. 1.8 V Output Rise/Fall Time

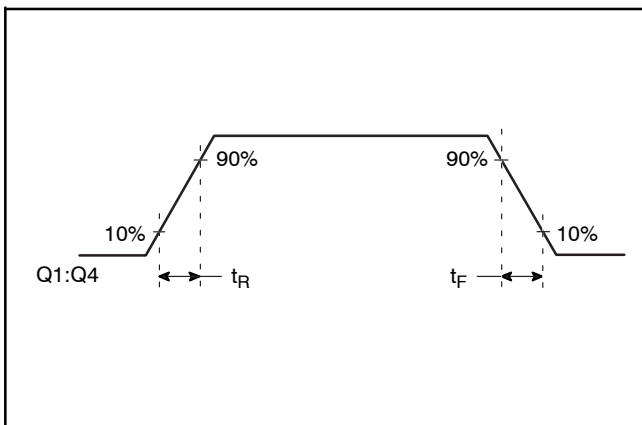


Figure 13. 2.5 V and 3.3 V Output Rise/Fall Time

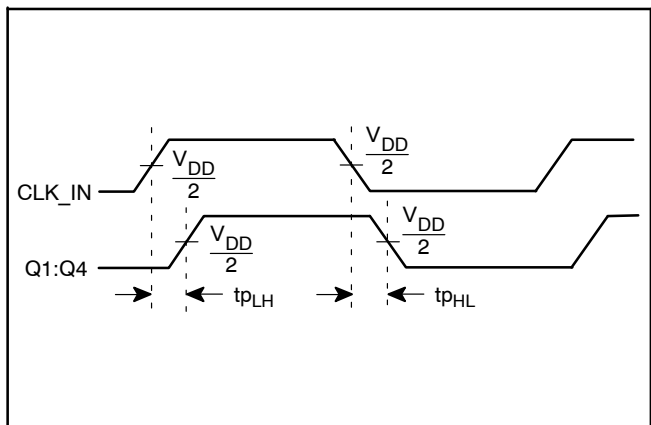


Figure 14. Propagation Delay

NB3U1548C

Table 7. THERMAL RESISTANCE θ_{JA}

θ_{JA} by Velocity			
FOR 8 LEAD SOIC, FORCED CONVECTION			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	102.5°C/W	93.5°C/W	88.6°C/W
FOR 8 LEAD TSSOP, FORCED CONVECTION			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	151.2°C/W	145.9°C/W	143.3°C/W
θ_{JA} by Velocity			

Table 8. ORDERING INFORMATION

Device	Package	Shipping [†]
NB3U1548CDG	SOIC-8 (Pb-Free)	96 Units / Tube
NB3U1548CDR2G	SOIC-8 (Pb-Free)	3,000 / Tape & Reel
NB3U1548CDTR2G	TSSOP-8 (Pb-Free)	2,500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

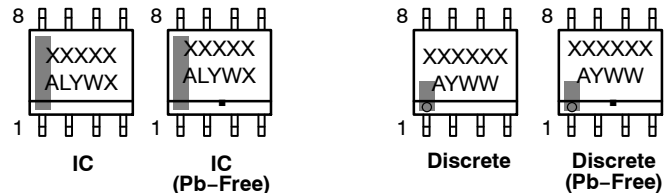
DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

onsemi and ONsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOIC-8 NB
CASE 751-07
ISSUE AK

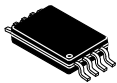
DATE 16 FEB 2011

- | | | | |
|--|---|---|---|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC_OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 2 OF 2

onsemi and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

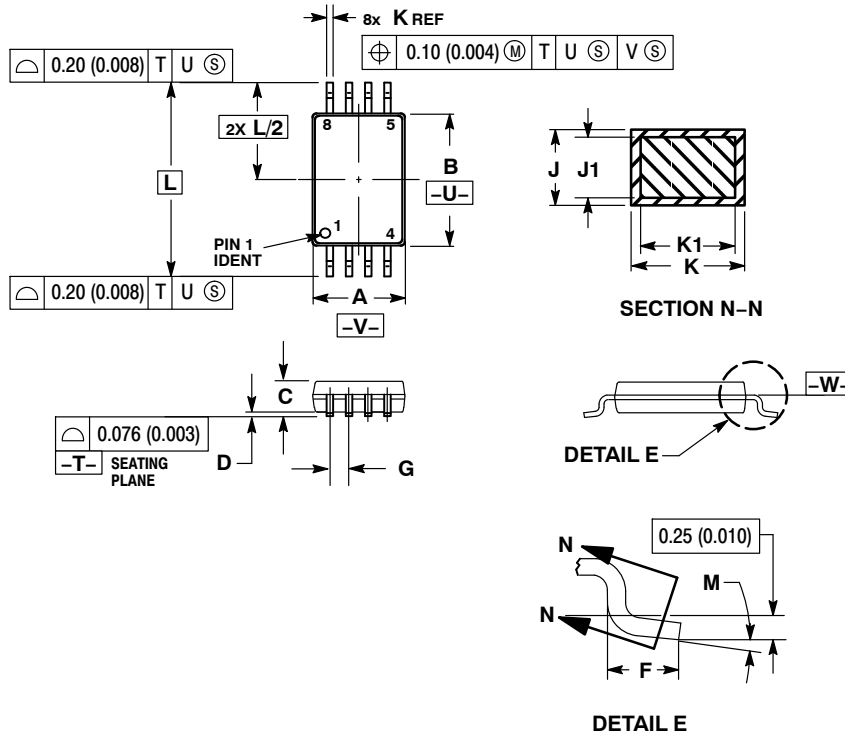
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

TSSOP-8
CASE 948S
ISSUE C

DATE 20 JUN 2008

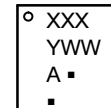


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026 BSC	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON00697D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSSOP-8	PAGE 1 OF 1

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales