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1Mb Ultra-Low Power Asynchronous CMOS SRAM

64K × 16 bit

Overview

The N01L6183A is an integrated memory device containing a 1 Mbit Static Random Access Memory organized as 65,536 words by 16 bits. The device is designed and fabricated using ON Semiconductor's advanced CMOS technology to provide both high-speed performance and ultra-low power. The device operates with a single chip enable (CE) control and output enable (OE) to allow for easy memory expansion. Byte controls $(\overline{UB} \text{ and } \overline{LB})$ allow the upper and lower bytes to be accessed independently. The N01L6183A is optimal for various applications where low-power is critical such as battery backup and hand-held devices. The device can operate over a very wide temperature range of -40°C to +85°C and is available in JEDEC standard packages compatible with other standard 64Kb x 16 SRAMs.

Features

- Single Wide Power Supply Range 1.65 to 2.2 Volts
- Very low standby current 0.5µA at 1.8V (Typical)
- Very low operating current 0.7mA at 1.8V and 1µs (Typical)
- Very low Page Mode operating current 0.5mA at 1.8V and 1µs (Typical)
- Simple memory control Single Chip Enable (CE) Byte control for independent byte operation Output Enable (OE) for memory expansion
- Low voltage data retention Vcc = 1.2V
- Very fast output enable access time 30ns OE access time
- Automatic power down to standby mode
- TTL compatible three-state output driver
- Compact space saving BGA package available

Part Number	Package Type	Operating Temperature	Power Supply (Vcc)	Speed	Standby Current (I _{SB}), Typical	Operating Current (Icc), Typical
N01L6183AB	48 - BGA					
N01L6183AT	44 - TSOP II	4000 1		70ns @ 1.8V 85ns @ 1.65V	0.5 μΑ	0.7 mA @
N01L6183AB2	48 - BGA Green	-40°C to +85°C	1.65V - 2.2V			1MHz
N01L6183AT2	44 - TSOP II Green					

6

NC I/O₀ I/O₂ V_{CC} V_{SS} I/O₆ I/O₇ NC

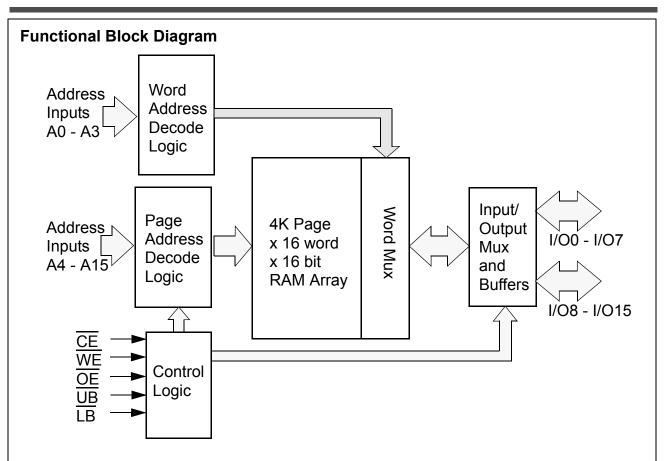
Product Family

Pin Configurations

A4 🗖 1 O	PIN	44 🗖 A5		1	2	3	4	5	
A3 2 A2 3 A1 4	ONE	43 A6 42 A7	А	LB	OE	A ₀	A ₁	A ₂	
$A_1 \square 4$ $A_0 \square 5$ $CE \square 6$		41 0E 40 UB 39 LB	в	1/O ₈	UB	A ₃	A ₄	CE	
I/O0 7 I/O1 8	∢	38 I/O15 37 I/O14	С	I/O ₉	I/O ₁₀	A ₅	A ₆	I/O ₁	
I/O2 9 I/O3 10 VCC 11	183. DP	36 I/O13 35 I/O12	D	v _{ss}	I/O ₁₁	NC	A ₇	I/O ₃	,
VSS 12 I/O4 13	N01L6183A TSOP	34 VSS 33 VCC 32 I/011	Е	v_{cc}	I/O ₁₂	NC	NC	I/O ₄	
I/O5 14 I/O6 15	Ň	31 I/O10 30 I/O9	F	I/O ₁₄	I/O ₁₃	A ₁₄	A ₁₅	I/O ₅	
I/O7 16 WE 17 A15 18		29 I/O8 28 NC	G	I/O ₁₅	NC	A ₁₂	A ₁₃	WE	
A15 18 A14 19 A13 20		27 A8 26 A9 25 A10	н	NC	A ₈	A ₉	A ₁₀	A ₁₁	
A12 21 NC 22		24 A11 23 NC		48	Pin		``	op)	
					6 ×	: 8 n	nm		

Pin Descriptions

Pin Name	Pin Function		
A ₀ -A ₁₅	Address Inputs		
WE	Write Enable Input		
CE	Chip Enable Input		
OE	Output Enable Input		
LB	Lower Byte Enable Input		
UB	Upper Byte Enable Input		
I/O ₀ -I/O ₁₅	Data Inputs/Outputs		
NC	Not Connected		
V _{CC}	Power		
V _{SS}	Ground		



Functional Description

CE	WE	OE	UB	LB	I/O ₀ - I/O ₁₅ ¹	MODE	POWER
Н	х	х	х	х	High Z	High Z Standby ²	
L	Х	Х	Н	Н	High Z	Active	Active
L	L	X ³	L^1	L^1	Data In	Write ³	Active -> Standby ⁴
L	Н	L	L ¹	L ¹	Data Out	Read	Active -> Standby ⁴
L	Н	Н	L ¹	L ¹	High Z	Active	Standby ⁴

1. When $\overline{\text{UB}}$ and $\overline{\text{LB}}$ are in select mode (low), I/O₀ - I/O₁₅ are affected as shown. When $\overline{\text{LB}}$ only is in the select mode only I/O₀ - I/O₇ are affected as shown. When $\overline{\text{UB}}$ is in the select mode only I/O₈ - I/O₁₅ are affected as shown.

2. When the device is in standby mode, control inputs (WE, OE, UB, and LB), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.

3. When WE is invoked, the OE input is internally disabled and has no effect on the circuit.

4. The device will consume active power in this mode whenever addresses are changed. Data inputs are internally isolated from any external influence.

Capacitance¹

ltem	Symbol	Test Condition	Min	Мах	Unit
Input Capacitance	C _{IN}	V _{IN} = 0V, f = 1 MHz, T _A = 25°C		8	pF
I/O Capacitance	C _{I/O}	V _{IN} = 0V, f = 1 MHz, T _A = 25°C		8	pF

1. These parameters are verified in device characterization and are not 100% tested

Absolute Maximum Ratings¹

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V _{IN,OUT}	–0.3 to V _{CC} +0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V _{CC}	-0.3 to 3.0	V
Power Dissipation	PD	500	mW
Storage Temperature	T _{STG}	-40 to 125	°C
Operating Temperature	T _A	-40 to +85	°C
Soldering Temperature and Time	T _{SOLDER}	260 ⁰ C, 10sec	°C

 Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Characteristics (Over Specified Temperature Range)

Item	Symbol	Test Conditions	Min.	Typ ¹	Max	Unit
Supply Voltage	V _{CC}		1.65	1.8	2.2	V
Data Retention Voltage	V _{DR}	Chip Disabled ³	1.2			V
Input High Voltage	V _{IH}		0.7V _{CC}		V _{CC} +0.3	V
Input Low Voltage	V _{IL}		-0.3		0.3V _{CC}	V
Output High Voltage	V _{OH}	I _{OH} = 0.2mA	V _{CC} -0.3			V
Output Low Voltage	V _{OL}	I _{OL} = -0.2mA			0.3	V
Input Leakage Current	ILI	$V_{IN} = 0$ to V_{CC}			0.5	μA
Output Leakage Current	I _{LO}	$\overline{OE} = V_{IH}$ or Chip Disabled			0.5	μA
Read/Write Operating Supply Current @ 1 µs Cycle Time ²	I _{CC1}	V_{CC} =2.2 V, V_{IN} = V_{IH} or V_{IL} Chip Enabled, I_{OUT} = 0		0.7	3.0	mA
Read/Write Operating Supply Current @ 85 ns Cycle Time ²	I _{CC2}	V_{CC} =2.2 V, V_{IN} = V_{IH} or V_{IL} Chip Enabled, I_{OUT} = 0		8	16	mA
Page Mode Operating Supply Current @ 85ns Cycle Time ² (Refer to Power Savings with Page Mode Operation diagram)	I _{CC3}	V _{CC} =2.2 V, V _{IN} =V _{IH} or V _{IL} Chip Enabled, I _{OUT} = 0,		3		mA
Read/Write Quiescent Operating Sup- ply Current ³	I _{CC4}	V_{CC} =2.2 V, V_{IN} = V_{IH} or V_{IL} Chip Enabled, I_{OUT} = 0, f = 0			20	μA
Maximum Standby Current ³	I _{SB1}	$V_{IN} = V_{CC} \text{ or } 0V$ Chip Disabled $t_A = 85^{\circ}C, V_{CC} = 2.2 V$		0.5	10	μΑ
Maximum Data Retention Current ³	I _{DR}	V_{CC} = 1.2V, V_{IN} = V_{CC} or 0 Chip Disabled, t_A = 85°C			5	μA

1. Typical values are measured at Vcc=Vcc Typ., $T_A \text{=} 25^\circ\text{C}$ and are not 100% tested.

2. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.

 This device assumes a standby mode if the chip is disabled (CE high). In order to achieve low standby current all inputs must be within 0.2 volts of either VCC or VSS

Power Savir	ngs with Page I	Node Operation (WE = V _{IH})	
Page Addre	ess (A4 - A15)	Open page	
Word Addre	ess (A0 - A3)	Word 1 Word 2 Word 16	3
CE			
ŌĒ			
$\overline{LB}, \overline{UB}$			

Note: Page mode operation is a method of addressing the SRAM to save operating current. The internal organization of the SRAM is optimized to allow this unique operating mode to be used as a valuable power saving feature.

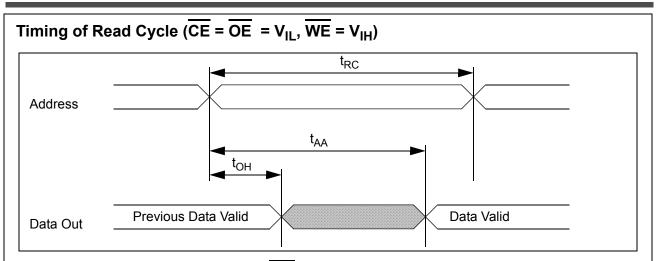
The only thing that needs to be done is to address the SRAM in a manner that the internal page is left open and 16-bit words of data are read from the open page. By treating addresses A0-A3 as the least significant bits and addressing the 16 words within the open page, power is reduced to the page mode value which is considerably lower than standard operating currents for low power SRAMs.

Timing Test Conditions

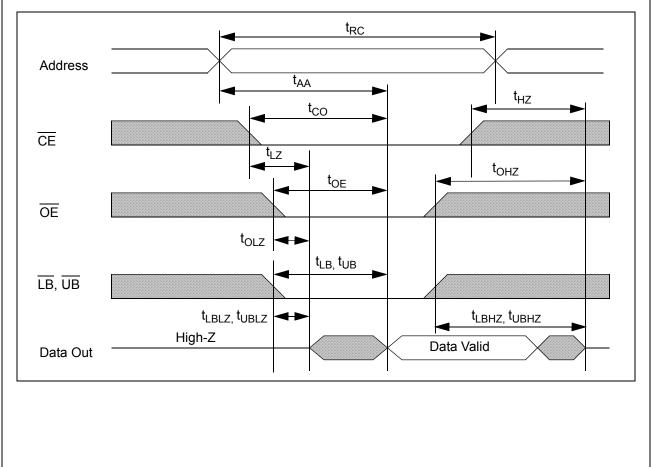
Item	
Input Pulse Level	0.1V _{CC} to 0.9 V _{CC}
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	0.5 V _{CC}
Output Load	CL = 30pF
Operating Temperature	-40 to +85 °C

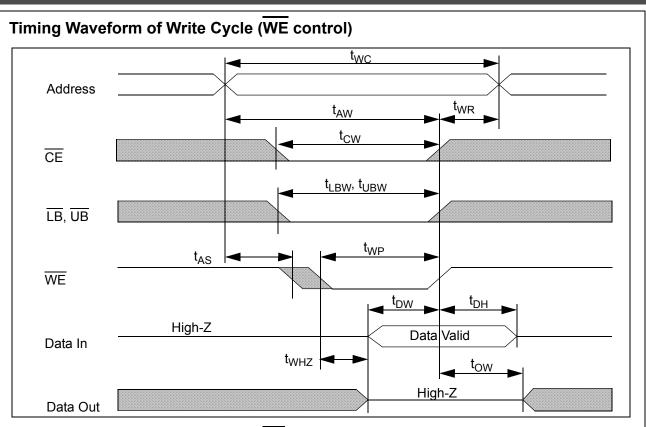
Timing

l to m	Cumhal	1.65 -	- 2.2 V	1.8 - 2.2 V		Unite
Item	Symbol	Min.	Max.	Min.	Max.	Units
Read Cycle Time	t _{RC}	85		70		ns
Address Access Time	t _{AA}		85		70	ns
Chip Enable to Valid Output	t _{CO}		85		70	ns
Output Enable to Valid Output	t _{OE}		35		30	ns
Byte Select to Valid Output	t _{LB} , t _{UB}		30		25	ns
Chip Enable to Low-Z output	t _{LZ}	10		10		ns
Output Enable to Low-Z Output	t _{OLZ}	5		5		ns
Byte Select to Low-Z Output	t _{LBZ} , t _{UBZ}	10		10		ns
Chip Disable to High-Z Output	t _{HZ}		30		25	ns
Output Disable to High-Z Output	t _{OHZ}		30		25	ns
Byte Select Disable to High-Z Output	t _{LBHZ} , t _{UBHZ}		30		25	ns
Output Hold from Address Change	t _{OH}	5		5		ns
Write Cycle Time	t _{WC}	85		70		ns
Chip Enable to End of Write	t _{CW}	50		40		ns
Address Valid to End of Write	t _{AW}	50		40		ns
Byte Select to End of Write	t _{LBW} , t _{UBW}	50		40		ns
Write Pulse Width	t _{WP}	50		40		ns
Address Setup Time	t _{AS}	0		0		ns
Write Recovery Time	t _{WR}	0		0		ns
Write to High-Z Output	t _{WHZ}		25		20	ns
Data to Write Time Overlap	t _{DW}	40		35		ns
Data Hold from Write Time	t _{DH}	0		0		ns
End Write to Low-Z Output	t _{ow}	10		10		ns

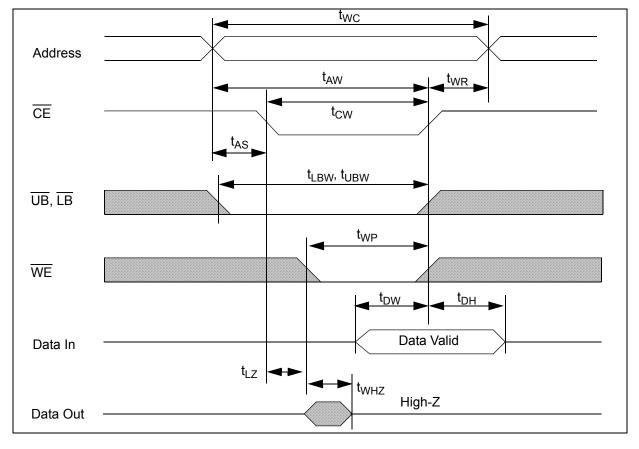


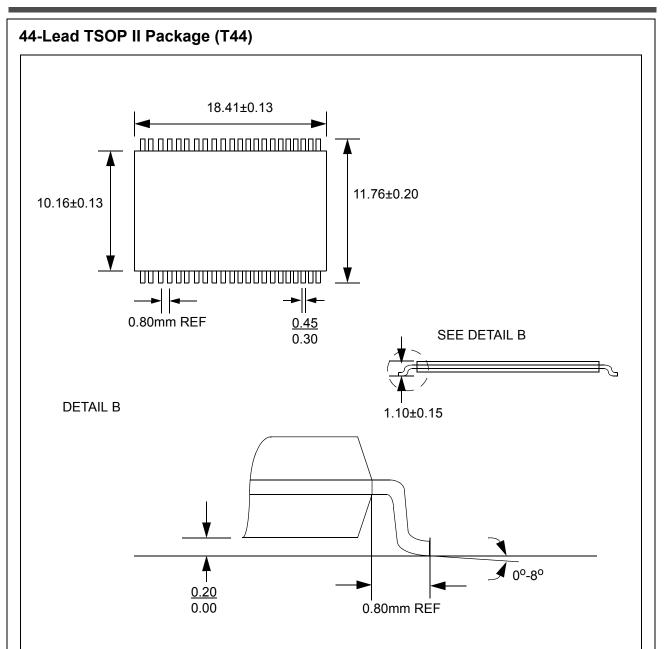
Timing Waveform of Read Cycle ($\overline{WE} = V_{IH}$)





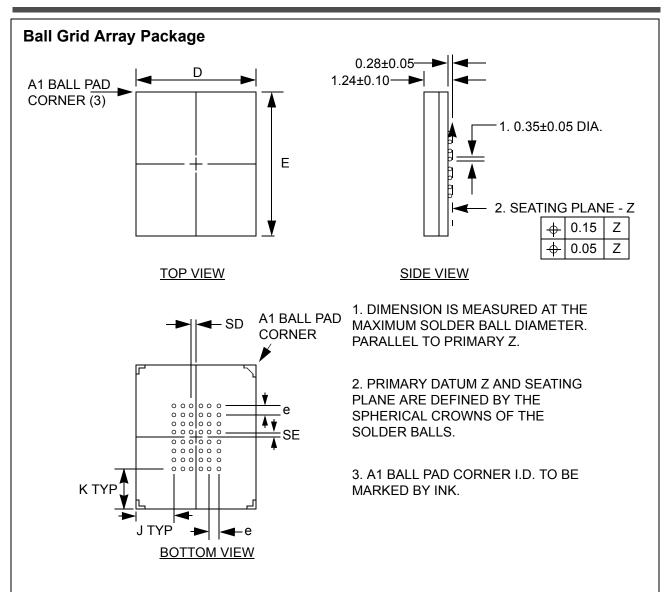
Timing Waveform of Write Cycle (CE Control)





Note:

- 1. All dimensions in millimeters
- 2. Package dimensions exclude molding flash



Dimensions (mm)

D	E		BALL MATRIX			
d	E	SD	SE	J	К	TYPE
6±0.10	8±0.10	0.375	0.375	1.125	1.375	FULL

Ordering Information

Part Number	Package	Shipping Method
N01L6183AT7I	Leaded 44-TSOP II	Tray
N01L6183AT27I	Green 44-TSOP II (RoHS Compliant)	Tray
N01L6183AB7I	Leaded 48-BGA	Tray
N01L6183AB27I	Green 48-BGA (RoHS Compliant)	Tray
N01L6183AT7IT	Leaded 44-TSOP II	Tape & Reel
N01L6183AT27IT	Green 44-TSOP II (RoHS Compliant)	Tape & Reel
N01L6183AB7IT	Leaded 48-BGA	Tape & Reel
N01L6183AB27IT	Green 48-BGA (RoHS Compliant)	Tape & Reel

Revision History

Revision #	Date	Change Description
A	Jan. 2001	Initial advance release
В	Apr. 2001	Changed operating voltage to 2.2V. Other minor erratas.
С	Dec. 2001	Part number change from EM064U16, modified Overview and Features, added Page Mode Operation diagam, revised Operating Characteristics table, Func- tional Description table and Ordering Information diagram
D	Nov. 2002	Replaced Isb and Icc on Product Family table with typical values
E	Oct. 2004	Added Pb-Free and Green Package Option
F	Nov. 2005	Removed Pb-Free Pkg, added Greenn Pkg & RoHS Compliant
G	September 2006	Converted to AMI Semiconductor
8	July 2008	Converted to ON Semiconductor and new part numbers

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