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MPS3906

General Purpose Transistor

High−Performance Silicon−Gate CMOS

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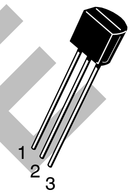
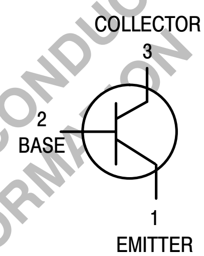


TO−92 (TO−226AA)
CASE 29−04
STYLE 1



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	−40	Vdc
Collector−Base Voltage	V_{CBO}	−40	Vdc
Emitter−Base Voltage	V_{EBO}	−5.0	Vdc
Collector Current — Continuous	I_C	−200	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Breakdown Voltage(1) (I_C = −1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	−40	—	Vdc
Collector−Base Breakdown Voltage (I_C = −10 μAdc, I_E = 0)	$V_{(BR)CBO}$	−40	—	Vdc
Emitter−Base Breakdown Voltage (I_E = −10 μAdc, I_C = 0)	$V_{(BR)EBO}$	−5.0	—	Vdc
Collector Cutoff Current (V_{CE} = −30 Vdc, $V_{EB(off)}$ = −3.0 Vdc)	I_{CEX}	—	−50	nAdc
Base Cutoff Current (V_{CE} = −30 Vdc, $V_{EB(off)}$ = −3.0 Vdc)	I_{BL}	—	−50	nAdc

1. Pulse Test: Pulse Width = 300 μs; Duty Cycle = 2.0%.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS[1]				
DC Current Gain	h_{FE}			—
(I_C = −0.1 mAdc, V_{CE} = −1.0 Vdc)		60	—	
(I_C = −1.0 mAdc, V_{CE} = −1.0 Vdc)		80	—	
(I_C = −10 mAdc, V_{CE} = −1.0 Vdc)		100	300	
(I_C = −50 mAdc, V_{CE} = −1.0 Vdc)		60	—	
(I_C = −100 mAdc, V_{CE} = −1.0 Vdc)		30	—	
Collector−Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = −10 mAdc, I_B = −1.0 mAdc)		—	−0.25	
(I_C = −50 mAdc, I_B = −5.0 mAdc)		—	−0.4	
Base−Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = −10 mAdc, I_B = −1.0 mAdc)		−0.65	−0.85	
(I_C = −50 mAdc, I_B = −5.0 mAdc)		—	−0.95	
SMALL−SIGNAL CHARACTERISTICS				
Current−Gain — Bandwidth Product (I_C = −10 mAdc, V_{CE} = −20 V, f = 100 MHz)	f_T	250	—	MHz
Output Capacitance (V_{CB} = −5.0 Vdc, I_E = 0, f = 1.0 MHz)	C_{obo}	—	4.5	pF
Input Capacitance (V_{EB} = −0.5 Vdc, I_C = 0, f = 1.0 MHz)	C_{ibo}	—	10	pF
Input Impedance (I_C = −1.0 mAdc, V_{CE} = −10 Vdc, f = 1.0 kHz)	h_{ie}	2.0	12	k Ω
Voltage Feedback Ratio (I_C = −1.0 mAdc, V_{CE} = −10 Vdc, f = 1.0 kHz)	h_{re}	1.0	10	X 10^{-4}
Small−Signal Current Gain (I_C = −1.0 mAdc, V_{CE} = −10 Vdc, f = 1.0 kHz)	h_{fe}	100	400	—
Output Admittance (I_C = −1.0 mAdc, V_{CE} = −10 Vdc, f = 1.0 kHz)	h_{oe}	3.0	60	μmhos
Noise Figure (I_C = −100 μAdc, V_{CE} = −5.0 Vdc, R_S = 1.0 k Ω, f = 1.0 kHz)	NF	—	4.0	dB
SWITCHING CHARACTERISTICS				
Delay Time (V_{CC} = −3.0 Vdc, $V_{BE(off)}$ = +0.5 Vdc, I_C = −10 mAdc, I_{B1} = 1.0 mAdc)	t_d	—	35	ns
Rise Time (V_{CC} = −3.0 Vdc, $V_{BE(off)}$ = +0.5 Vdc, I_C = −10 mAdc, I_{B1} = 1.0 mAdc)	t_r	—	50	ns
Storage Time (V_{CC} = −3.0 Vdc, I_C = −10 mAdc, I_{B1} = I_{B2} = −1.0 mAdc)	t_s	—	600	ns
Fall Time (V_{CC} = −3.0 Vdc, I_C = −10 mAdc, I_{B1} = I_{B2} = −1.0 mAdc)	t_f	—	90	ns

1. Pulse Test: Pulse Width = 300 μs; Duty Cycle = 2.0%.

TYPICAL NOISE CHARACTERISTICS

(V_{CE} = −5.0 Vdc, T_A = 25°C)

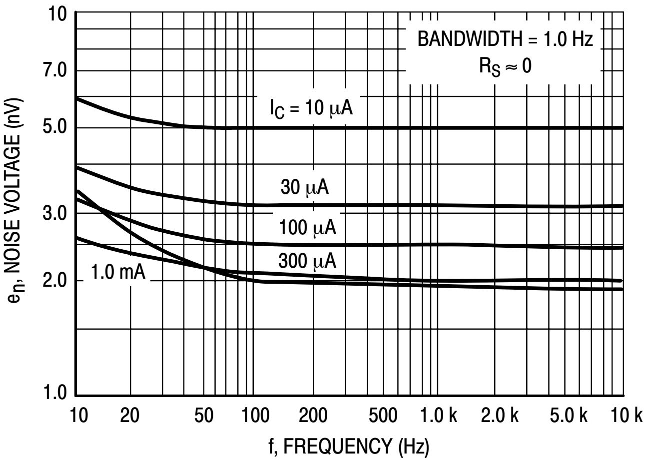


Figure 1. Noise Voltage

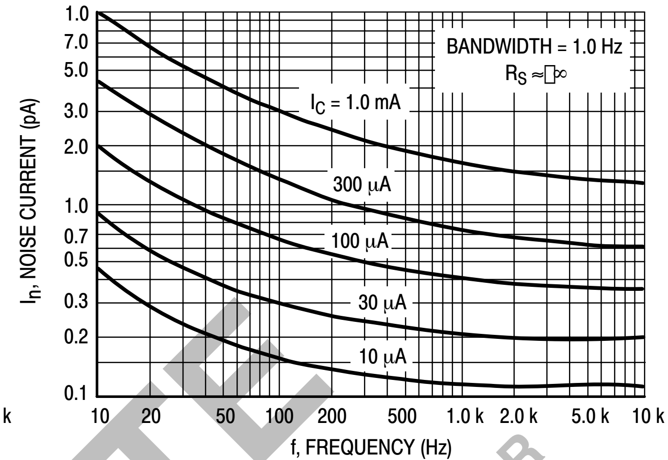


Figure 2. Noise Current

NOISE FIGURE CONTOURS

(V_{CE} = −5.0 Vdc, T_A = 25°C)

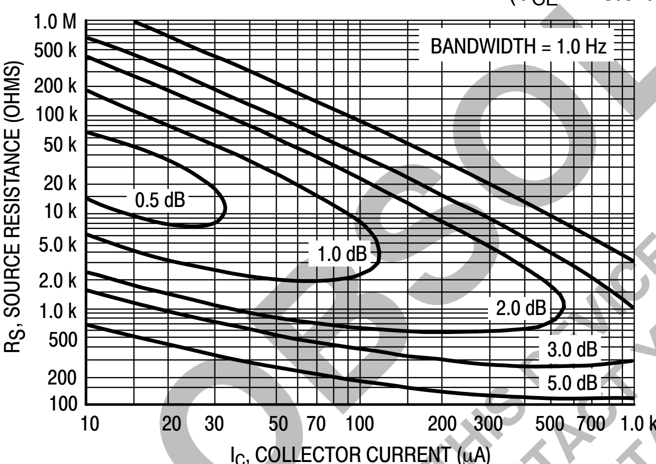


Figure 3. Narrow Band, 100 Hz

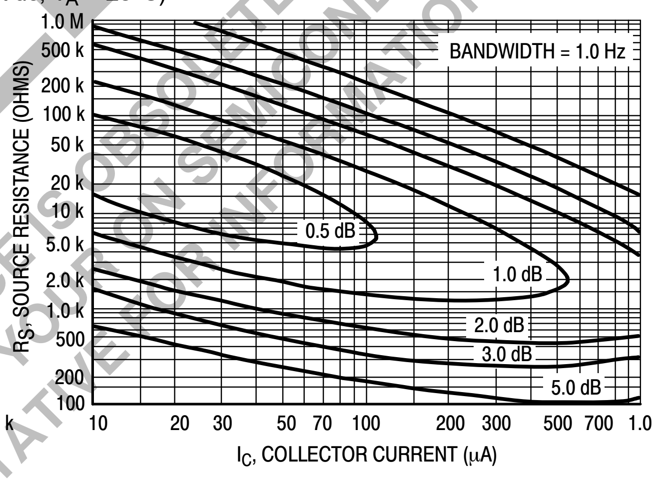


Figure 4. Narrow Band, 1.0 kHz

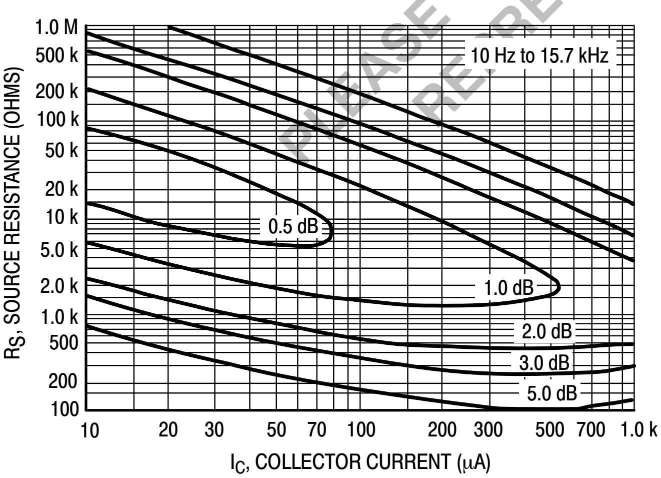


Figure 5. Wideband

Noise Figure is Defined as:

$$NF = 20 \log_{10}\left[\frac{e_n^2 + 4KTR_S + I_n^2 R_S^2}{4KTR_S}\right]^{1/2}$$

e_n = Noise Voltage of the Transistor referred to the input. (Figure 3)
I_n = Noise Current of the Transistor referred to the input. (Figure 4)
K = Boltzman's Constant (1.38 x 10^{-23} j/°K)
T = Temperature of the Source Resistance (°K)
R_S = Source Resistance (Ohms)

TYPICAL STATIC CHARACTERISTICS

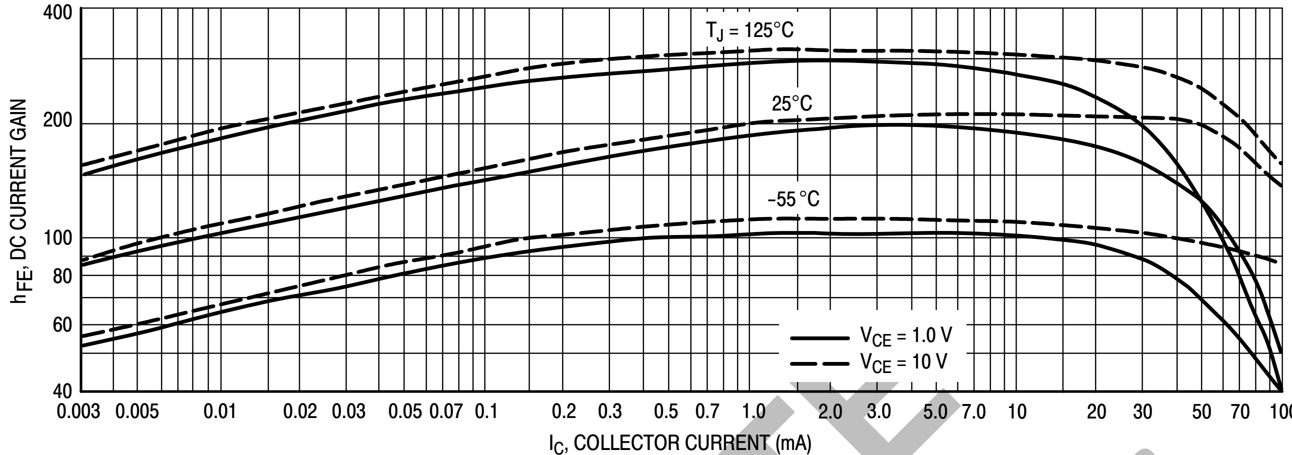


Figure 6. DC Current Gain

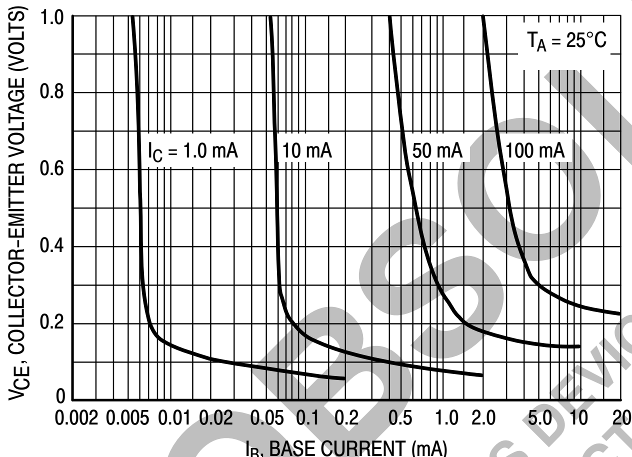


Figure 7. Collector Saturation Region

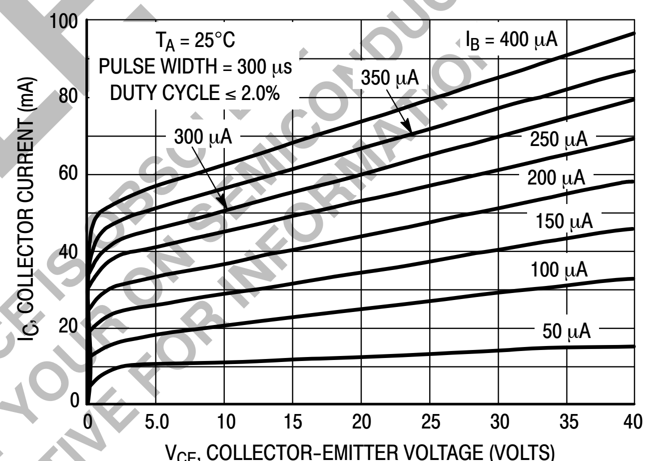


Figure 8. Collector Characteristics

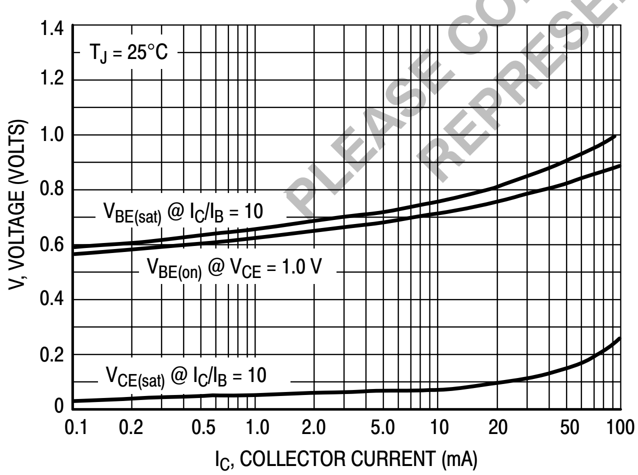


Figure 9. “On” Voltages

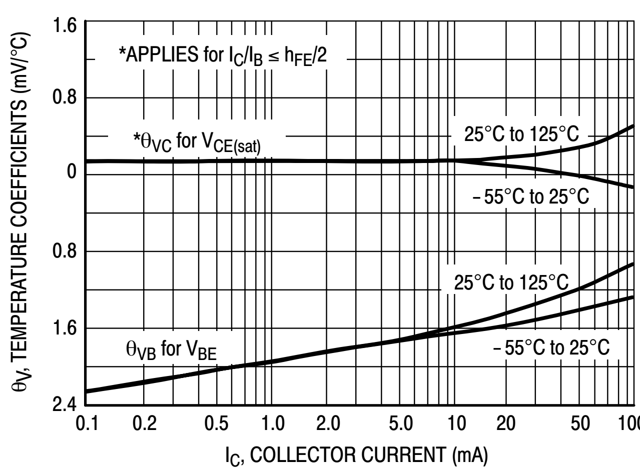


Figure 10. Temperature Coefficients

TYPICAL DYNAMIC CHARACTERISTICS

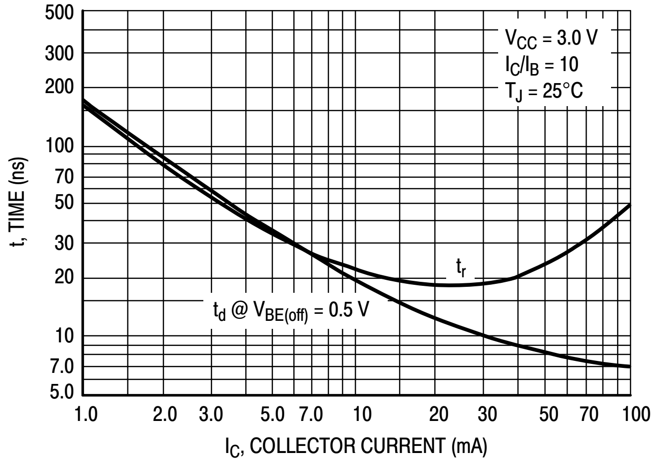


Figure 11. Turn−On Time

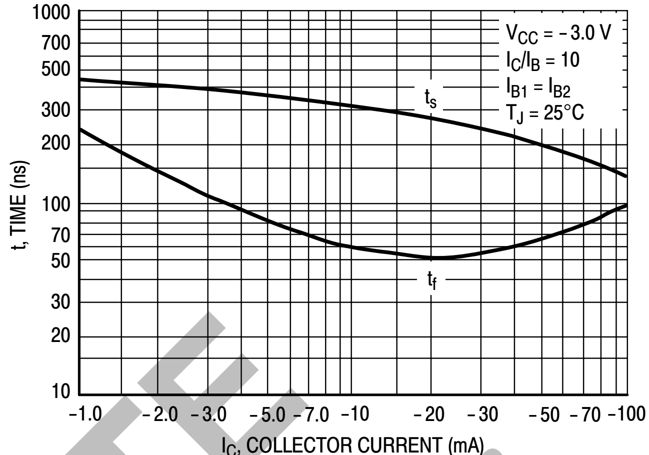


Figure 12. Turn−Off Time

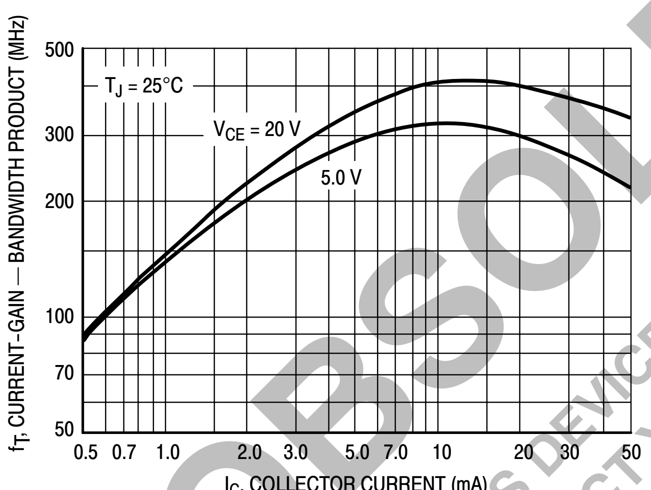


Figure 13. Current−Gain — Bandwidth Product

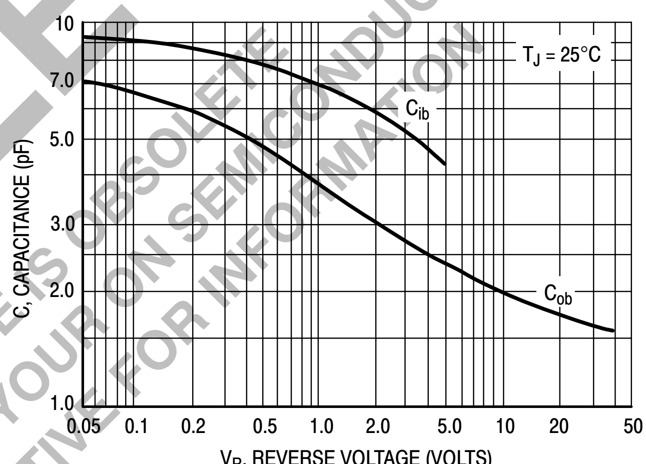


Figure 14. Capacitance

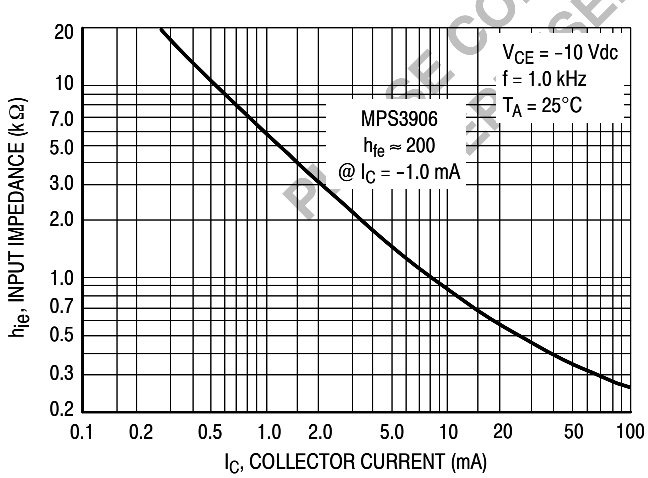


Figure 15. Input Impedance

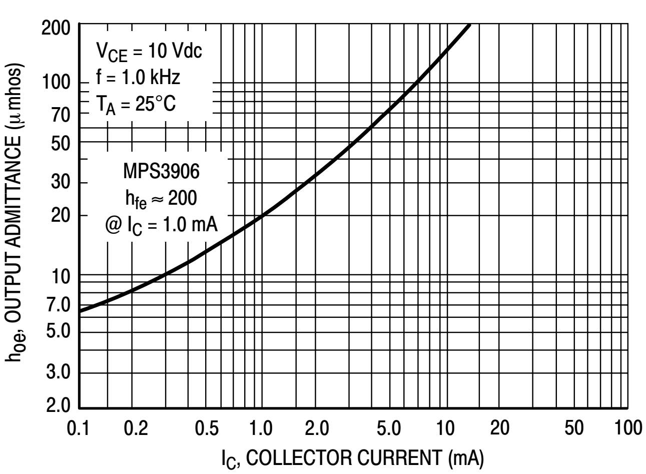


Figure 16. Output Admittance

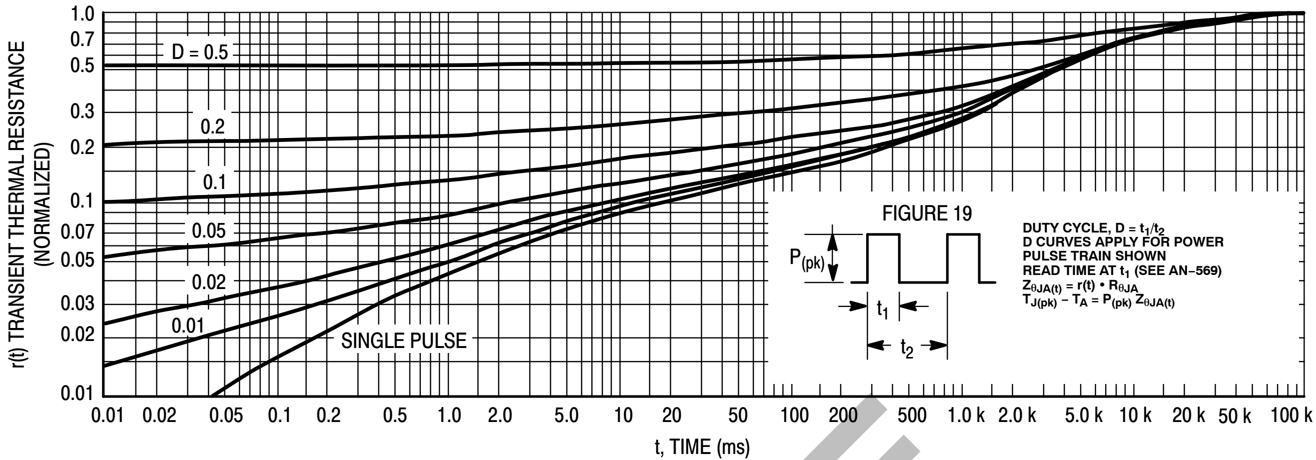


Figure 17. Thermal Response

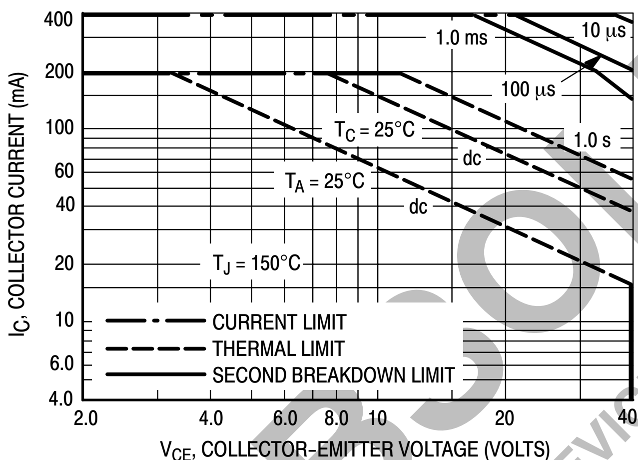


Figure 18. Active−Region Safe Operating Area

The safe operating area curves indicate I_C−V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 18 is based upon $T_{J(pk)}$ = 150°C; T_C or T_A is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 17. At high case or ambient temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

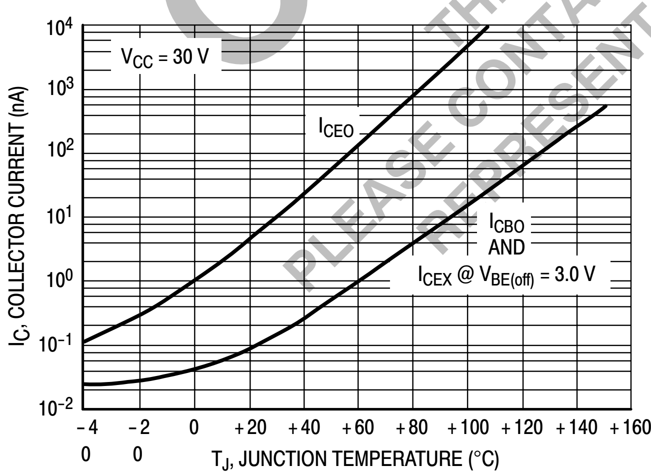


Figure 19. Typical Collector Leakage Current

DESIGN NOTE: USE OF THERMAL RESPONSE DATA

A train of periodical power pulses can be represented by the model as shown in Figure 19. Using the model and the device thermal response the normalized effective transient thermal resistance of Figure 17 was calculated for various duty cycles.

To find $Z_{\theta JA(t)}$, multiply the value obtained from Figure 17 by the steady state value $R_{\theta JA}$.

Example:

Dissipating 2.0 watts peak under the following conditions:

t_1 = 1.0 ms, t_2 = 5.0 ms (D = 0.2)

Using Figure 17 at a pulse width of 1.0 ms and D = 0.2, the reading of r(t) is 0.22.

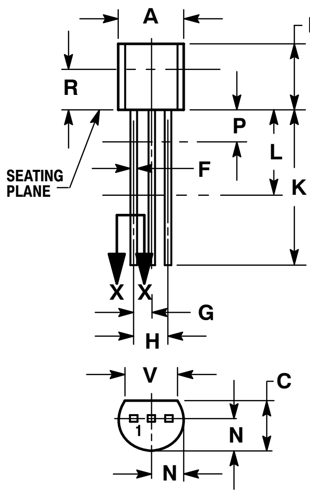
The peak rise in junction temperature is therefore

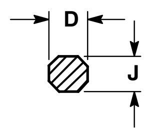
$\Delta T = r(t) \times P_{(pk)} \times R_{\theta JA} = 0.22 \times 2.0 \times 200 = 88°C$.

For more information, see AN−569.

PACKAGE DIMENSIONS

CASE 029–04
(TO–226AA)
ISSUE AD





SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

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