Octal D-Type Flip-Flops with Clear

MM74HC273

General Description

The MM74HC273 edge triggered flip−flops utilize advanced silicon−gate CMOS technology to implement D−type flip−flops. They possess high noise immunity, low power, and speeds comparable to low power Schottky TTL circuits. This device contains 8 master−slave flip−flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the LOW−to−HIGH transition of the CLOCK input. The CLEAR input when LOW, sets all outputs to a low state.

Each output can drive 10 low power Schottky TTL equivalent loads. The MM74HC273 is functionally as well as pin compatible to the 74LS273. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical Propagation Delay: 18 ns
- Wide Operating Voltage Range
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 160 μA (74 Series)
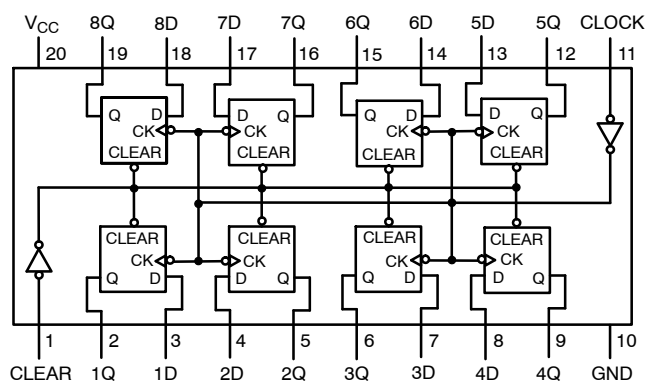- Output Drive: 10 LS−TTL Loads
- This is a Pb−Free Device

SOIC−20 WB
CASE 751D−05

SOIC−20, 300 mils
CASE 751BJ−01

TSSOP−20 WB
CASE 948E

MARKING DIAGRAMS

SOIC−20 WB


```
HC273A
AWLYYWW
```

TSSOP−20 WB


```
HC
273A
ALYW
```
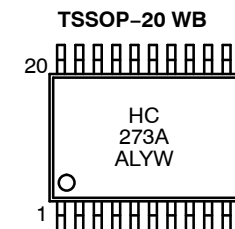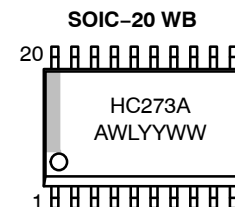
HC273A	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot Number
Y	= Year
WW, YW	= Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

Figure 1. Connection Diagram

TRUTH TABLE (Each Flip−Flop)

Inputs			Outputs
Clear	**Clock**	**D**	**Q**
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

NOTES:

H = HIGH Level (Steady State)
L = LOW Level (Steady State)
X = Don't Care
↑ = Transition from LOW−to−HIGH level
Q_0 = The level of Q before the indicated steady state input
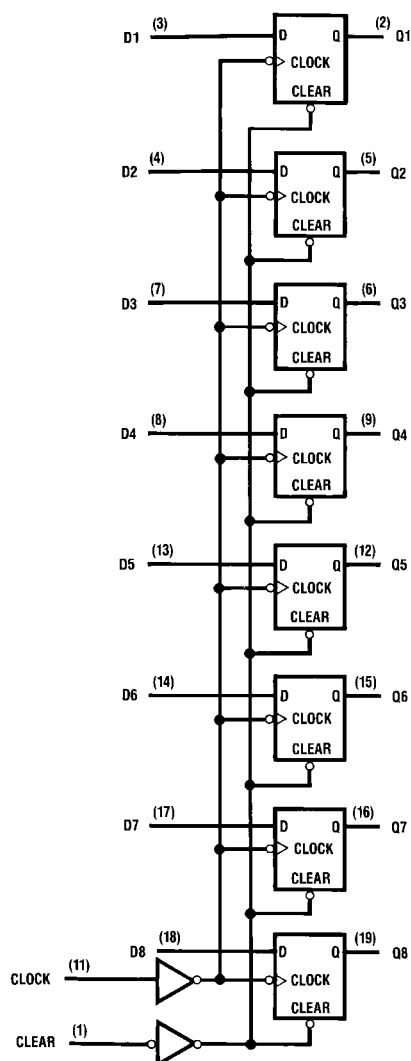conditions were established.

Figure 2. Logic Diagram

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Rating		Value	Unit
V_{CC}	Supply Voltage		−0.5 to +7.0 V	V
V_{IN}	DC Input Voltage		−0.5 to V_{CC} +0.5 V	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC} +0.5 V	V
I_{IK}, I_{OK}	Clamp Diode Current		±20	mA
I_{OUT}	DC Output Current, per pin		±25	mA
I_{CC}	DC V_{CC} or GND Current, per pin		±50	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
P_D	Power Dissipation	Note 2	600	mW
		S. O. Package only	500	mW
T_L	Lead Temperature (Soldering 10 seconds)		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Unless otherwise specified all voltages are referenced to ground.
2. Power Dissipation temperature derating – plastic "N" package: 12 mW/°C from 65°C to 85°C.

MM74HC273

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		2	6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage		0	V_{CC}	V
T_A	Operating Temperature Range		−55	125	°C
t_r, t_f	Input Rise or Fall Times	V_{CC} = 2.0 V	–	1000	ns
		V_{CC} = 4.5 V	–	500	ns
		V_{CC} = 6.0 V	–	400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Note 3)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C Typ	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C	Unit
					Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage		2.0 V		1.5	1.5	1.5	V
			4.5 V		3.15	3.15	3.15	V
			6.0 V		4.2	4.2	4.2	V
V_{IL}	Maximum LOW Level Input Voltage		2.0 V		0.5	0.5	0.5	V
			4.5 V		1.35	1.35	1.35	V
			6.0 V		1.8	1.8	1.8	V
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $|I_{OUT}| \leq$ 20 µA	2.0 V	2.0	1.9	1.9	1.9	V
			4.5 V	4.5	4.4	4.4	4.4	V
			6.0 V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $|I_{OUT}| \leq$ 4.0 mA	4.5 V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}| \leq$ 5.2 mA	6.0 V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $|I_{OUT}| \leq$ 20 µA	2.0 V	0	0.1	0.1	0.1	V
			4.5 V	0	0.1	0.1	0.1	V
			6.0 V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $|I_{OUT}| \leq$ 4.0 mA	4.5 V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}| \leq$ 5.2 mA	6.0 V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0 V		±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 µA	6.0 V		8	80	160	µA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. For a power supply of 5 V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V respectively. (The V_{IH} value at 5.5 V is 3.85 V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0 V values should be used.

AC ELECTRICAL CHARACTERISTICS
(V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, t_r = t_f = 6 ns)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Unit
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		18	27	ns
t_{PHL}	Maximum Propagation Delay, Clear to Output		18	27	ns
t_{REM}	Minimum Removal Time, Clear to Clock		10	20	ns
t_s	Minimum Setup Time, Data to Clock		10	20	ns
t_H	Minimum Hold Time, Clock to Data		−2	0	ns
t_W	Minimum Pulse Width, Clock to Clear		10	16	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS
(C_L = 50 pF, t_r = t_f = 6 ns, unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C Typ	T_A = 25°C Guaranteed Limits	T_A = −40 to 85°C	T_A = −55 to 125°C	Unit
f_{MAX}	Maximum Operating Frequency		2.0 V 4.5 V 6.0 V	16 74 78	5 27 31	4 21 24	3 18 20	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		2.0 V 4.5 V 6.0 V	38 14 12	135 27 23	170 34 29	205 41 35	ns ns ns
t_{PHL}	Maximum Propagation Delay, Clear to Output		2.0 V 4.5 V 6.0 V	42 19 18	135 27 23	170 34 29	205 41 35	ns ns ns
t_{REM}	Minimum Removal Time, Clear to Clock		2.0 V 4.5 V 6.0 V	0 0 0	25 5 4	32 6 5	37 7 6	ns ns ns
t_s	Minimum Setup Time, Data to Clock		2.0 V 4.5 V 6.0 V	26 7 5	100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time, Clock to Clock		2.0 V 4.5 V 6.0 V	−15 −6 −4	0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Pulse Width, Clock or Clear		2.0 V 4.5 V 6.0 V	34 11 10	80 16 14	100 20 18	120 24 20	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time, Clock		2.0 V 4.5 V 6.0 V	− − −	1000 500 400	1000 500 400	1000 500 400	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0 V 4.5 V 6.0 V	28 11 9	75 15 13	95 19 16	110 22 19	ns ns ns

AC ELECTRICAL CHARACTERISTICS (continued)
(C_L = 50 pF, t_r = t_f = 6 ns, unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C		Unit
				Typ	Guaranteed Limits			
C_{PD}	Power Dissipation Capacitance (Note 4)	(per flip−flop)		45				pF
C_{IN}	Maximum Input Capacitance			7	10	10	10	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

ORDERING INFORMATION

Device	Package	Shipping[†]
MM74HC273WM	SOIC−20 WB (Pb−Free and Halide Free)	38 Units / Tube
MM74HC273WMX	SOIC−20, 300 mils (Pb−Free and Halide Free)	1000 / Tape & Reel
MM74HC273MTC	TSSOP−20 WB (Pb−Free)	75 Units / Tube
MM74HC273MTCX		2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SOIC−20, 300 mils
CASE 751BJ−01
ISSUE O

DATE 19 DEC 2008
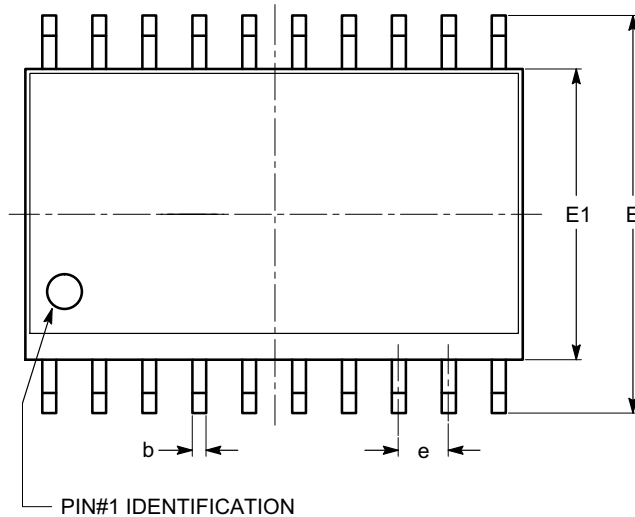
SYMBOL	MIN	NOM	MAX
A	2.36	2.49	2.64
A1	0.10		0.30
A2	2.05		2.55
b	0.31	0.41	0.51
c	0.20	0.27	0.33
D	12.60	12.80	13.00
E	10.01	10.30	10.64
E1	7.40	7.50	7.60
e	1.27 BSC		
h	0.25		0.75
L	0.40	0.81	1.27
θ	0º		8º
$\theta 1$	5º		15º

PIN#1 IDENTIFICATION

TOP VIEW
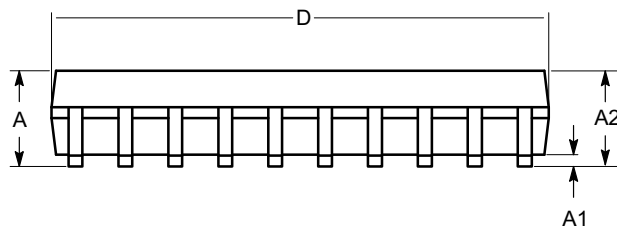
SIDE VIEW
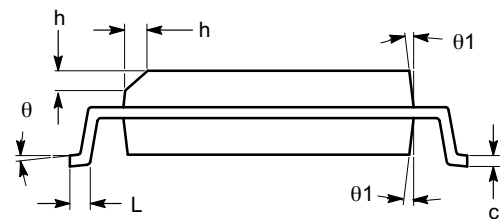
END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-013.

DOCUMENT NUMBER:	98AON34287E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−20, 300 MILS**		**PAGE 1 OF 1**

SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015

SCALE 1:1
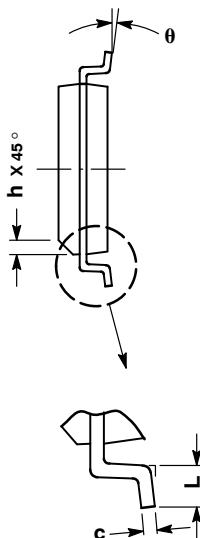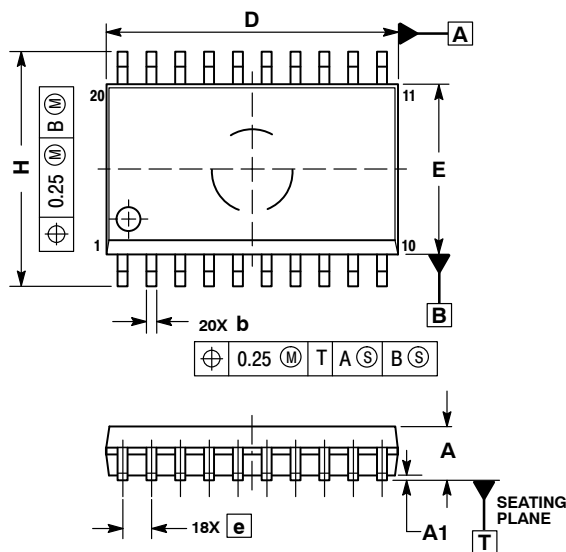
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

RECOMMENDED SOLDERING FOOTPRINT*

20X 0.52
20X 1.30
11.00
1.27
PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXXXXXXXX
XXXXXXXXXX
AWLYYWWG
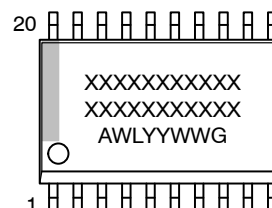
XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASB42343B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOIC−20 WB		PAGE 1 OF 1

TSSOP−20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

SCALE 2:1

$\oplus$ | 0.15 (0.006) | T | U | Ⓢ

20X **K** REF

$\oplus$ | 0.10 (0.004) | Ⓜ | T | U | Ⓢ | V | Ⓢ

2X **L/2**

L

PIN 1 IDENT

$\oplus$ | 0.15 (0.006) | T | U | Ⓢ

A
−V−

20   11
10

B
−U−

K
K1

J **J1**

SECTION N−N

N

0.25 (0.010)

M

N

F

DETAIL E

C
D **G** **H**

$\triangle$ | 0.100 (0.004)
−T− **SEATING PLANE**

−W−

DETAIL E

SOLDERING FOOTPRINT

7.06

1

0.65 PITCH

16X
0.36

16X
1.26

DIMENSIONS: MILLIMETERS
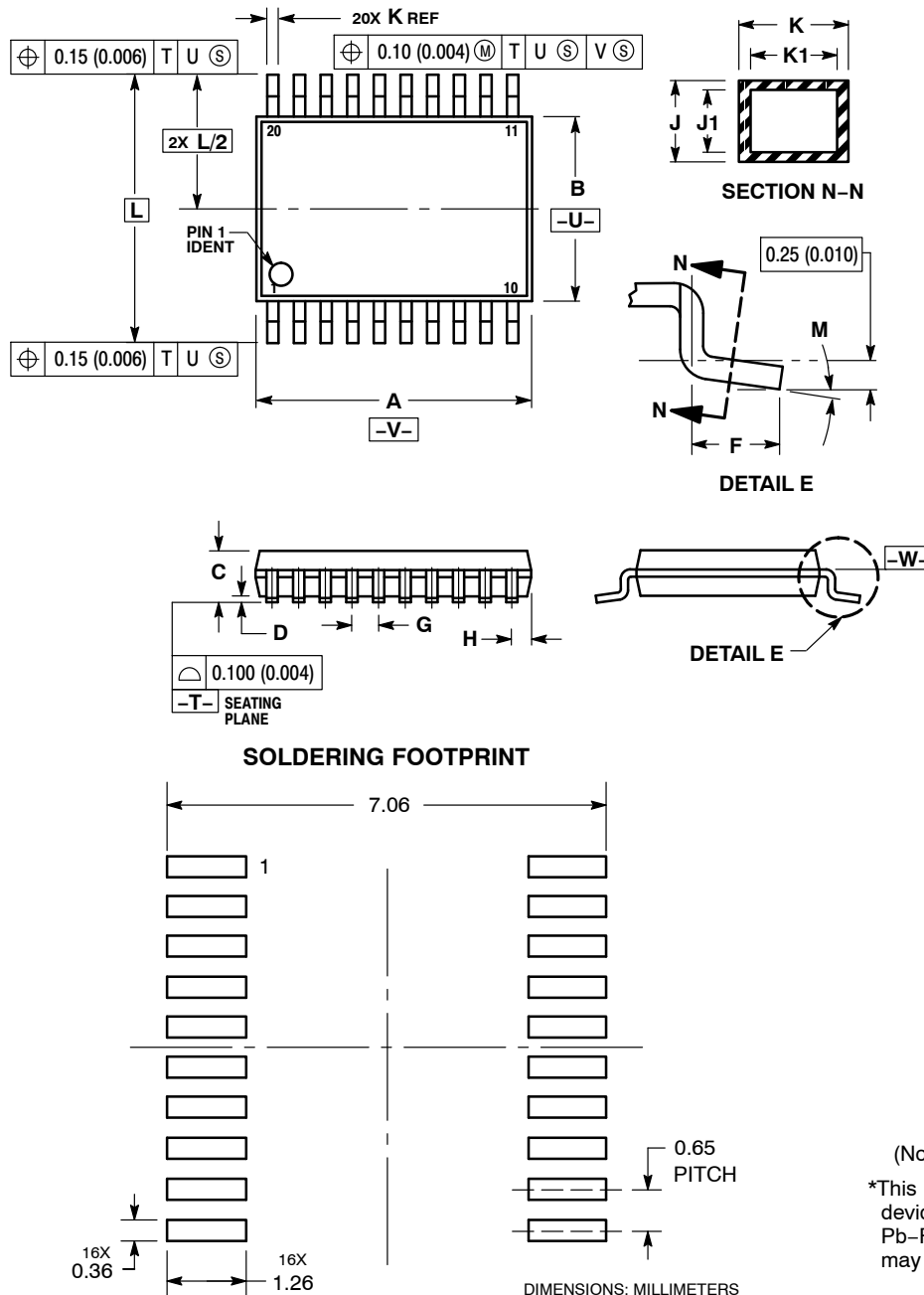
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

GENERIC MARKING DIAGRAM*

XXXX
XXXX
ALYW■

A   = Assembly Location
L   = Wafer Lot
Y   = Year
W   = Work Week
■   = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ■", may or may not be present.

DOCUMENT NUMBER:	98ASH70169A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	TSSOP−20 WB		PAGE 1 OF 1

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales