

MJE200G (NPN), MJE210G (PNP)

Complementary Silicon Power Plastic Transistors

These devices are designed for low voltage, low-power, high-gain audio amplifier applications.

Features

- High DC Current Gain
- Low Collector–Emitter Saturation Voltage
- High Current–Gain – Bandwidth Product
- Annular Construction for Low Leakage
- These Devices are Pb–Free and are RoHS Compliant*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	40	Vdc
Collector–Base Voltage	V_{CB}	25	Vdc
Emitter–Base Voltage	V_{EB}	8.0	Vdc
Collector Current – Continuous	I_C	5.0	Adc
Collector Current – Peak	I_{CM}	10	Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	15 0.12	W mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	1.5 0.012	W mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	8.34	$^\circ\text{C/W}$
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	83.4	$^\circ\text{C/W}$

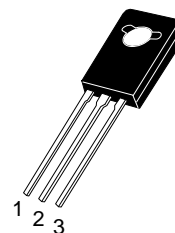
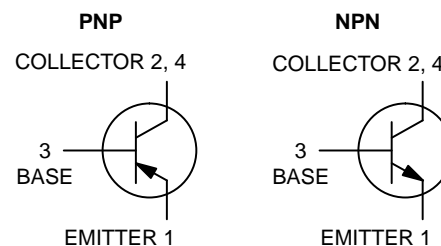
*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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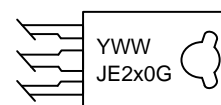
<http://onsemi.com>

5.0 AMPERES POWER TRANSISTORS COMPLEMENTARY SILICON 25 VOLTS, 15 WATTS



**TO-225
CASE 77-09
STYLE 1**

MARKING DIAGRAM



Y = Year
 WW = Work Week
 JE2x0 = Device Code
 x = 0 or 1
 G = Pb–Free Package

ORDERING INFORMATION

Device	Package	Shipping
MJE200G	TO–225 (Pb–Free)	500 Units / Box
MJE210G	TO–225 (Pb–Free)	500 Units / Box
MJE210TG	TO–225 (Pb–Free)	500 Units / Box

MJE200G (NPN), MJE210G (PNP)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (Note 1) (I _C = 10 mA _{dc} , I _B = 0)	V _{CEO(sus)}	25	–	V _{dc}
Collector Cutoff Current (V _{CB} = 40 V _{dc} , I _E = 0) (V _{CB} = 40 V _{dc} , I _E = 0, T _J = 125°C)	I _{CBO}	–	100	nA _{dc} μA _{dc}
Emitter Cutoff Current (V _{BE} = 8.0 V _{dc} , I _C = 0)	I _{EBO}	–	100	nA _{dc}

ON CHARACTERISTICS

DC Current Gain (Note 1) (I _C = 500 mA _{dc} , V _{CE} = 1.0 V _{dc}) (I _C = 2.0 A _{dc} , V _{CE} = 1.0 V _{dc}) (I _C = 5.0 A _{dc} , V _{CE} = 2.0 V _{dc})	h _{FE}	70 45 10	– 180 –	–
Collector–Emitter Saturation Voltage (Note 1) (I _C = 500 mA _{dc} , I _B = 50 mA _{dc}) (I _C = 2.0 A _{dc} , I _B = 200 mA _{dc}) (I _C = 5.0 A _{dc} , I _B = 1.0 A _{dc})	V _{CE(sat)}	– – –	0.3 0.75 1.8	V _{dc}
Base–Emitter Saturation Voltage (Note 1) (I _C = 5.0 A _{dc} , I _B = 1.0 A _{dc})	V _{BE(sat)}	–	2.5	V _{dc}
Base–Emitter On Voltage (Note 1) (I _C = 2.0 A _{dc} , V _{CE} = 1.0 V _{dc})	V _{BE(on)}	–	1.6	V _{dc}

DYNAMIC CHARACTERISTICS

Current–Gain – Bandwidth Product (Note 2) (I _C = 100 mA _{dc} , V _{CE} = 10 V _{dc} , f _{test} = 10 MHz)	f _T	65	–	MHz
Output Capacitance (V _{CB} = 10 V _{dc} , I _E = 0, f = 0.1 MHz) MJE200G MJE210G	C _{ob}	– –	80 120	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2.0%.

2. f_T = |h_{fe}| • f_{test}.

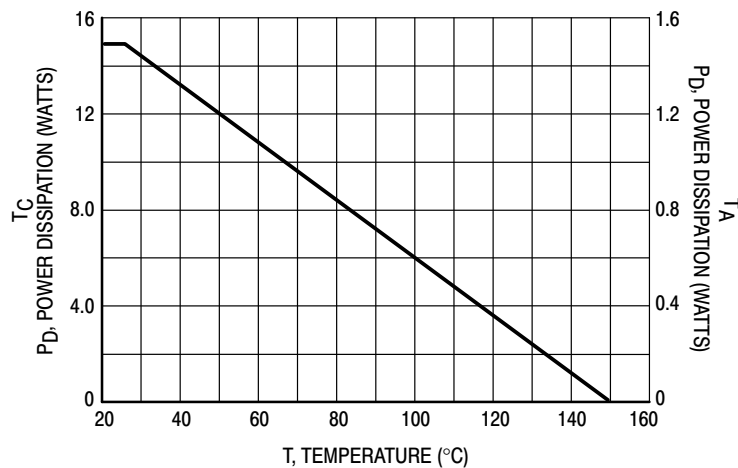


Figure 1. Power Derating

MJE200G (NPN), MJE210G (PNP)

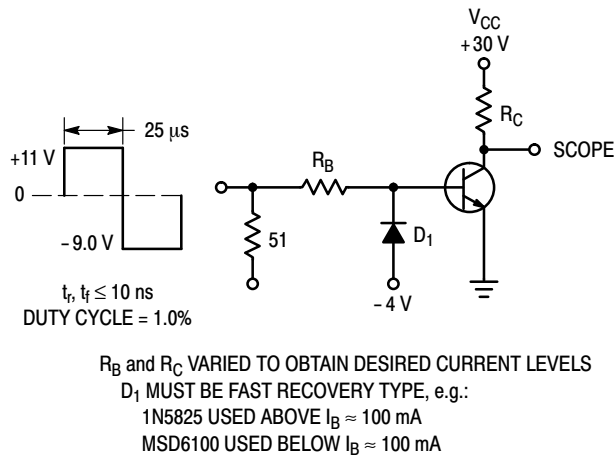


Figure 2. Switching Time Test Circuit

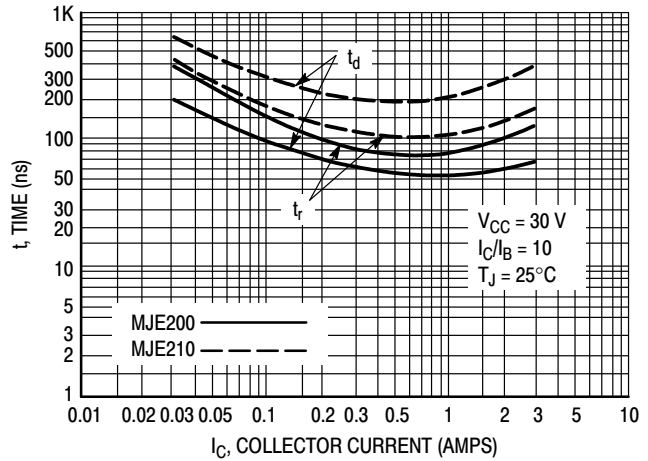


Figure 3. Turn-On Time

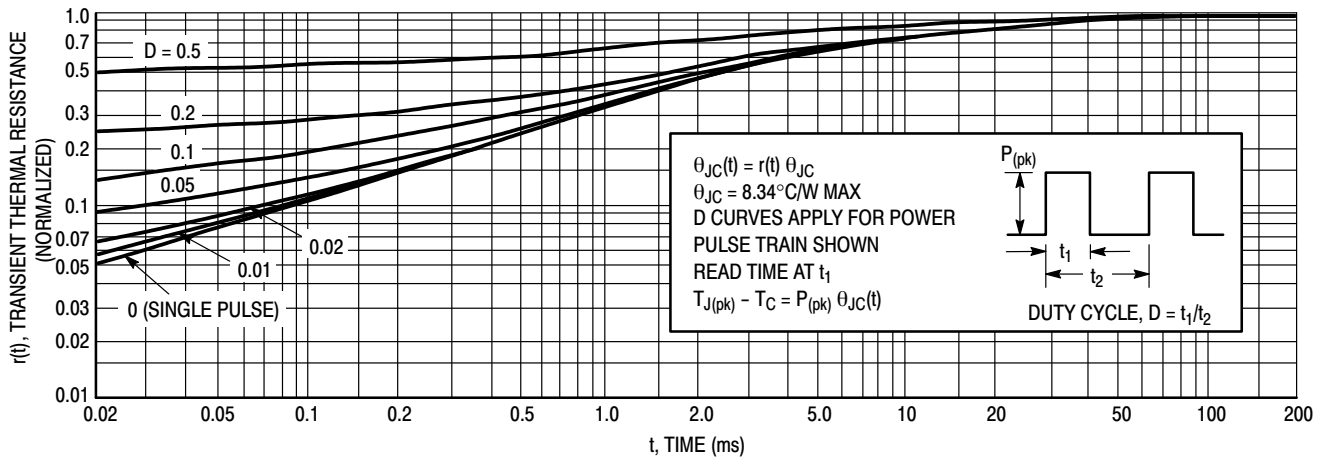


Figure 4. Thermal Response

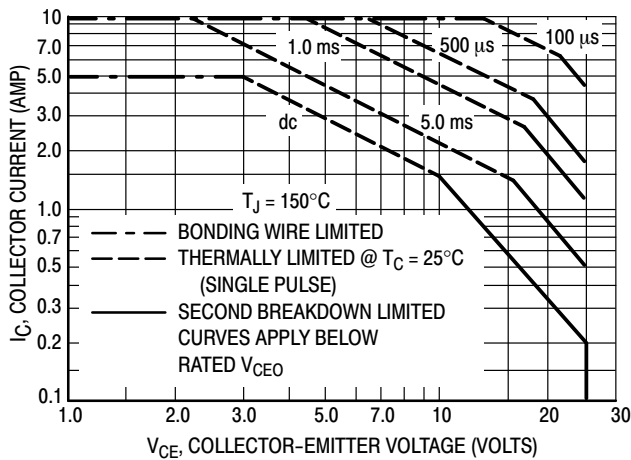


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

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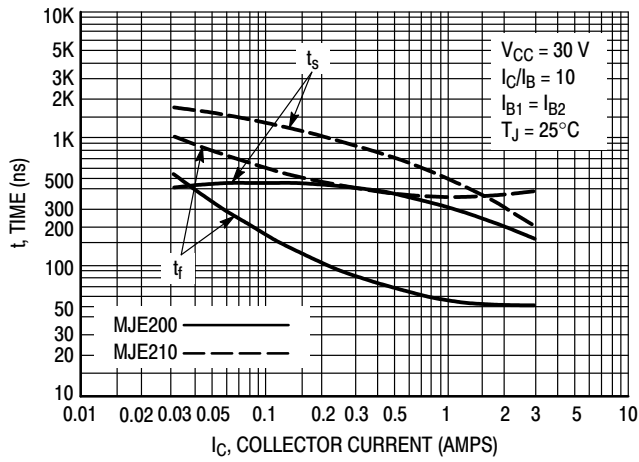


Figure 6. Turn-Off Time

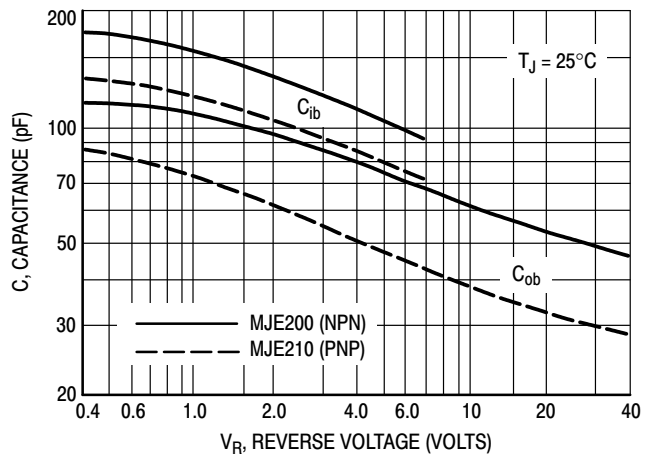


Figure 7. Capacitance

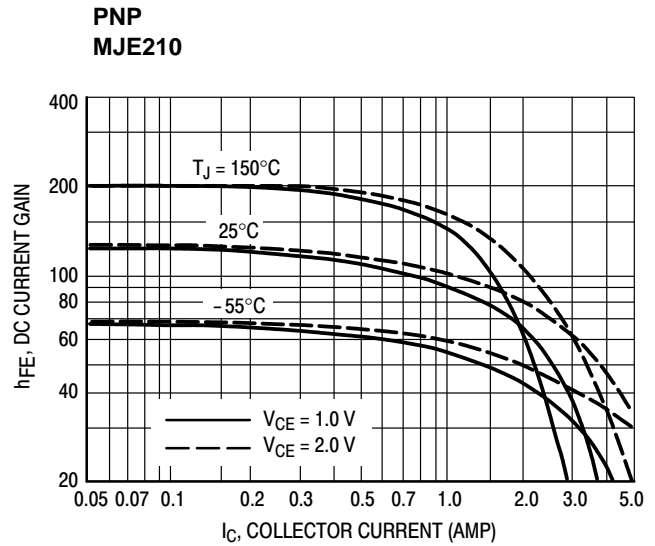
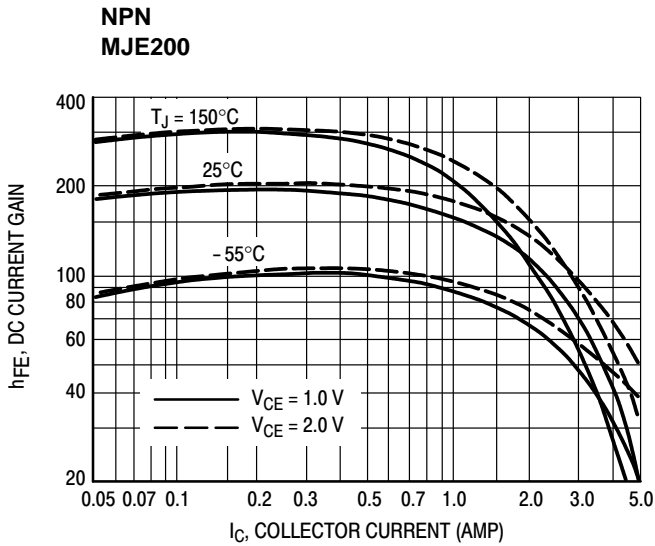


Figure 8. DC Current Gain

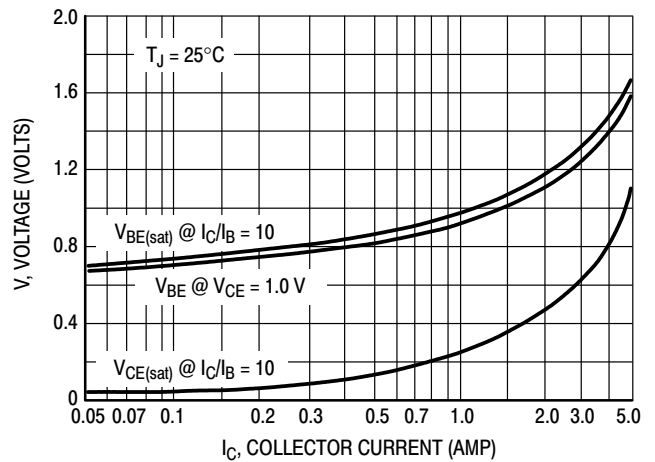
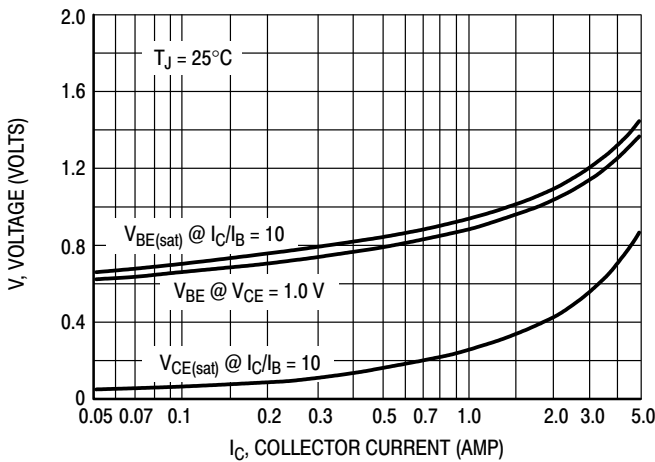


Figure 9. "On" Voltage

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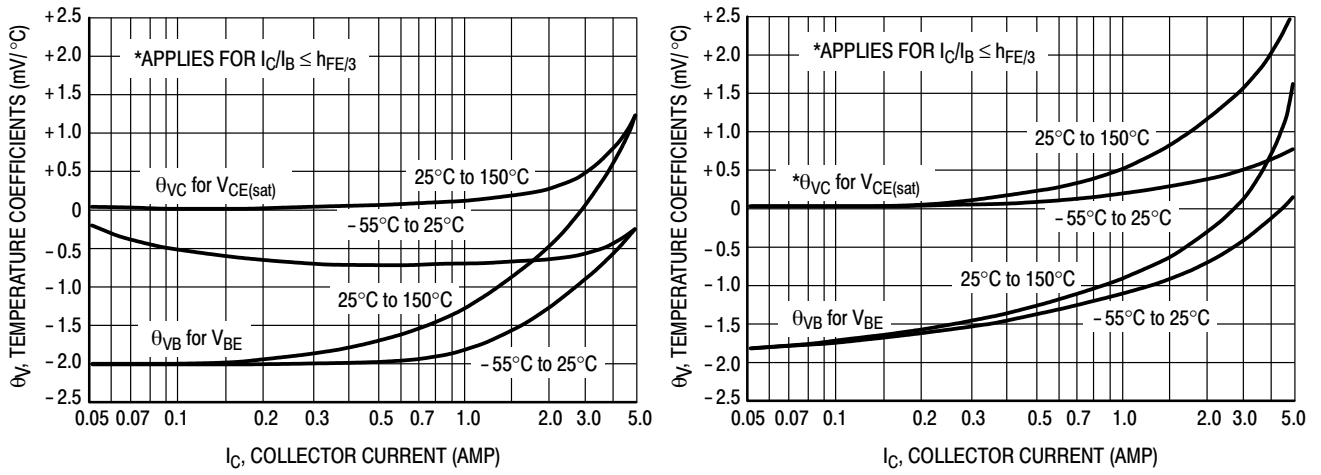
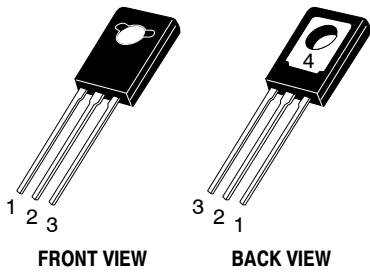


Figure 10. Temperature Coefficients

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



TO-225
CASE 77-09
ISSUE AD

DATE 25 MAR 2015

SCALE 1:1

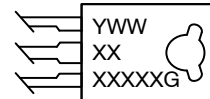


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. NUMBER AND SHAPE OF LUGS OPTIONAL.

DIM	MILLIMETERS	
	MIN	MAX
A	2.40	3.00
A1	1.00	1.50
b	0.60	0.90
b2	0.51	0.88
c	0.39	0.63
D	10.60	11.10
E	7.40	7.80
e	2.04	2.54
L	14.50	16.63
L1	1.27	2.54
P	2.90	3.30
Q	3.80	4.20

GENERIC MARKING DIAGRAM*



- Y = Year
- WW = Work Week
- XXXXX = Device Code
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present.

- | | | | | |
|---|---|---|---|---|
| <p>STYLE 1:
PIN 1. EMITTER
2., 4. COLLECTOR
3. BASE</p> | <p>STYLE 2:
PIN 1. CATHODE
2., 4. ANODE
3. GATE</p> | <p>STYLE 3:
PIN 1. BASE
2., 4. COLLECTOR
3. EMITTER</p> | <p>STYLE 4:
PIN 1. ANODE 1
2., 4. ANODE 2
3. GATE</p> | <p>STYLE 5:
PIN 1. MT 1
2., 4. MT 2
3. GATE</p> |
| <p>STYLE 6:
PIN 1. CATHODE
2., 4. GATE
3. ANODE</p> | <p>STYLE 7:
PIN 1. MT 1
2., 4. GATE
3. MT 2</p> | <p>STYLE 8:
PIN 1. SOURCE
2., 4. GATE
3. DRAIN</p> | <p>STYLE 9:
PIN 1. GATE
2., 4. DRAIN
3. SOURCE</p> | <p>STYLE 10:
PIN 1. SOURCE
2., 4. DRAIN
3. GATE</p> |

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