MC74LVX74

Dual D-Type Flip-Flop with Set and Clear

With 5.0 V−Tolerant Inputs

The MC74LVX74 is an advanced high speed CMOS D−type flip−flop. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

The signal level applied to the D input is transferred to O output during the positive going transition of the Clock pulse.

Clear ($\overline{CD}$) and Set ($\overline{SD}$) are independent of the Clock (CP) and are accomplished by setting the appropriate input Low.

Features

- High Speed: f_{max} = 145 MHz (Typ) at V_{CC} = 3.3 V
- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.5 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
  - Human Body Model > 2000 V;
  - Machine Model > 200 V
- These Devices are Pb−Free and are RoHS Compliant

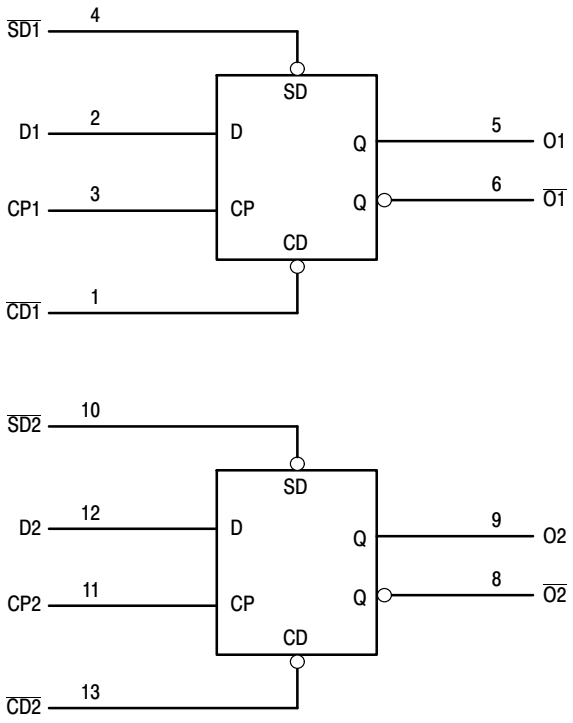

Figure 1. Logic Diagram

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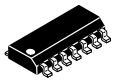
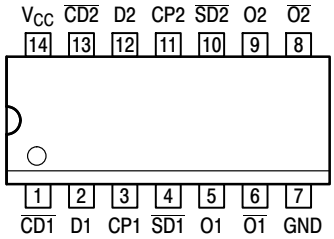
http://onsemi.com



SOIC−14 NB
D SUFFIX
CASE 751A

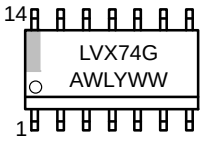
TSSOP−14
DT SUFFIX
CASE 948G

PIN ASSIGNMENT

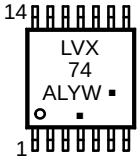


14−Lead (Top View)

MARKING DIAGRAMS



SOIC−14 NB



TSSOP−14

LVX74	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
W, WW	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN NAMES

Pins	Function
CP1, CP2	Clock Pulse Inputs
D1, D2	Data Inputs
$\overline{CD1}$, $\overline{CD2}$	Direct Clear Inputs
$\overline{SD1}$, $\overline{SD2}$	Direct Set Inputs
On, $\overline{On}$	Outputs

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

INPUTS				OUTPUTS		OPERATING MODE
$\overline{SDn}$	$\overline{CDn}$	CPn	Dn	On	$\overline{On}$	
L	H	X	X	H	L	Asynchronous Set
H	L	X	X	L	H	Asynchronous Clear
L	L	X	X	H	H	Undetermined
H	H	↑	h	H	L	Load and Read Register
H	H	↑	l	L	H	
H	H	↥	X	NC	NC	Hold

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Low−to−High Clock Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Low−to−High Clock Transition; NC = No Change; X = High or Low Voltage Level or Transitions are Acceptable; ↑ = Low−to−High Transition; ↥ = Not a Low−to−High Transition; For I_{CC} Reasons DO NOT FLOAT Inputs

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_{in}	DC Input Voltage	–0.5 to +7.0	V
V_{out}	DC Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current	−20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	–65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	−40	+85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = − 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High−Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low−Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High−Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = −50μA I_{OH} = −50μA I_{OH} = −4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low−Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND	3.6			±0.1		±1.0	μA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			2.0		20.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay CP to O or $\overline{O}$	V_{CC} = 2.7V	C_L = 15pF		7.3	15.0	1.0	18.5	ns
			C_L = 50pF		9.8	18.5	1.0	22.0	
		V_{CC} = 3.3 ± 0.3V	C_L = 15pF		5.7	9.7	1.0	11.5	
			C_L = 50pF		8.2	13.2	1.0	15.0	
t_{PLH}, t_{PHL}	Propagation Delay $\overline{SD}$ or $\overline{CD}$ to O or $\overline{O}$	V_{CC} = 2.7V	C_L = 15pF		8.4	15.6	1.0	18.5	ns
			C_L = 50pF		10.9	19.1	1.0	22.0	
		V_{CC} = 3.3 ± 0.3V	C_L = 15pF		6.6	10.1	1.0	12.0	
			C_L = 50pF		9.1	13.6	1.0	15.5	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	V_{CC} = 2.7V	C_L = 15pF	55	135		50		MHz
			C_L = 50pF	45	60		40		
		V_{CC} = 3.3 ± 0.3V	C_L = 15pF	95	145		80		
			C_L = 50pF	60	85		50		
t_{OSHL} t_{OSLH}	Output−to−Output Skew (Note 1)	V_{CC} = 2.7V	C_L = 50pF			1.5		1.5	ns
		V_{CC} = 3.3 ±0.3V	C_L = 50pF			1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH−to−LOW (t_{OSHL}) or LOW−to−HIGH (t_{OSLH}); parameter guaranteed by design.

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit $T_A = 25°C$	Guaranteed Limit $T_A = -40$ to $85°C$	Unit
t_w	Minimum Pulse Width, CP	2.7V	8.5	10.0	ns
		3.3V ±0.3	6.0	7.0	
t_w	Minimum Pulse Width, $\overline{CD}$ or $\overline{SD}$	2.7V	8.5	10.0	ns
		3.3V ±0.3	6.0	7.0	
t_{su}	Minimum Setup Time, D to CP	2.7V	8.0	9.5	ns
		3.3V ±0.3	5.5	6.5	
t_h	Minimum Hold Time, D to CP	2.7V	0.5	0.5	ns
		3.3V ±0.3	0.5	0.5	
t_{rec}	Minimum Recovery Time, $\overline{SD}$ or $\overline{CD}$ to CP	2.7V	6.5	7.5	ns
		3.3V ±0.3	5.0	5.0	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
Cin	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 2)		25				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/2$ (per flip−flop). C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 3.3$V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−0.3	−0.5	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

SWITCHING WAVEFORMS

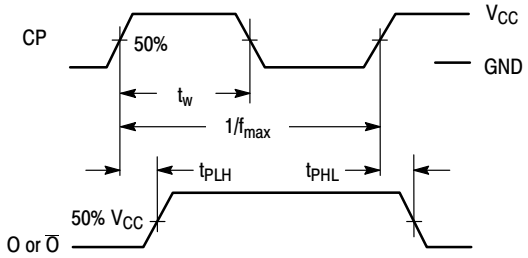


Figure 2.

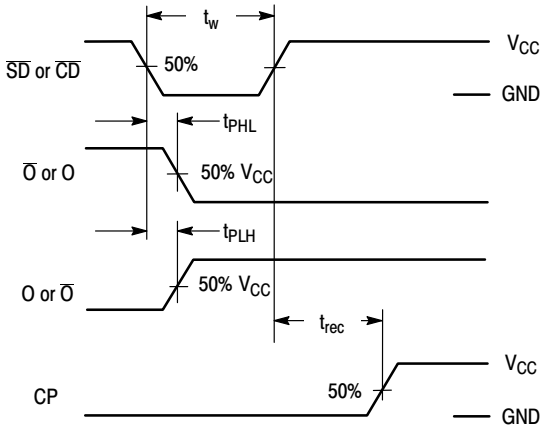


Figure 3.

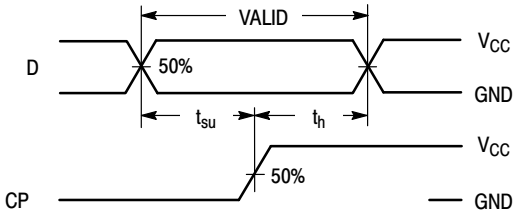
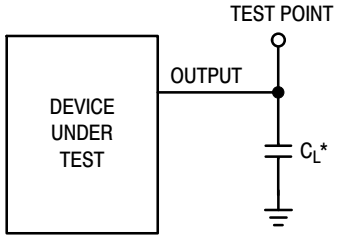


Figure 4.

TEST CIRCUIT



*Includes all probe and jig capacitance

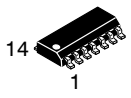
Figure 5.

ORDERING INFORMATION

Device	Package	Shipping†
MC74LVX74DR2G	SOIC−14 NB (Pb−Free)	2500 Tape & Reel
MC74LVX74DTG	TSSOP−14 (Pb−Free)	96 Units / Rail
MC74LVX74DTR2G	TSSOP−14 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

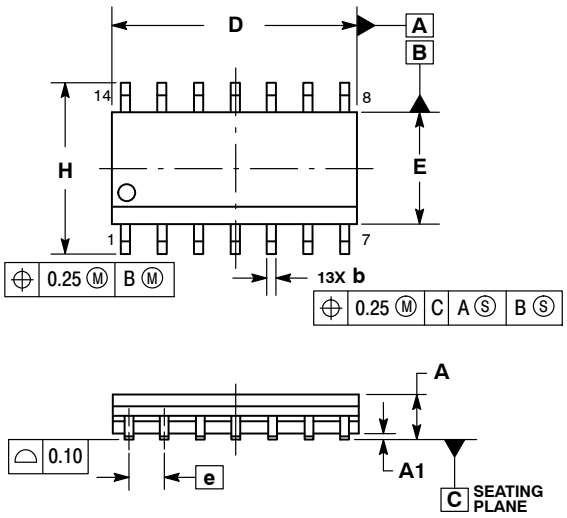
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

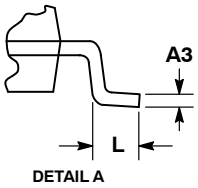


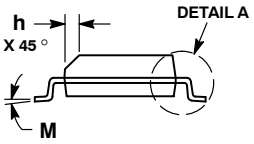
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



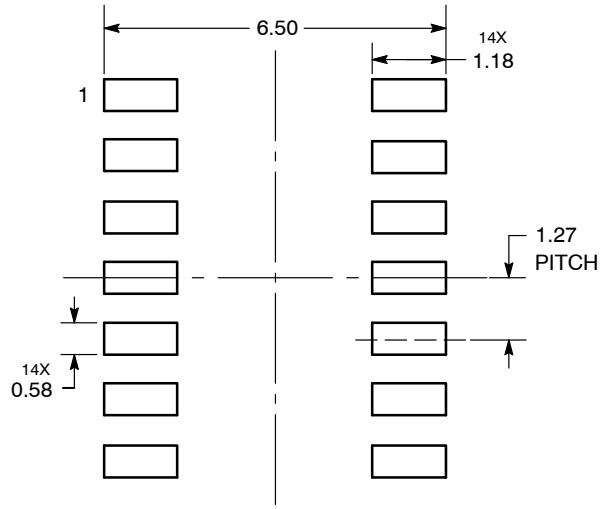




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

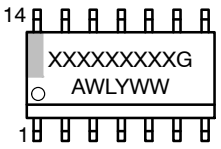
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42565B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOIC−14 NB**		**PAGE 1 OF 2**

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

ADDITIONAL INFORMATION

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For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales