

# MC74LVX139

## Dual 2-to-4 Decoder/ Demultiplexer

The MC74LVX139 is an advanced high speed CMOS 2-to-4 decoder/demultiplexer fabricated with silicon gate CMOS technology.

When the device is enabled ( $\overline{E} = \text{low}$ ), it can be used for gating or as a data input for demultiplexing operations. When the enable input is held high, all four outputs are fixed high, independent of other inputs.

The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

### Features

- High Speed:  $t_{PD} = 6.0 \text{ ns}$  (Typ) at  $V_{CC} = 3.3 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 4 \mu\text{A}$  (Max) at  $T_A = 25^\circ\text{C}$
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 3.6 V Operating Range
- Low Noise:  $V_{OLP} = 0.5 \text{ V}$  (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- Chip Complexity: 100 FETs or 25 Equivalent Gates
- ESD Performance:
  - Human Body Model > 2000 V;
  - Machine Model > 200 V
- These Devices are Pb-Free and are RoHS Compliant

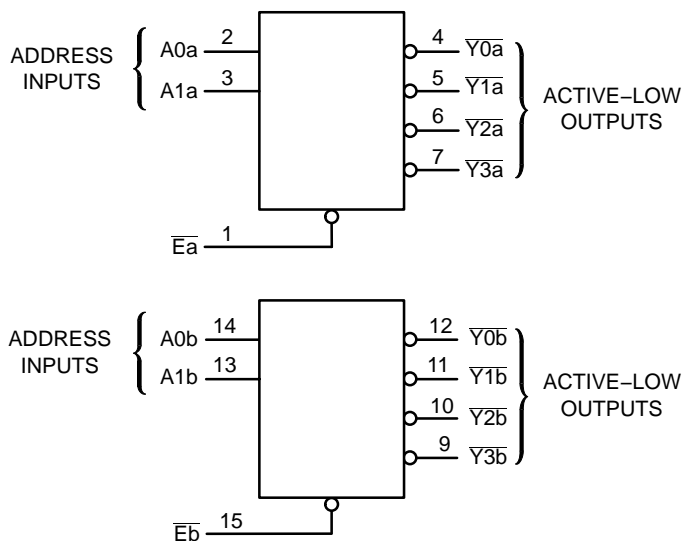
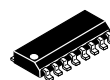


Figure 1. Logic Diagram



**ON Semiconductor®**

<http://onsemi.com>

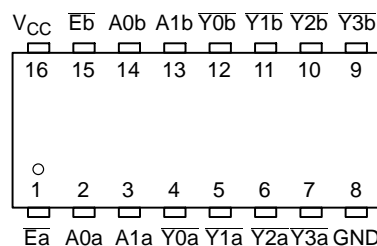


**SOIC-16  
D SUFFIX  
CASE 751B**

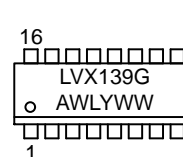


**TSSOP-16  
DT SUFFIX  
CASE 948F**

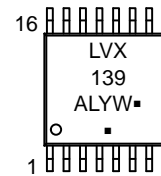
### PIN ASSIGNMENT



### MARKING DIAGRAMS



**SOIC-16**



**TSSOP-16**

LVX139 = Specific Device Code  
A = Assembly Location  
WL, L = Wafer Lot  
Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

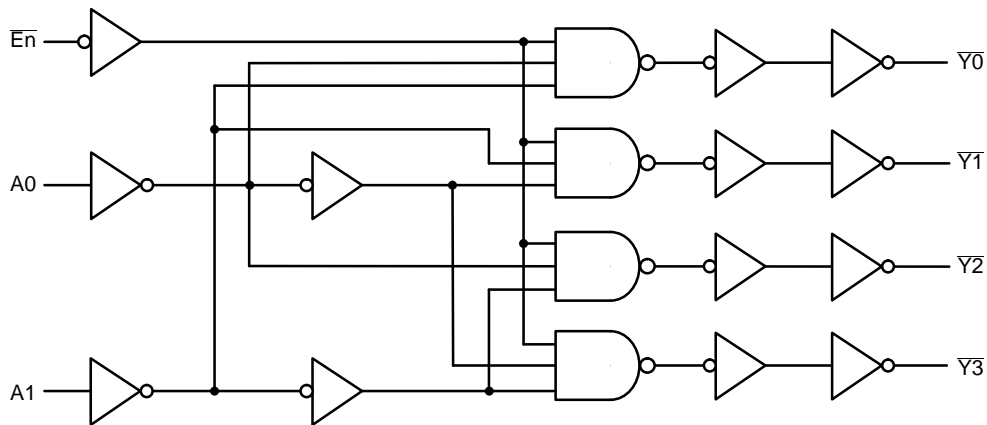
### FUNCTION TABLE

Inputs			Outputs			
E	A1	A0	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

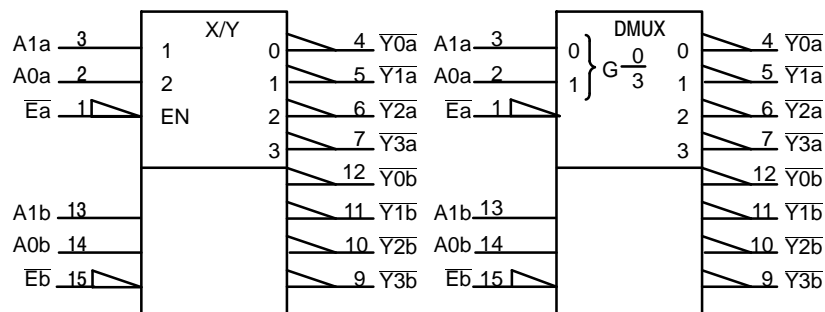
### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

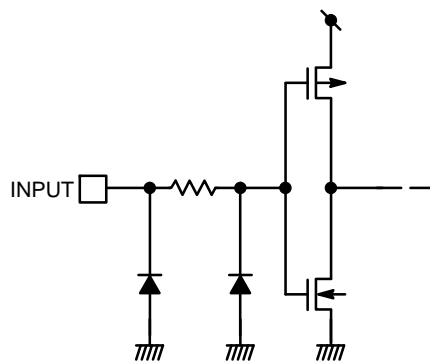
# MC74LVX139



**Figure 2. Expanded Logic Diagram**  
(1/2 of Device)



**Figure 3. IEC Logic Diagram**



**Figure 4. Input Equivalent Circuit**

# MC74LVX139

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Positive DC Supply Voltage	-0.5 to +7.0	V
$V_{IN}$	Digital Input Voltage	-0.5 to +7.0	V
$V_{OUT}$	DC Output Voltage	-0.5 to $V_{CC}$ +0.5	V
$I_{IK}$	Input Diode Current	-20	mA
$I_{OK}$	Output Diode Current	±20	mA
$I_{OUT}$	DC Output Current, per Pin	±25	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	±75	mA
$P_D$	Power Dissipation in Still Air SOIC Package TSSOP	200 180	mW
$T_{STG}$	Storage Temperature Range	-65 to +150	°C
$V_{ESD}$	ESD Withstand Voltage Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	> 2000 > 200 > 2000	V
$I_{LATCHUP}$	Latchup Performance Above $V_{CC}$ and Below GND at 125°C (Note 4)	±300	mA
$\theta_{JA}$	Thermal Resistance, Junction-to-Ambient SOIC Package TSSOP	143 164	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22-A114-A
2. Tested to EIA/JESD22-A115-A
3. Tested to JESD22-C101-A
4. Tested to EIA/JESD78

## RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
$V_{CC}$	DC Supply Voltage	2.0	3.6	V
$V_{IN}$	DC Input Voltage	0	5.5	V
$V_{OUT}$	DC Output Voltage Output in 3-State High or Low State	0	$V_{CC}$	V
$T_A$	Operating Temperature Range, all Package Types	-40	85	°C
$t_r, t_f$	Input Rise or Fall Time $V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# MC74LVX139

## DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			-40°C ≤ T <sub>A</sub> ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	Minimum High-Level Input Voltage		2.0 3.0 3.6	0.75 V <sub>CC</sub> 0.7 V <sub>CC</sub> 0.7 V <sub>CC</sub>	— — —	— — —	0.75 V <sub>CC</sub> 0.7 V <sub>CC</sub> 0.7 V <sub>CC</sub>	— — —	V
V <sub>IL</sub>	Maximum Low-Level Input Voltage		2.0 3.0 3.6	— — —	— — —	0.25 V <sub>CC</sub> 0.3 V <sub>CC</sub> 0.3 V <sub>CC</sub>	— — —	0.25 V <sub>CC</sub> 0.3 V <sub>CC</sub> 0.3 V <sub>CC</sub>	V
V <sub>OH</sub>	High-Level Output Voltage	I <sub>OH</sub> = -50 μA I <sub>OH</sub> = -50 μA I <sub>OH</sub> = -4 mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 3.0	— — —	1.9 2.9 2.48	— — —	V
V <sub>OL</sub>	Low-Level Output Voltage	I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 4 mA	2.0 3.0 3.0	— — —	0.0 — —	0.1 0.1 0.36	— — —	0.1 0.1 0.44	V
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	0 to 3.6	—	—	±0.1	—	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per package)	V <sub>IN</sub> = V <sub>CC</sub> or GND	3.6	1.0	1.0	2.0	—	—	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## AC ELECTRICAL CHARACTERISTICS Input t<sub>r</sub> = t<sub>f</sub> = 3.0 ns

Symbol	Parameter	Test Conditions		T <sub>A</sub> = 25°C			-40°C ≤ T <sub>A</sub> ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A to Y	V <sub>CC</sub> = 2.7 V	C <sub>L</sub> = 15 pF	–	8.5	15.0	1.0	17.8	ns
			C <sub>L</sub> = 50 pF	–	11.0	16.5	1.0	18.0	
		V <sub>CC</sub> = 3.3 V ± 0.3 V	C <sub>L</sub> = 15 pF	–	6.0	10.0	1.0	12.0	
			C <sub>L</sub> = 50 pF	–	8.5	13.0	1.0	15.0	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, E̅ to Y	V <sub>CC</sub> = 2.7 V	C <sub>L</sub> = 15 pF	–	8.0	13.0	1.0	15.5	ns
			C <sub>L</sub> = 50 pF	–	10.0	16.5	1.0	18.0	
		V <sub>CC</sub> = 3.3 V ± 0.3 V	C <sub>L</sub> = 15 pF	–	5.5	8.2	1.0	10.0	
			C <sub>L</sub> = 50 pF	–	7.5	13.0	1.0	15.0	
C <sub>IN</sub>	Maximum Input Capacitance			–	4	10	–	10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 5)	Typical @ 25°C, V <sub>CC</sub> = 3.3 V							pF
		26							

5. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/2 (per decoder). C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

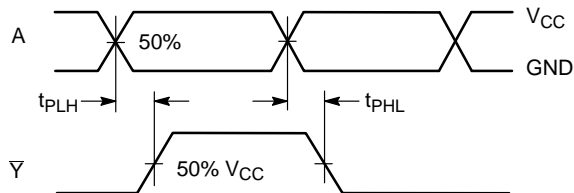


Figure 5. Switching Waveform

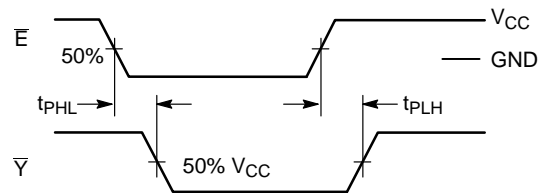
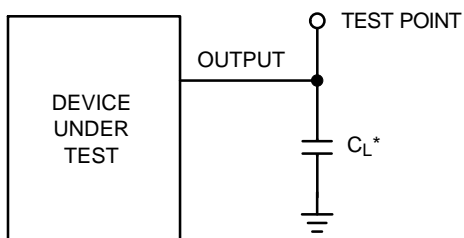


Figure 6. Switching Waveform

## MC74LVX139



\*Includes all probe and jig capacitance

**Figure 7. Test Circuit**

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC74LVX139DR2G	SOIC–16 (Pb–Free)	2500 Tape & Reel
MC74LVX139DTR2G	TSSOP–16 (Pb–Free)	2500 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

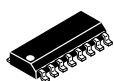
### EMBOSSED CARRIER DIMENSIONS (See Notes 6 and 7)

Tape Size	B <sub>1</sub> Max	D	D <sub>1</sub>	E	F	K	P	P <sub>0</sub>	P <sub>2</sub>	R	T	W
8 mm	4.35 mm (0.179")	1.5 mm + 0.1 – 0.0 (0.059" +0.004 – 0.0)	1.0 mm Min (0.179")	1.75 mm ±0.1 (0.069 ±0.004")	3.5 mm ±0.5 (1.38 ±0.002")	2.4 mm Max (0.094")	4.0 mm ±0.10 (0.157 ±0.004")	4.0 mm ±0.1 (0.157 ±0.004")	2.0 mm ±0.1 (0.079 ±0.004")	25 mm (0.98")	0.6 mm (0.024)	8.3 mm (0.327)
12 mm	8.2 mm (0.323")		1.5 mm Min (0.060)		5.5 mm ±0.5 (0.217 ±0.002")	6.4 mm Max (0.252")	4.0 mm ±0.10 (0.157 ±0.004") 8.0 mm ±0.10 (0.315 ±0.004")			30 mm (1.18")		12.0 mm ±0.3 (0.470 ±0.012")
16 mm	12.1 mm (0.476")				7.5 mm ±0.10 (0.295 ±0.004")	7.9 mm Max (0.311")	4.0 mm ±0.10 (0.157 ±0.004") 8.0 mm ±0.10 (0.315 ±0.004") 12.0 mm ±0.10 (0.472 ±0.004")					16.3 mm (0.642)
24 mm	20.1 mm (0.791")				11.5 mm ±0.10 (0.453 ±0.004")	11.9 mm Max (0.468")	16.0 mm ±0.10 (0.63 ±0.004")					24.3 mm (0.957)

6. Metric Dimensions Govern—English are in parentheses for reference only.

7. A<sub>0</sub>, B<sub>0</sub>, and K<sub>0</sub> are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

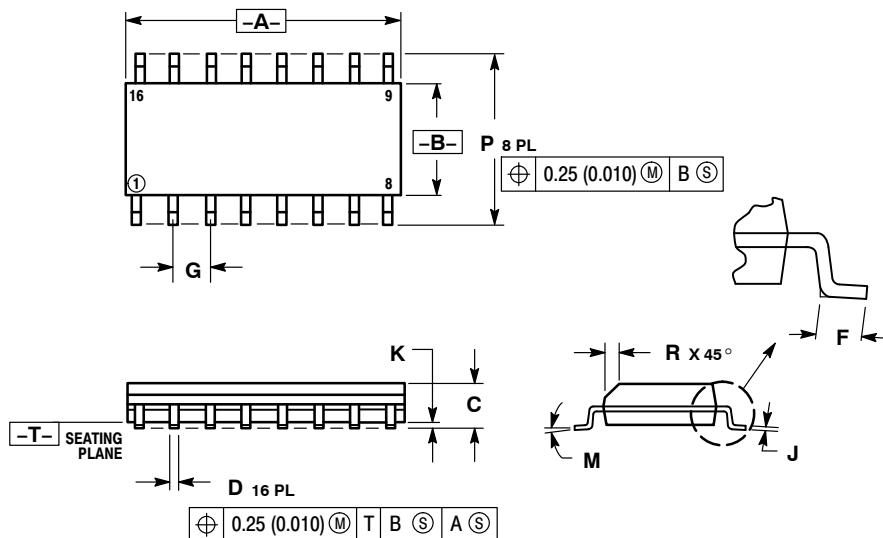
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

## SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



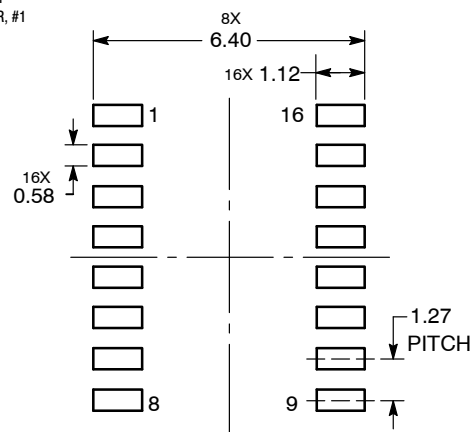
### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1: PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR 15. EMITTER 16. COLLECTOR	STYLE 2: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION 4. CATHODE 5. CATHODE 6. NO CONNECTION 7. ANODE 8. CATHODE 9. CATHODE 10. ANODE 11. NO CONNECTION 12. CATHODE 13. CATHODE 14. NO CONNECTION 15. ANODE 16. CATHODE	STYLE 3: PIN 1. COLLECTOR, DYE #1 2. BASE, #1 3. EMITTER, #1 4. COLLECTOR, #1 5. COLLECTOR, #2 6. BASE, #2 7. EMITTER, #2 8. COLLECTOR, #2 9. COLLECTOR, #3 10. BASE, #3 11. EMITTER, #3 12. COLLECTOR, #3 13. COLLECTOR, #4 14. BASE, #4 15. EMITTER, #4 16. COLLECTOR, #4	STYLE 4: PIN 1. COLLECTOR, DYE #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. COLLECTOR, #3 6. COLLECTOR, #3 7. COLLECTOR, #4 8. COLLECTOR, #4 9. BASE, #4 10. EMITTER, #4 11. BASE, #3 12. EMITTER, #3 13. BASE, #2 14. EMITTER, #2 15. BASE, #1 16. EMITTER, #1
STYLE 5: PIN 1. DRAIN, DYE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. DRAIN, #3 6. DRAIN, #3 7. DRAIN, #4 8. DRAIN, #4 9. GATE, #4 10. SOURCE, #4 11. GATE, #3 12. SOURCE, #3 13. GATE, #2 14. SOURCE, #2 15. GATE, #1 16. SOURCE, #1	STYLE 6: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. CATHODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE 15. ANODE 16. ANODE	STYLE 7: PIN 1. SOURCE N-CH 2. COMMON DRAIN (OUTPUT) 3. COMMON DRAIN (OUTPUT) 4. GATE P-CH 5. COMMON DRAIN (OUTPUT) 6. COMMON DRAIN (OUTPUT) 7. COMMON DRAIN (OUTPUT) 8. SOURCE P-CH 9. SOURCE P-CH 10. COMMON DRAIN (OUTPUT) 11. COMMON DRAIN (OUTPUT) 12. COMMON DRAIN (OUTPUT) 13. GATE N-CH 14. COMMON DRAIN (OUTPUT) 15. COMMON DRAIN (OUTPUT) 16. SOURCE N-CH	

### RECOMMENDED SOLDERING FOOTPRINT\*



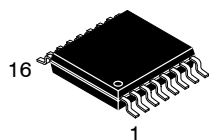
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-16	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**TSSOP-16 WB**  
**CASE 948F**  
**ISSUE B**

DATE 19 OCT 2006



## NOTES:

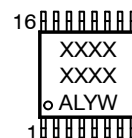
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

## RECOMMENDED SOLDERING FOOTPRINT\*



## GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

<b>DOCUMENT NUMBER:</b>	<b>98ASH70247A</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>TSSOP-16</b>	<b>PAGE 1 OF 1</b>

**onsemi** and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)