## 8-Input Data Selector/ Multiplexer with <br> 3-State Outputs <br> High-Performance Silicon-Gate CMOS

## MC74HC251A

The MC54/74HC251 is identical in pinout to the LS251. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device selects one of the eight binary Data Inputs, as determined by the Address Inputs. The Output Enable pin must be a low level for the selected data to appear at the outputs. If Output Enable is high, both the Y and the $\overline{\mathrm{Y}}$ outputs are in the high-impedance state. This 3-state feature allows the HC251 to be used in bus-oriented systems.

The HC251 is similar in function to the HC251 which does not have 3 -state outputs.

## Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: $1 \mu \mathrm{~A}$
- High Noise Immunity Characteristic of CMOS Devices
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are $\mathrm{Pb}-$ Free, Halogen Free/BFR Free and are RoHS Compliant

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| (Note: Microdot may be in either location) |  |  |
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ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.


FUNCTION TABLE

| Inputs |  |  |  | Outputs |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A2 | A1 | A0 | Output <br> Enabled | Y | P |
| X | X | X | H | Z | Z |
| L | L | L | L | D0 | D0 |
| L | L | H | L | D1 | D1 |
| L | H | L | L | D2 | D2 |
| H | L | H | L | D3 | D3 |
| H | L | H | L | D4 | D4 |
| H | H | L | L | D5 | D5 |
| H | H | H | L | D6 |  |

$\mathrm{Z}=$ high impedance
D0, $D 1, \ldots, D 7=$ the level of the respective D input.

Figure 1. Logic Diagram

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
| :---: | :--- | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| $\mathrm{~V}_{\text {in }}$ | DC Input Voltage (Referenced to GND) | -1.5 to $\mathrm{V}_{\mathrm{CC}}+1.5$ | V |
| $\mathrm{~V}_{\text {out }}$ | DC Output Voltage (Referenced to GND) | -0.5 to $\mathrm{V}_{\mathrm{CC}}+0.5$ | V |
| $\mathrm{I}_{\text {in }}$ | DC Input Current, per Pin | $\pm 25$ | mA |
| $\mathrm{I}_{\text {out }}$ | DC Output Current, per Pin | $\pm 50$ | mA |
| $\mathrm{I}_{\mathrm{CC}}$ | DC Supply Current, $\mathrm{V}_{\mathrm{CC}}$ and GND Pins | $\pm 75$ | mA |
| $\mathrm{P}_{\mathrm{D}}$ | Power Dissipation in Still Air $\quad$SOIC Package <br> TSSOP Package | 500 | mW |
|  |  | TBD |  |
| $\mathrm{T}_{\text {stg }}$ | Storage Temperature | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, $V_{\text {in }}$ and $V_{\text {out }}$ should be constrained to the range $G N D \leq\left(V_{\text {in }}\right.$ or $\left.V_{\text {out }}\right) \leq V_{\text {Cc }}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $\mathrm{V}_{\mathrm{CC}}$ ). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
| :---: | :--- | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| $\mathrm{~V}_{\text {in }}, \mathrm{V}_{\text {out }}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | $\mathrm{~V}_{\mathrm{CC}}$ | V |
| $\mathrm{T}_{\mathrm{A}}$ | Operating Temperature, All Package Types | -55 | +125 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{t}_{\mathrm{r}}, \mathrm{t}_{\mathrm{f}}$ | Input Rise and Fall Time | $\mathrm{V}_{\mathrm{CC}}=2.0 \mathrm{~V}$ | 0 | 1000 |
|  | (Figure 2) | ns |  |  |
|  |  | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}$ | 0 | 500 |
|  | $\mathrm{~V}_{\mathrm{CC}}=6.0 \mathrm{~V}$ | 0 | 400 |  |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $\stackrel{\mathrm{v}_{\mathrm{Cc}}}{\mathbf{V}}$ | Guaranteed Limit |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | $\begin{gathered} -55 \text { to } \\ 25^{\circ} \mathrm{C} \end{gathered}$ | $\leq 85^{\circ} \mathrm{C}$ | $\leq 125^{\circ} \mathrm{C}$ |  |
| $\mathrm{V}_{\mathrm{IH}}$ | Minimum High-Level Input Voltage | $\begin{aligned} & \mathrm{V}_{\text {out }}=0.1 \mathrm{~V} \text { or } \mathrm{V}_{\mathrm{CC}}-0.1 \mathrm{~V} \\ & \left.\right\|_{\text {lout }} \leq 20 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{gathered} \hline 1.5 \\ 3.15 \\ 4.2 \end{gathered}$ | $\begin{gathered} \hline 1.5 \\ 3.15 \\ 4.2 \end{gathered}$ | $\begin{gathered} \hline 1.5 \\ 3.15 \\ 4.2 \end{gathered}$ | V |
| $\mathrm{V}_{\text {IL }}$ | Maximum Low-Level Input Voltage | $\begin{aligned} & \mathrm{V}_{\text {out }}=0.1 \mathrm{~V} \text { or } \mathrm{V}_{\mathrm{CC}}-0.1 \mathrm{~V} \\ & \left.\right\|_{\text {lout }} \leq 20 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 0.3 \\ & 0.9 \\ & 1.2 \end{aligned}$ | $\begin{aligned} & 0.3 \\ & 0.9 \\ & 1.2 \end{aligned}$ | $\begin{aligned} & 0.3 \\ & 0.9 \\ & 1.2 \end{aligned}$ | V |
| $\mathrm{V}_{\mathrm{OH}}$ | Minimum High-Level Output Voltage | $\begin{aligned} & V_{\text {in }}=V_{\text {IH }} \text { or } V_{\text {IL }} \\ & \mid l_{\text {lout }} \leq 20 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 4.4 \\ & 5.9 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 4.4 \\ & 5.9 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 4.4 \\ & 5.9 \end{aligned}$ | V |
|  |  | $\begin{array}{ll}\mathrm{V}_{\text {in }}=\mathrm{V}_{\mathrm{IH}} \text { or } \mathrm{V}_{\mathrm{IL}} & \begin{array}{l}\left\|l_{\text {out }}\right\| \leq 4.0 \mathrm{~mA} \\ \mid \mathrm{l}_{\text {out }}\end{array} \leq 5.2 \mathrm{~mA}\end{array}$ | $\begin{aligned} & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 3.98 \\ & 5.48 \end{aligned}$ | $\begin{aligned} & 3.84 \\ & 5.34 \end{aligned}$ | $\begin{aligned} & 3.70 \\ & 5.20 \end{aligned}$ |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Maximum Low-Level Output Voltage | $\begin{aligned} & V_{\text {in }}=V_{\text {IH }} \text { or } V_{\text {IL }} \\ & \mid l_{\text {lout }} \leq 20 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & \hline 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & \hline 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & \hline 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | V |
|  |  | $\begin{array}{\|ll} \hline \mathrm{V}_{\text {in }}=\mathrm{V}_{\mathrm{IH}} \text { or } \mathrm{V}_{\mathrm{IL}} & \begin{array}{l} \mid l_{\text {out }} \leq 4.0 \mathrm{~mA} \\ \left\|\\|_{\text {out }}\right\| \leq 5.2 \mathrm{~mA} \end{array} \end{array}$ | $\begin{aligned} & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 0.26 \\ & 0.26 \end{aligned}$ | $\begin{aligned} & 0.33 \\ & 0.33 \end{aligned}$ | $\begin{aligned} & 0.40 \\ & 0.40 \end{aligned}$ |  |
| 1 in | Maximum Input Leakage Current | $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {CC }}$ or GND | 6.0 | $\pm 0.1$ | $\pm 1.0$ | $\pm 1.0$ | $\mu \mathrm{A}$ |
| loz | Maximum Three-State Leakage Current | Output in High-Impedance State $V_{\text {in }}=V_{I L}$ or $V_{I H}$ <br> $V_{\text {out }}=V_{C C}$ or $G N D$ | 6.0 | $\pm 0.5$ | $\pm 5.0$ | $\pm 10$ | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{CC}}$ | Maximum Quiescent Supply Current (per Package) | $\begin{aligned} & \mathrm{V}_{\text {in }}=\mathrm{V}_{\mathrm{CC}} \text { or GND } \\ & \mathrm{I}_{\text {out }}=0 \mu \mathrm{~A} \end{aligned}$ | 6.0 | 8 | 80 | 160 | $\mu \mathrm{A}$ |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS ( $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$, Input $\left.\mathrm{t}_{\mathrm{r}}=\mathrm{t}_{\mathrm{f}}=6 \mathrm{~ns}\right)$

| Symbol | Parameter | $\mathrm{v}_{\mathrm{cc}}$ | Guaranteed Limit |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\begin{gathered} -55 \text { to } \\ 25^{\circ} \mathrm{C} \end{gathered}$ | $\leq 85^{\circ} \mathrm{C}$ | $\leq 125^{\circ} \mathrm{C}$ |  |
| $\begin{aligned} & \mathrm{t}_{\mathrm{PLH}}, \\ & \mathrm{t}_{\mathrm{PH}}, \end{aligned}$ | Maximum Propagation Delay, Input $D$ to Output $Y$ or $\bar{Y}$ (Figures 2, 3 and 6) | $\begin{aligned} & \hline 2.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 185 \\ & 37 \\ & 31 \end{aligned}$ | $\begin{gathered} 230 \\ 46 \\ 39 \end{gathered}$ | $\begin{gathered} 280 \\ 56 \\ 48 \end{gathered}$ | ns |
| $\begin{aligned} & \hline \mathrm{t}_{\mathrm{PLH}}, \\ & \mathrm{t}_{\text {PH }} \end{aligned}$ | Maximum Propagation Delay, Input $A$ to Output $Y$ or $Y$ (Figures 3 and 6) | $\begin{aligned} & 2.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{gathered} 205 \\ 41 \\ 35 \end{gathered}$ | $\begin{gathered} 255 \\ 51 \\ 43 \end{gathered}$ | $\begin{gathered} 310 \\ 62 \\ 53 \end{gathered}$ | ns |
| $\begin{aligned} & \mathrm{t}_{\mathrm{PLLZ}}, \\ & \mathrm{t}_{\mathrm{PHZ}} \end{aligned}$ | Maximum Propagation Delay, Output Enable to Output Y (Figures 5 and 7) | $\begin{aligned} & 2.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{gathered} 195 \\ 39 \\ 33 \end{gathered}$ | $\begin{gathered} 245 \\ 49 \\ 42 \end{gathered}$ | $\begin{gathered} 295 \\ 59 \\ 50 \end{gathered}$ | ns |
| $\begin{aligned} & \text { tPZL, } \\ & \mathrm{t}_{\mathrm{PzH}} \end{aligned}$ | Maximum Propagation Delay, Output Enable to Output Y (Figures 5 and 7) | $\begin{aligned} & 2.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 145 \\ & 29 \\ & 25 \end{aligned}$ | $\begin{gathered} 180 \\ 36 \\ 31 \end{gathered}$ | $\begin{gathered} 220 \\ 44 \\ 38 \end{gathered}$ | ns |
| $\begin{aligned} & \text { tpLZ, } \\ & t_{\text {PHZ }} \end{aligned}$ | Maximum Propagation Delay, Output Enable to Output Y (Figures 5 and 7) | $\begin{aligned} & 2.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{gathered} 220 \\ 44 \\ 37 \end{gathered}$ | $\begin{gathered} 275 \\ 55 \\ 47 \end{gathered}$ | $\begin{gathered} 330 \\ 66 \\ 56 \end{gathered}$ | ns |
| $\begin{aligned} & \text { tpZL, } \\ & \mathrm{t}_{\text {PZH }} \end{aligned}$ | Maximum Propagation Delay, Output Enable to Output P (Figures 5 and 7) | $\begin{aligned} & 2.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & \hline 150 \\ & 30 \\ & 26 \end{aligned}$ | $\begin{aligned} & \hline 190 \\ & 38 \\ & 33 \end{aligned}$ | $\begin{gathered} 225 \\ 45 \\ 38 \end{gathered}$ | ns |
| $\begin{aligned} & \mathrm{t}_{\mathrm{T} \mathrm{~L}, \mathrm{H}}, \\ & \mathrm{t}_{\mathrm{TH}} \end{aligned}$ | Maximum Output Transition Time, Any Output (Figures 2 and 6) | $\begin{aligned} & \hline 2.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & \hline 75 \\ & 15 \\ & 13 \end{aligned}$ | $\begin{aligned} & 95 \\ & 19 \\ & 16 \end{aligned}$ | $\begin{aligned} & 110 \\ & 22 \\ & 19 \end{aligned}$ | ns |
| $\mathrm{C}_{\text {in }}$ | Maximum Input Capacitance | - | 10 | 10 | 10 | pF |
| $\mathrm{C}_{\text {out }}$ | Maximum Three-State Output Capacitance (Output in High-Impedance State) | - | 15 | 15 | 15 | pF |


|  |  | Typical @ $\mathbf{2 5}{ }^{\circ} \mathbf{C}, \mathbf{V}_{\mathbf{C C}}=\mathbf{5 . 0} \mathbf{V}$ |  |
| :---: | :---: | :---: | :---: |
| $\mathrm{C}_{\mathrm{PD}}$ | Power Dissipation Capacitance (Per Package) | 36 | pF |

## PIN DESCRIPTIONS

## INPUTS

## D0, D1, ..., D7 (Pins 4, 3, 2, 1, 15, 14, 13, 12)

Data inputs. Data on one of these eight binary inputs may be selected to appear on the output.

## CONTROL INPUTS

A0, A1, A2 (Pins 11, 10, 9)
Address inputs. The data on these pins are the binary address of the selected input (see the Function Table).

Output Enable (Pin 7)
Output Enable. This input pin must be at a low level for the selected data to appear at the outputs. If the Output Enable pin is high, both the Y and $\overline{\mathrm{Y}}$ outputs are taken to the high-impedance state.

## OUTPUTS

Y, Y (Pins 5, 6)
Data outputs. The selected data is presented at these pins in both true (Y output) and complemented ( $\overline{\mathrm{Y}}$ output) forms.

## MC74HC251A

## SWITCHING WAVEFORMS



Figure 2.


Figure 4.


Figure 3.


Figure 5.

## TEST CIRCUITS


*Includes all probe and jig capacitance
Figure 6.

*Includes all probe and jig capacitance

Figure 7.


Figure 8. Expanded Logic Diagram

ORDERING INFORMATION

| Device | Package | Shipping ${ }^{\text {² }}$ |
| :---: | :---: | :---: |
| MC74HC251ADG | SOIC-16 <br> (Pb-Free) | 48 Units / Rail |
| MC74HC251ADR2G |  | 2500 Tape \& Reel |
| NLV74HC251ADR2G* |  | 2500 Tape \& Reel |
| MC74HC251ADTG | $\begin{aligned} & \text { TSSOP-16 } \\ & \text { (Pb-Free) } \end{aligned}$ | 96 Units / Rail |
| MC74HC251ADTR2G |  | 2500 Tape \& Reel |

$\dagger$ For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

SOIC-16
CASE 751B-05
ISSUE K
SCALE 1:1


STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. EMITT
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 5:
PIN 1. DRAIN, DYE \#1
2. DRAIN, \#1
3. DRAIN, \#2
4. DRAIN, \#2
4. DRAIN, \#2
5. DRAIN, \#3
6. DRAIN, \#3 6. CATHODE
7. DRAIN, \#4 7. CATHODE
8. DRAIN, \#4
9. GATE, \#4
10. SOURCE, \#4
11. GATE, \#3
12. SOURCE, \#3
12. SOURCE, \#3
13. GATE, \#2
14. SOURCE, \#2
15. GATE, \#1
16. SOURCE, \#1

| STYLE 2: |  |
| ---: | :--- |
| PIN 1. | CATHODE |
| 2. | ANODE |
| 3. | NO CONNECTION |
| 4. | CATHODE |
| 5. | CATHODE |
| 6. | NO CONNECTION |
| 7. | ANODE |
| 8. | CATHODE |
| 9. | CATHODE |
| 10. | ANODE |
| 11. | NO CONNECTION |
| 12. | CATHODE |
| 13. | CATHODE |
| 14. | NO CONNECTION |
| 15. | ANODE |
| 16. | CATHODE |

PIN 1. CATHODE

STYLE 3:
PIN 1. COLLECTOR DYE
2. BASE,\#1
3. EMITTER, \#1
4. COLLECTOR \#1

STYLE 4:
PIN 1. COLLECTOR, DYE \#1
2. COLLECTOR,\#1
3. COLLECTOR, \#2 4. COLLECTOR, \#2 4. COLLECTOR, \#2 5. COLLECTOR, \#3 6. COLLECTOR, \#3 7. COLLECTOR, \#4 9. BASE, \#4
10. EMITTER, \#4
11. BASE, \#3
11. BASE, \#3
12. EMITTER, \#3
12. EMITTER, \#
13. BASE, \#2
14. EMITTER, \#2 R RECOMMENDED
15. BASE, \#1
16. EMITTER, \#1 8X

STYLE 6: STYLE 7:
PIN 1.
IN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
12. COMMON DR
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH


DIMENSIONS: MILLIMETERS
*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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| ---: | :--- | :--- | :--- |
| DESCRIPTION: | SOIC-16 | PAGE 1 OF 1 |  |

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TSSOP-16 WB
CASE 948F
ISSUE B
DATE 19 OCT 2006


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 ( 0.006 ) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 ( 0.010 ) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL in EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE - $W$ -

| DIM | MILLIMETERS |  | INCHES |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| c |  | 1.20 |  | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 | SC | 0.026 | BSC |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 | BC | 0.25 | BSC |
| M | $0^{\circ}$ | $8^{\circ}$ | $0^{\circ}$ | $8^{\circ}$ |



| GENERIC <br> MARKING DIAGRAM* |  |
| :---: | :---: |
|  |  |
| XXXX | = Specific Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| G or - | = Pb-Free Package |

*This information is generic. Please refer to device data sheet for actual part marking. $\mathrm{Pb}-$ Free indicator, " G " or microdot " $\mathrm{\bullet}$ ", may or may not be present. Some products may not follow the Generic Marking.
*For additional information on our $\mathrm{Pb}-$ Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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| DESCRIPTION: | TSSOP-16 | PAGE 1 OF 1 |

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