## Quad 2-Input NAND Gate <br> High-Performance Silicon-Gate CMOS <br> MC74HC00A

The MC74HC00A is identical in pinout to the LS00. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

## Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: $1 \mu \mathrm{~A}$
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 32 FETs or 8 Equivalent Gates
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are $\mathrm{Pb}-$ Free, Halogen Free and are RoHS Compliant


Figure 1. Logic Diagram


Figure 2. Pinout (Top View)

$\qquad$

## FUNCTION TABLE

| Inputs |  | Output |
| :---: | :---: | :---: |
| A | B | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

## ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

MAXIMUM RATINGS

| Symbol | Parameter |  | Value | Unit |
| :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | DC Supply Voltage |  | -0.5 to +6.5 | V |
| $V_{1}$ | DC Input Voltage |  | -0.5 to $\mathrm{V}_{\mathrm{CC}}+0.5$ | V |
| $\mathrm{V}_{\mathrm{O}}$ | DC Output Voltage |  | -0.5 to $\mathrm{V}_{\mathrm{CC}}+0.5$ | V |
| $\mathrm{I}_{\mathrm{IN}}$ | DC Input Current, per Pin |  | $\pm 20$ | mA |
| IOUT | DC Output Current, Per Pin |  | $\pm 25$ | mA |
| $I_{\text {CC }}$ | DC Supply Current, $\mathrm{V}_{\mathrm{CC}}$ and GND Pins |  | $\pm 50$ | mA |
| $\mathrm{IIK}^{\text {I }}$ | Input Clamp Current ( $\mathrm{V}_{\text {IN }}<0$ or $\mathrm{V}_{\text {IN }}>\mathrm{V}_{\mathrm{CC}}$ ) |  | $\pm 20$ | mA |
| IOK | Output Clamp Current ( $\mathrm{V}_{\text {OUT }}<0$ or $\mathrm{V}_{\text {OUT }}>\mathrm{V}_{\mathrm{CC}}$ ) |  | $\pm 20$ | mA |
| $\mathrm{T}_{\text {STG }}$ | Storage Temperature Range |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\mathrm{L}}$ | Lead Temperature, 1 mm from Case for 10 secs |  | 260 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{J}$ | Junction Temperature Under Bias |  | +150 | ${ }^{\circ} \mathrm{C}$ |
| $\theta_{\text {JA }}$ | Thermal Resistance (Note 1) | $\begin{array}{r} \text { SOIC-14 } \\ \text { QFN14 } \\ \text { TSSOP-14 } \end{array}$ | $\begin{aligned} & 116 \\ & 130 \\ & 150 \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $P_{D}$ | Power Dissipation in Still Air at $25^{\circ} \mathrm{C}$ | $\begin{array}{r} \text { SOIC-14 } \\ \text { QFN14 } \\ \text { TSSOP-20 } \end{array}$ | $\begin{gathered} 1077 \\ 962 \\ 833 \end{gathered}$ | mW |
| MSL | Moisture Sensitivity |  | Level 1 | - |
| $\mathrm{F}_{\mathrm{R}}$ | Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V -0 @ 0.125 in | - |
| $\mathrm{V}_{\text {ESD }}$ | ESD Withstand Voltage (Note 2) | Human Body Model Charged Device Model | $\begin{gathered} >2000 \\ N / A \end{gathered}$ | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm -by- $114 \mathrm{~mm}, 2$-ounce copper trace no air flow per JESD51-7.
2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
| :---: | :--- | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| $\mathrm{~V}_{\text {IN }}$, | DC Input, Output Voltage (Referenced to GND) (Note 3) | 0 | $V_{C C}$ | V |
| $\mathrm{~V}_{\mathrm{OUT}}$ |  |  | -55 | +125 |
| $\mathrm{~T}_{\mathrm{A}}$ | Operating Free-Air Temperature | $\mathrm{V}_{\mathrm{CC}}=2.0 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{CC}}=4.5 \mathrm{~V}$ | -0 |
| $\mathrm{t}_{\mathrm{r}}, \mathrm{t}_{\mathrm{f}}$ | Input Rise or Fall Rate | $\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}$ | 0 | 1000 |
|  |  | 0 | 500 | ns |
|  |  |  |  |  |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $\mathrm{V}_{\mathrm{Cc}}$ ). Unused outputs must be left open.

## MC74HC00A

DC CHARACTERISTICS

| Symbol | Parameter | Condition | $\underset{\mathbf{v c}}{\mathrm{v}_{\mathrm{cc}}}$ | Guaranteed Limit |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | -55 to $25^{\circ} \mathrm{C}$ | $\leq 85{ }^{\circ} \mathrm{C}$ | $\leq 125^{\circ} \mathrm{C}$ |  |
| $\mathrm{V}_{\mathrm{IH}}$ | Minimum High-Level Input Voltage | $\begin{aligned} & \mathrm{V}_{\text {out }}=0.1 \mathrm{~V} \text { or } \mathrm{V}_{\mathrm{CC}}-0.1 \mathrm{~V} \\ & \left\|\left.\right\|_{\text {out }} \leq 20 \mu \mathrm{~A}\right. \end{aligned}$ | $\begin{aligned} & \hline 2.0 \\ & 3.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 1.50 \\ & 2.10 \\ & 3.15 \\ & 4.20 \end{aligned}$ | $\begin{aligned} & 1.50 \\ & 2.10 \\ & 3.15 \\ & 4.20 \end{aligned}$ | $\begin{aligned} & 1.50 \\ & 2.10 \\ & 3.15 \\ & 4.20 \end{aligned}$ | V |
| $\mathrm{V}_{\text {IL }}$ | Maximum Low-Level Input Voltage | $\begin{aligned} & \begin{array}{l} \mathrm{V}_{\text {out }}=0.1 \mathrm{~V} \text { or } \mathrm{V}_{\mathrm{CC}}-0.1 \mathrm{~V} \\ \mid l_{\text {out }} \end{array} \leq 20 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & \hline 2.0 \\ & 3.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & \hline 0.50 \\ & 0.90 \\ & 1.35 \\ & 1.80 \end{aligned}$ | $\begin{aligned} & \hline 0.50 \\ & 0.90 \\ & 1.35 \\ & 1.80 \end{aligned}$ | $\begin{aligned} & \hline 0.50 \\ & 0.90 \\ & 1.35 \\ & 1.80 \end{aligned}$ | V |
| $\mathrm{V}_{\mathrm{OH}}$ | Minimum High-Level Output Voltage | $\begin{aligned} & V_{\text {in }}=V_{I H} \text { or } V_{I L} \\ & \left\|l_{\text {lout }}\right\| \leq 20 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & \hline 2.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 4.4 \\ & 5.9 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 4.4 \\ & 5.9 \end{aligned}$ | 1.9 4.4 5.9 | V |
|  |  |  | $\begin{aligned} & \hline 3.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 2.48 \\ & 3.98 \\ & 5.48 \end{aligned}$ | $\begin{aligned} & 2.34 \\ & 3.84 \\ & 5.34 \end{aligned}$ | $\begin{aligned} & 2.20 \\ & 3.70 \\ & 5.20 \end{aligned}$ |  |
| $\mathrm{V}_{\text {OL }}$ | Maximum Low-Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\text {in }}=\mathrm{V}_{\mathrm{IH}} \text { or } \mathrm{V}_{\mathrm{IL}} \\ & \left\|l_{\text {out }}\right\| 20 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & \hline 2.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & \hline 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & \hline 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & \hline 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | V |
|  |  |  | $\begin{aligned} & \hline 3.0 \\ & 4.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 0.26 \\ & 0.26 \\ & 0.26 \end{aligned}$ | $\begin{aligned} & 0.33 \\ & 0.33 \\ & 0.33 \end{aligned}$ | $\begin{aligned} & 0.40 \\ & 0.40 \\ & 0.40 \end{aligned}$ |  |
| $\mathrm{l}_{\text {in }}$ | Maximum Input Leakage Current | $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {cc }}$ or GND | 6.0 | $\pm 0.1$ | $\pm 1.0$ | $\pm 1.0$ | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{CC}}$ | Maximum Quiescent Supply Current (per Package) | $\begin{aligned} & \mathrm{V}_{\text {in }}=\mathrm{V}_{\mathrm{CC}} \text { or GND } \\ & \mathrm{I}_{\text {out }}=0 \mu \mathrm{~A} \end{aligned}$ | 6.0 | 1.0 | 10 | 40 | $\mu \mathrm{A}$ |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## AC CHARACTERISTICS

| Symbol | Parameter | $\underset{\mathbf{V C}}{\mathbf{v}_{\mathrm{cc}}}$ | Guaranteed Limit |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | -55 to $25^{\circ} \mathrm{C}$ | $\leq 85^{\circ} \mathrm{C}$ | $\leq 125^{\circ} \mathrm{C}$ |  |
| $\begin{aligned} & \mathrm{t}_{\mathrm{PLH}}, \\ & \mathrm{t}_{\mathrm{PH}}, \end{aligned}$ | Maximum Propagation Delay, (A or B) to Y (Figures 3 and 4) | 2.0 | 75 | 95 | 110 | ns |
|  |  | 3.0 | 30 | 40 | 55 |  |
|  |  | 4.5 | 15 | 19 | 22 |  |
|  |  | 6.0 | 13 | 16 | 19 |  |
| $\begin{aligned} & \mathrm{t}_{\mathrm{T} \mathrm{LH}}, \\ & \mathrm{t}_{\mathrm{TH}} \end{aligned}$ | Maximum Output Transition Time, Any Output (Figures 3 and 4) | 2.0 | 75 | 95 | 110 | ns |
|  |  | 3.0 | 27 | 32 | 36 |  |
|  |  | 4.5 | 15 | 19 | 22 |  |
|  |  | 6.0 | 13 | 16 | 19 |  |
| $\mathrm{C}_{\text {in }}$ | Maximum Input Capacitance |  | 10 | 10 | 10 | pF |


| CPD | Power Dissipation Capacitance (Per Buffer)* | Typical @ 25 ${ }^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}$ | pF |
| :---: | :---: | :---: | :---: |
|  |  | 22 |  |

[^0]
## MC74HC00A


${ }^{*} \mathrm{C}_{\mathrm{L}}$ Includes probe and jig capacitance

| Test | Switch Position | $\mathbf{C}_{\mathbf{L}}$ | $\mathbf{R}_{\mathbf{L}}$ |
| :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\mathrm{PLL}} / \mathrm{t}_{\text {PHL }}$ | Open | 50 pF | $1 \mathrm{k} \Omega$ |
| $\mathrm{t}_{\text {PLZ }} / \mathrm{t}_{\text {PZL }}$ | $\mathrm{V}_{\mathrm{CC}}$ |  |  |
| $\mathrm{t}_{\mathrm{PHZ}} / \mathrm{t}_{\text {PZH }}$ | GND |  |  |

Figure 3. Test Circuit


| Device | $\mathbf{V}_{\mathbf{I N}}, \mathbf{V}$ | $\mathbf{V}_{\mathbf{m}}, \mathbf{V}$ |
| :---: | :---: | :---: |
| MC74HC00A | $\mathrm{V}_{\mathrm{CC}}$ | $50 \% \times \mathrm{V}_{\mathrm{CC}}$ |

Figure 4. Switching Waveforms


Figure 5. Expanded Logic Diagram (1/4 of the Device)

## MC74HC00A

ORDERING INFORMATION

| Device | Package | Marking | Shipping $^{\dagger}$ |
| :--- | :---: | :---: | :---: |
| MC74HC00ADG | SOIC-14 | HC00A | 55 Units / Rail |
| MC74HC00ADR2G | SOIC-14 | HC00A | $2500 /$ Tape \& Reel |
| MC74HC00ADTR2G | TSSOP-14 | HC <br> $00 A$ | $2500 /$ Tape \& Reel |
| MC74HC00ADR2G-Q* $^{\text {MC74HC00ADTR2G-Q* }}$ | SOIC-14 | HC00A | $2500 /$ Tape \& Reel |

$\dagger$ For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable


SOIC-14 NB
CASE 751A-03
ISSUE L
SCALE 1:1


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR

PROTRUSION. ALLOWABLE PROTRUSION
SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION
4. DIMENSIONS D AND E DO NOT INCLUDE

MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS |  |  | INCHES |  |
| :---: | ---: | :---: | ---: | ---: | :---: |
|  | MIN | MAX | MIN | MAX |  |
|  | 1.35 | 1.75 | 0.054 | 0.068 |  |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |  |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |  |
| b | 0.35 | 0.49 | 0.014 | 0.019 |  |
| D | 8.55 | 8.75 | 0.337 | 0.344 |  |
| E | 3.80 | 4.00 | 0.150 | 0.157 |  |
| e | 1.27 BSC | 0.050 | BSC |  |  |
| H | 5.80 | 6.20 | 0.228 | 0.244 |  |
| h | 0.25 | 0.50 | 0.010 | 0.019 |  |
| L | 0.40 | 1.25 | 0.016 | 0.049 |  |
| M | 0 | $7^{\circ}$ | $7^{\circ}$ | $0^{\circ}$ |  |



SOLDERING FOOTPRINT*


For additional information on our $\mathrm{Pb}-$ Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## STYLES ON PAGE 2

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STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
4. COMMON ANODE

STYLE 5
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHOD
4. ANODE/CATHOD
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHOD
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2 :
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION 2. ANODE 3. ANODE
4. NO CONNECTION 5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

## STYLE 6

PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
5. CATHODE
6. CATHODE
7. CATHOD
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
11. COMMON CATHOD
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 4:
PIN 1. NO CONNECTION 2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
11. NO CONNECTION
12. ANODE/CATHODE
12. ANODE/CATHODE
13. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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TSSOP-14 WB
CASE 948G
ISSUE C
DATE 17 FEB 2016


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS MOLD FLASH OR GATE BURRS SHALL NOT MOLD FLASH OR GATE BURRS
EXCEED $0.15(0.006)$ PER SIDE.
4. DIMENSION B DOES NOT INCLUDE

INTERLEAD FLASH OR PROTRUSION.
INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |  | INCHES |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 | BSC | 0.026 |  |
| BSC |  |  |  |  |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | 0.252 | BSC |  |
| M | $00^{\circ}$ | $8^{\circ}$ | $0^{\circ}$ | $8^{\circ}$ |

GENERIC MARKING DIAGRAM*

SOLDERING FOOTPRINT


|  |
| :---: |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |


| A | $=$ Assembly Location |
| :--- | :--- |
| L | $=$ Wafer Lot |
| Y | $=$ Year |
| W | $=$ Work Week |
| - | $=$ Pb-Free Package |

(Note: Microdot may be in either location)
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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[^0]:    *Used to determine the no-load dynamic power consumption: $P_{D}=C_{P D} V_{C C}{ }^{2 f}+I_{C C} V_{C C}$.

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