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MC33566

Smart Voltage Regulator for Peripheral Card Applications

The MC33566 Low Dropout Regulator is designed for computer peripheral card applications complying with the *instantly available requirements* as specified by ACPI objectives. The MC33566 permits glitch-free transitions from “sleep” to “active” system modes and has internal logic circuitry to detect whether the system is being powered from the motherboard main 5.0 V power supply or the 3.3 V aux supply.

The MC33566 provides a regulated output voltage of 3.3 V via either an internal low dropout 5.0 V-to-3.3 V voltage regulator or an external P-channel MOSFET, depending on the operating status of the system in which the card is installed. During normal operating mode (5.0 V main supply available) the 3.3 V output is provided from the internal low dropout regulator at an output current of 0.4 A. When the motherboard enters sleep mode, the MC33566 operates from the 3.3 V aux supply and routes the aux current to the output via the external P-channel MOSFET bypass transistor controlled by the *drive out* pin. As a result, the output voltage provided to the peripheral card remains constant at 3.3 V even during host systems transitions to and from sleep mode.

MC33566 Features:

- Output Current up to 0.4 A
- Excellent Line and Load Regulation
- Low Dropout Voltage
- Prevents Reverse Current Flow During Sleep Mode
- Glitch-Free Transfer from Sleep Mode to Active Mode
- Compatible with *Instantly Available* PC Systems

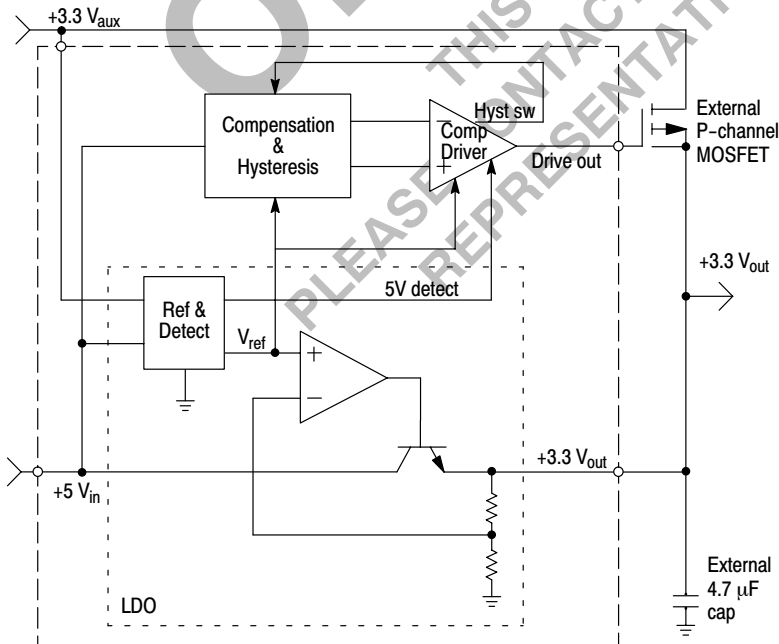


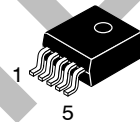
Figure 1. Simplified Block Diagram



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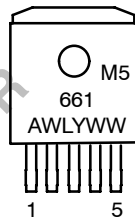
MARKING DIAGRAM



Pin

D²PAK
D2T SUFFIX
CASE 936A

1. V_{aux}
2. V_{in}
3. Gnd
4. V_{out}
5. Drv



Note: Tab is ground

- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week

ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------|--------------------|-----------------|
| MC33566D2T-1 | D ² PAK | 50 Units/Rail |
| MC33566D2T-1RK | D ² PAK | 800 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PIN ASSIGNMENTS AND FUNCTIONS

| Pin # | Pin Name | Pin Description |
|-------|-----------------------|---|
| 1 | +3.3 V _{aux} | Auxiliary input. Typical voltage 3.3 V. |
| 2 | +5.0 V _{in} | This is the input supply for the IC. Typical voltage 5.0 V. (Notes 1 and 2) |
| 3 | Gnd | Logic and power ground. |
| 4 | +3.3 V _{out} | 3.3 V output provided to the application circuit (output current is sourced to this pin from the 5.0 V input.) |
| 5 | Drive out | This output drives a P-channel MOSFET with up to 2000 pF of "effective" gate capacitance. Recommended devices are the MMFT5P03HD and MTSF1P02HD. Drive out has active internal pull-up and pull-down circuitry to guarantee fast transitions. |

MAXIMUM RATINGS (T_C = 25°C, unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|---------------------------|---------------|------|
| +5.0 V _{in} Supply Voltage | V _{in} | 7.0 | Vdc |
| | V _{in} | -0.5 (Note 3) | Vdc |
| Operating Ambient Temperature | T _a | -5.0 to +85 | °C |
| Operating Junction Temperature | T _J | - 5.0 to +150 | °C |
| Lead Temperature (Soldering, 10 seconds) | T _L | 300 | °C |
| Storage Temperature | T _{stg} | - 55 to +150 | °C |
| Package Thermal Resistance | R _{θJA} (Note 4) | 65 | °C/W |

AC ELECTRICAL SPECIFICATIONS (Notes 5, 6, and 7)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|-----------------|-----|-----|-----|------|
| Drive High Delay (V _{in} ramping up) C _{drive} = 1.2 nF, measured from +5.0 V _{in} = V _{thresHi} to V _{Drive} = 2.0 V | t _{DH} | - | 0.5 | 3.5 | μS |
| Drive Low Delay (V _{in} ramping down) C _{drive} = 1.2 nF, measured from +5.0 V _{in} = V _{thresLo} to V _{Drive} = 2.0 V | t _{DL} | - | 0.5 | 3.5 | μS |

1. See 5.0 V Detect Thresholds Diagram.
2. Recommended source impedance for 5.0 V supply: ≤ 0.12 Ω. This will ensure that I_o × R_{source} < V_{hyst}, thus avoiding driveout toggling during 5.0 V detect threshold transitions.
3. V_{in} should not be allowed to go negative relative to ground.
4. Mounted on recommended minimum PCB pad on FR4, 2-oz. copper circuit board.
5. AC specs are guaranteed by characterization, but not production tested after characterization.
6. See Figure 3. Application Block Diagram.
7. See Timing Diagram.

MC33566

DC ELECTRICAL CHARACTERISTICS (Note 8)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|----------------------|------|-----|-----|------|
| +5.0 V _{in} Supply Voltage Range | +5.0 V _{in} | 4.35 | 5.0 | 5.5 | Vdc |
| Reverse Leakage Current from Output | I _{reverse} | – | – | 25 | μA |
| V _{aux} Quiescent Current | I _{qaux} | – | – | 2.0 | mA |
| +5.0 V _{in} Quiescent Current, Operating | I _{qvin} | – | – | 10 | mA |
| Load Capacitance (Note 9) | C _{load} | 4.7 | 22 | – | μF |

REGULATOR OUTPUT

| | | | | | |
|--|-----------------------|----------------|--------------|----------------|-----|
| Output Voltage (4.35 V ≤ V _{in} ≤ 5.5 V, 0 mA ≤ I _o ≤ 400 mA) T _A = 25°C (T _J = –5°C to 150°C) | +3.3 V _{out} | 3.267 3.234 | 3.30 3.30 | 3.333 3.366 | Vdc |
| In-to-Out Voltage (3.9 V ≤ V _{in} ≤ 4.35 V, V _{aux} = 3.3 V) | V _d | 3.0 | – | – | Vdc |
| Voltage Out at Max Voltage In (V _{in} = 7.0 V) | V _{outmax} | 3.1 | 3.3 | 3.5 | Vdc |
| Line Regulation (I _o = 400 mA) | Linereg | – | – | 0.4 | % |
| Load Regulation (I _o = 0 to 400 mA) | Loadreg | – | – | 0.8 | % |

5.0 V DETECT

| | | | | | |
|--|----------------------|------|------|------|-----|
| Low Threshold Voltage (+5.0 V _{in} Falling, I _o = 400 mA) | V _{thresLo} | 3.9 | 4.05 | – | Vdc |
| High Threshold Voltage (+5.0 V _{in} Rising, I _o = 400 mA) | V _{thresHi} | – | 4.2 | 4.35 | Vdc |
| Hysteresis | V _{hyst} | 0.05 | – | – | Vdc |

DRIVE OUTPUT

| | | | | | |
|---|-------------------|-----|-----|-----|------|
| Output Peak Source Current (+5.0 V _{in} > V _{thresHi}) | I _{peak} | 15 | – | – | mA |
| Output Peak Sink Current (+5.0 V _{in} < V _{thresLo}) | I _{peak} | 15 | – | – | mA |
| Low Output Voltage (I _{oL} = 200 μA, V _{in} < V _{thresLo}) | V _{oL} | – | 100 | 200 | mVdc |
| High Output Voltage (I _{oH} = 200 μA) | V _{oH} | 3.4 | – | – | Vdc |

8. –5°C < T_a < 70°C, 4.35 V < V_{in} < 5.5 V, C_{load} ≥ 4.7 μF unless otherwise noted.

9. 4.7 μF minimum over temperature; 22 μF recommended; 500 mΩ ESR maximum.

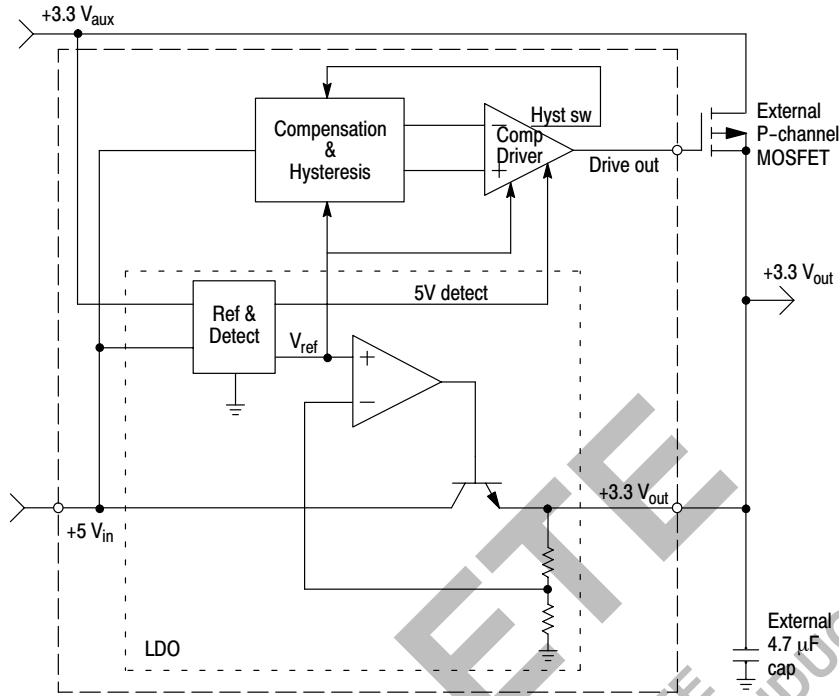


Figure 2. Functional Block Diagram

FUNCTIONAL DESCRIPTION

Input Blocking – The internal NPN pass transistor of the LDO regulator ensures that no significant reverse current will flow from +3.3 V_{out} back to the +5.0 V_{in} input when the 5.0 V input is not powered and the 3.3 V_{in} supply is present.

5.0 Volt Detect – Internal circuitry detects the presence of the 5.0 V input supply. When the 5.0 V supply drops below a given threshold, the +3.3 V_{in} bypass transistor (an external P-channel MOSFET) is enabled. The 5.0 V detect logic is active throughout the entire range of ramp-up from 0 to 5.5 V. Additionally, the drive out signal is never turned ON or OFF inappropriately during ramp-up of the +5.0 V_{in} supply. Also, +3.3 V_{out} never drops below 3.0 V while +5.0 V_{in} is above the 5.0 V detect minimum threshold.

Glitch-free Transfer – The design of the 5.0 V detect circuitry and drive out control circuitry guarantees that the +3.3 V_{out} will not exceed the output voltage specification listed in the table of DC Operating Specifications even with +5.0 V_{in} ramping up and down at the extremes of the slew rates in the table of AC Operating Specifications.

Offset Voltage Performance – To ensure performance when external offsets are present on the +5.0 V_{in} and +3.3 V_{in} power inputs, the device has been designed to be capable of operating with either one or both of these inputs rising from or falling to zero volts, or with offsets of 0.05 V to 0.9 V as the inputs ramp up and down.

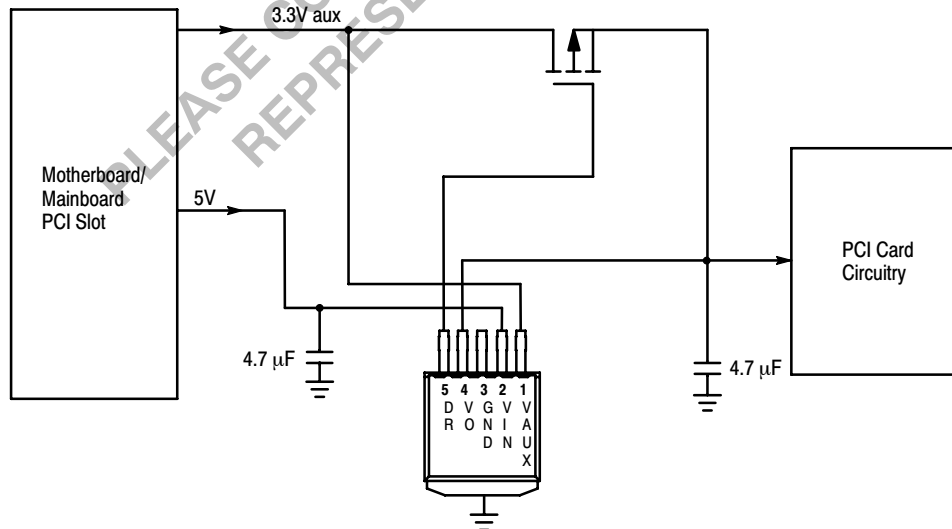
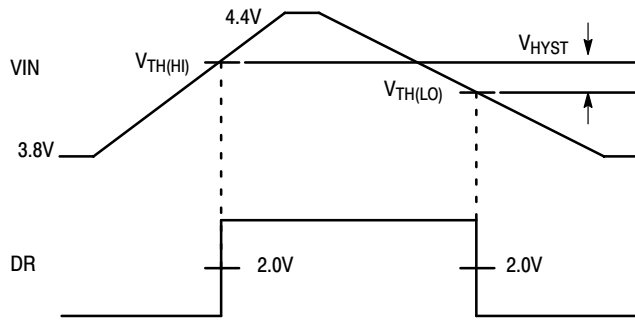


Figure 3. Application Block Diagram

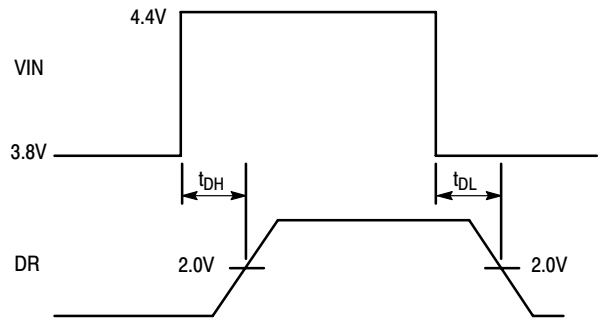
MC33566



NOTE:

(1) V_{in} rise and fall times (10% to 90%) to be $\geq 100 \mu s$.

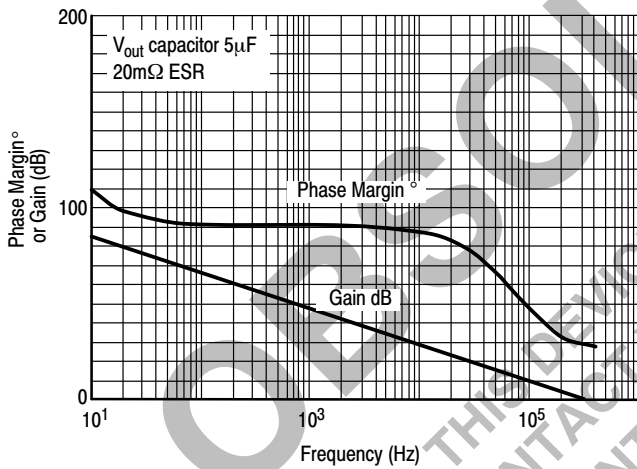
Figure 4. 5.0 V Detect Thresholds Diagram



NOTE:

(1) V_{in} rise and fall times (10% to 90%) to be $\leq 100 ns$.

Figure 5. Timing Diagram



NOTE: V_{out} capacitor $\geq 4.7 \mu F$ over operating temperature range.
Maximum ESR permissible = 500 m Ω over operating temperature range.

Figure 6. Predicted Gain and Phase at Zero Load Current

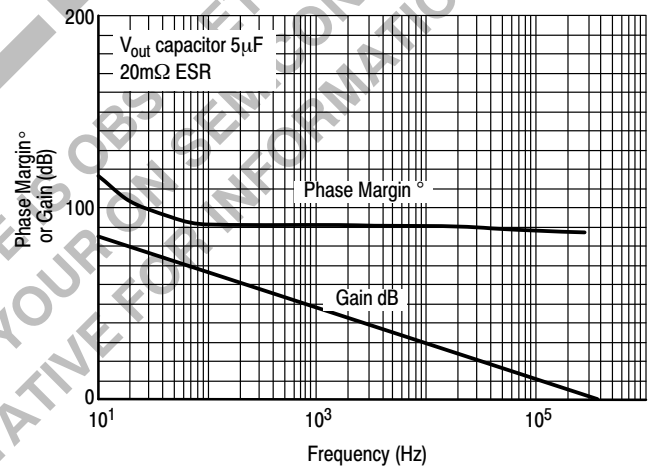
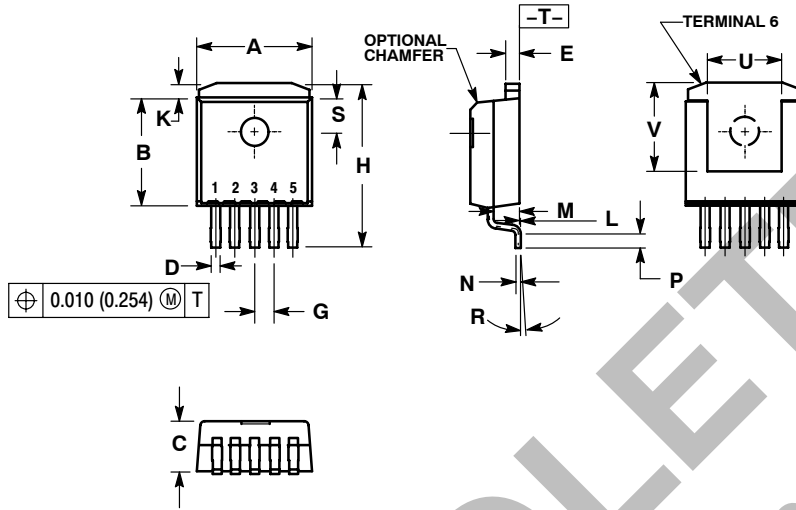


Figure 7. Predicted Gain and Phase at Full Load Current

MC33566

PACKAGE DIMENSIONS

(D²PAK)
D2T SUFFIX
PLASTIC PACKAGE
CASE 936A-02
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|--------|
| | MIN | MAX | MIN | MAX |
| A | 0.386 | 0.403 | 9.804 | 10.236 |
| B | 0.356 | 0.368 | 9.042 | 9.347 |
| C | 0.170 | 0.180 | 4.318 | 4.572 |
| D | 0.026 | 0.036 | 0.660 | 0.914 |
| E | 0.045 | 0.055 | 1.143 | 1.397 |
| G | 0.067 BSC | | 1.702 BSC | |
| H | 0.539 | 0.579 | 13.691 | 14.707 |
| K | 0.050 REF | | 1.270 REF | |
| L | 0.000 | 0.010 | 0.000 | 0.254 |
| M | 0.088 | 0.102 | 2.235 | 2.591 |
| N | 0.018 | 0.026 | 0.457 | 0.660 |
| P | 0.058 | 0.078 | 1.473 | 1.981 |
| R | 5° REF | | 5° REF | |
| S | 0.116 REF | | 2.946 REF | |
| U | 0.200 MIN | | 5.080 MIN | |
| V | 0.250 MIN | | 6.350 MIN | |

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