

# ON Semiconductor

## Is Now

# onsemi™

To learn more about onsemi™, please visit our website at  
[www.onsemi.com](http://www.onsemi.com)

---

**onsemi** and **onsemi** and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.

# MC3346

## General Purpose Transistor Array One Differentially Connected Pair and Three Isolated Transistor Arrays

The MC3346 is designed for general purpose, low power applications for consumer and industrial designs.

- Guaranteed Base–Emitter Voltage Matching
- Operating Current Range Specified: 10  $\mu$ A to 10 mA
- Five General Purpose Transistors in One Package



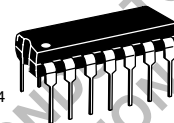
ON Semiconductor®

<http://onsemi.com>

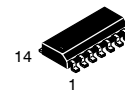
### GENERAL PURPOSE TRANSISTOR ARRAY SEMICONDUCTOR TECHNICAL DATA

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	15	Vdc
Collector–Base Voltage	$V_{CBO}$	20	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0	Vdc
Collector–Substrate Voltage	$V_{CISO}$	20	Vdc
Collector Current – Continuous	$I_C$	50	mAdc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.2 10	W mW/ $^\circ\text{C}$
Operating Temperature Range	$T_A$	-40 to +85	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$

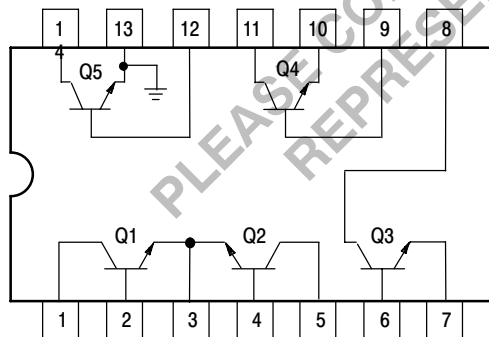


**P SUFFIX**  
PLASTIC PACKAGE  
CASE 646



**D SUFFIX**  
PLASTIC PACKAGE  
CASE 751A  
(SO-14)

#### PIN CONNECTIONS



Pin 13 is connected to substrate and must remain at the lowest circuit potential.

#### ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3346D	$T_A = -40^\circ$ to $+85^\circ\text{C}$	SO-14
MC3356P		Plastic DIP

# MC3346

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
<b>STATIC CHARACTERISTICS</b>					
Collector–Base Breakdown Voltage (I <sub>C</sub> = 10 μAdc)	V <sub>(BR)CBO</sub>	20	60	–	Vdc
Collector–Emitter Breakdown Voltage (I <sub>C</sub> = 1.0 mAdc)	V <sub>(BR)CEO</sub>	15	–	–	Vdc
Collector–Substrate Breakdown Voltage (I <sub>C</sub> = 10 μA)	V <sub>(BR)CIO</sub>	20	60	–	Vdc
Emitter–Base Breakdown Voltage (I <sub>E</sub> = 10 μAdc)	V <sub>(BR)EBO</sub>	5.0	7.0	–	Vdc
Collector–Base Cutoff Current (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0)	I <sub>CBO</sub>	–	–	40	nAdc
DC Current Gain (I <sub>C</sub> = 10 mAdc, V <sub>CE</sub> = 3.0 Vdc) (I <sub>C</sub> = 1.0 mAdc, V <sub>CE</sub> = 3.0 Vdc) (I <sub>C</sub> = 10 μAdc, V <sub>CE</sub> = 3.0 Vdc)	h <sub>FE</sub>	– 40 –	140 130 60	– – –	–
Base–Emitter Voltage (V <sub>CE</sub> = 3.0 Vdc, I <sub>E</sub> = 1.0 mAdc) (V <sub>CE</sub> = 3.0 Vdc, I <sub>E</sub> = 10 mAdc)	V <sub>BE</sub>	– –	0.72 0.8	– –	Vdc
Input Offset Current for Matched Pair Q1 and Q2 (V <sub>CE</sub> = 3.0 Vdc, I <sub>C</sub> = 1.0 mAdc)	I <sub>IO1</sub> – I <sub>IO2</sub>	–	0.3	2.0	μAdc
Magnitude of Input Offset Voltage (V <sub>CE</sub> = 3.0 Vdc, I <sub>C</sub> = 1.0 mAdc)	–	–	0.5	5.0	mVdc
Temperature Coefficient of Base–Emitter Voltage (V <sub>CE</sub> = 3.0 Vdc, I <sub>C</sub> = 1.0 mAdc)	$\frac{\Delta V_{BE}}{D_T}$	–	–1.9	–	mV/°C
Temperature Coefficient	$\frac{ \Delta V_{IO} }{D_T}$	–	1.0	–	μV/°C
Collector–Emitter Cutoff Current (V <sub>CE</sub> = 10 Vdc, I <sub>B</sub> = 0)	I <sub>CEO</sub>	–	–	0.5	μAdc
<b>DYNAMIC CHARACTERISTICS</b>					
Low Frequency Noise Figure (V <sub>CE</sub> = 3.0 Vdc, I <sub>C</sub> = 100 μAdc, R <sub>S</sub> = 1.0 kΩ, f = 1.0 kHz)	NF	–	3.25	–	dB
Forward Current Transfer Ratio (V <sub>CE</sub> = 3.0 Vdc, I <sub>C</sub> = 1.0 mAdc, f = 1.0 kHz)	h <sub>FE</sub>	–	110	–	–
Short Circuit Input Impedance (V <sub>CE</sub> = 3.0 Vdc, I <sub>C</sub> = 1.0 mAdc)	h <sub>ie</sub>	–	3.5	–	kΩ
Open Circuit Output Impedance (V <sub>CE</sub> = 3.0 Vdc, I <sub>C</sub> = 1.0 mAdc)	h <sub>oe</sub>	–	15.6	–	μmhos
Reverse Voltage Transfer Ratio (V <sub>CE</sub> = 3.0 Vdc, I <sub>C</sub> = 1.0 mAdc)	h <sub>re</sub>	–	1.8	–	x10 <sup>–4</sup>
Forward Transfer Admittance (V <sub>CE</sub> = 3.0 Vdc, I <sub>C</sub> = 1.0 mAdc, f = 1.0 MHz)	y <sub>fe</sub>	–	31–j1.5	–	–
Input Admittance (V <sub>CE</sub> = 3.0 Vdc, I <sub>C</sub> = 1.0 mAdc, f = 1.0 MHz)	y <sub>ie</sub>	–	0.3 + j0.04	–	–
Output Admittance (V <sub>CE</sub> = 3.0 Vdc, I <sub>C</sub> = 1.0 mAdc, f = 1.0 MHz)	y <sub>oe</sub>	–	0.001 + j0.03	–	–
Current–Gain – Bandwidth Product (V <sub>CE</sub> = 3.0 Vdc, I <sub>C</sub> = 3.0 mAdc)	f <sub>T</sub>	300	550	–	MHz
Emitter–Base Capacitance (V <sub>EB</sub> = 3.0 Vdc, I <sub>E</sub> = 0)	C <sub>eb</sub>	–	0.6	–	pF
Collector–Base Capacitance (V <sub>CB</sub> = 3.0 Vdc, I <sub>C</sub> = 0)	C <sub>cb</sub>	–	0.58	–	pF
Collector–Substrate Capacitance (V <sub>CS</sub> = 3.0 Vdc, I <sub>C</sub> = 0)	C <sub>Cl</sub>	–	2.8	–	pF

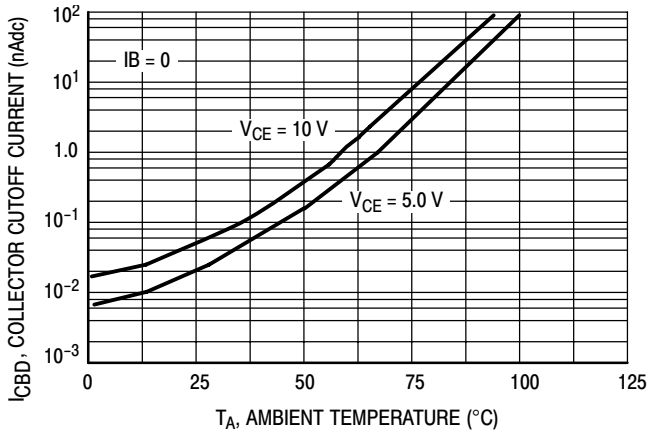


Figure 1. Collector Cutoff Current versus Temperature (Each Transistor)

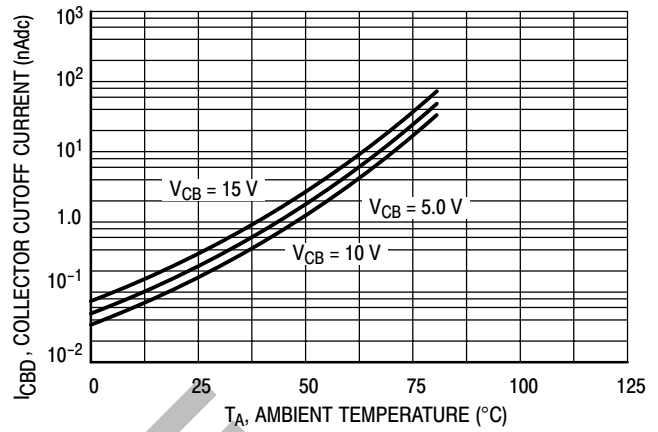


Figure 2. Collector Cutoff Current versus Temperature (Each Transistor)

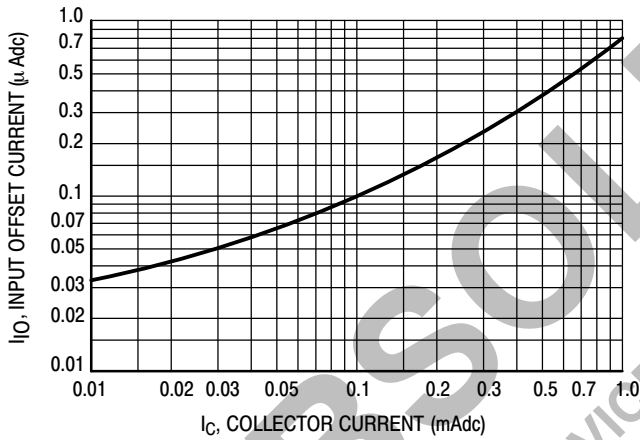


Figure 3. Input Offset Characteristics for Q1 and Q2

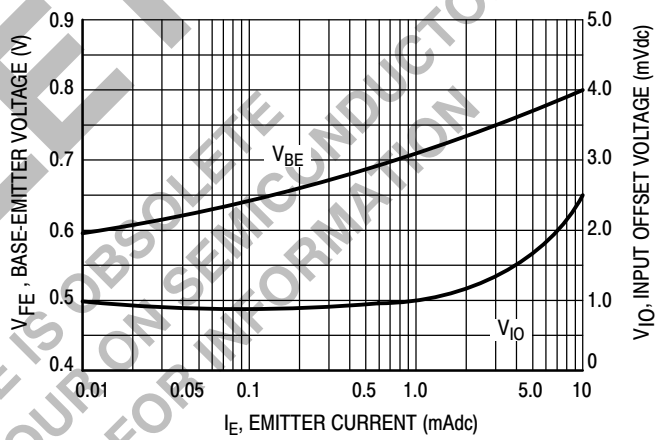


Figure 4. Base-Emitter and Input Offset Voltage Characteristics

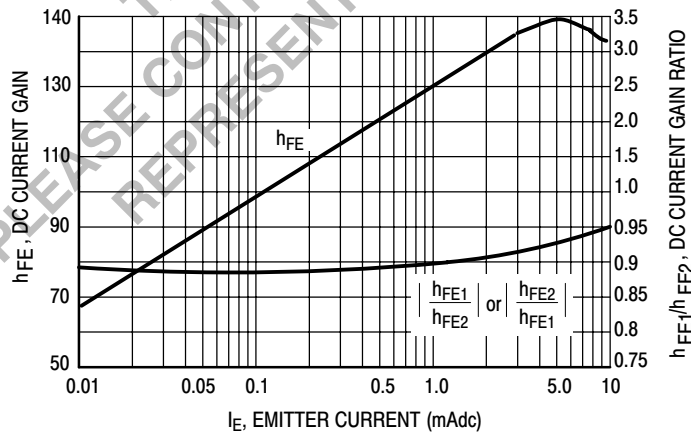
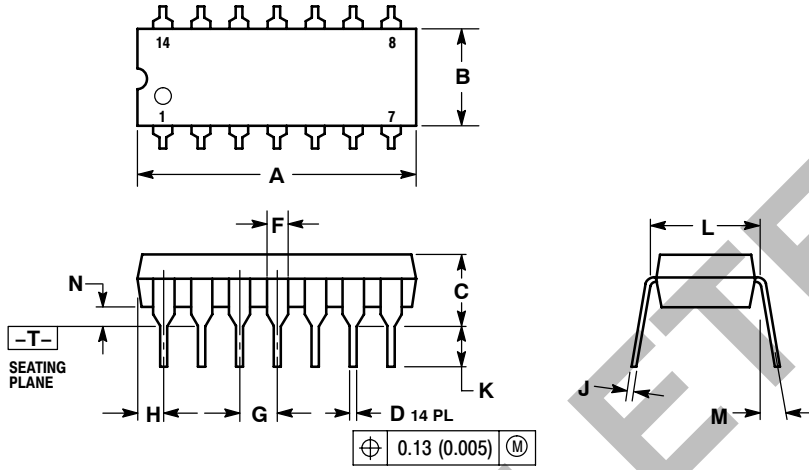


Figure 5. DC Current Gain

# MC3346

## PACKAGE DIMENSIONS

**P SUFFIX**  
**PLASTIC PACKAGE**  
**CASE 646-06**  
**ISSUE M**



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---		10°	
N	0.015	0.039	0.38	1.01

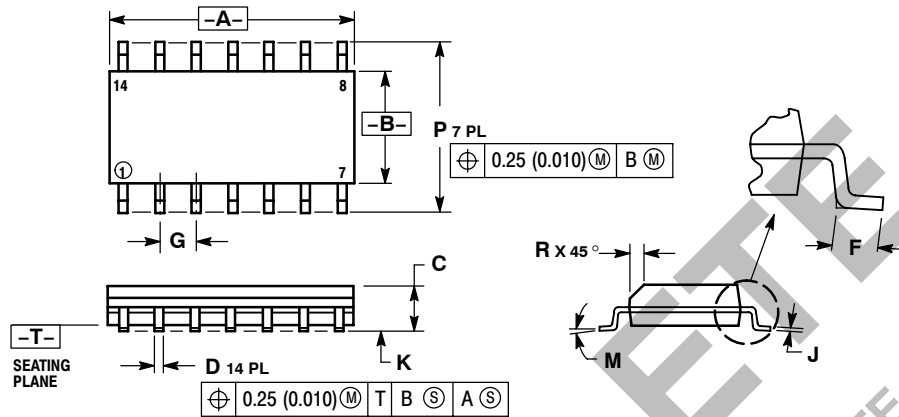
OBSOLETE

THIS DEVICE IS OBSOLETE  
 PLEASE CONTACT YOUR ON SEMICONDUCTOR  
 REPRESENTATIVE FOR INFORMATION

# MC3346

## PACKAGE DIMENSIONS

**D SUFFIX**  
**PLASTIC PACKAGE**  
 CASE 751A-03  
 (SO-8)  
 ISSUE F



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

**ON Semiconductor** and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

**PUBLICATION ORDERING INFORMATION**

**LITERATURE FULFILLMENT:**  
 Literature Distribution Center for ON Semiconductor  
 P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
 Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
 Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative