J111, J112

JFET Chopper Transistors

N-Channel — Depletion

Features

• Pb–Free Packages are Available*

MAXIMUM RATINGS

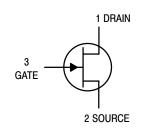
Rating	Symbol	Value	Unit
Drain-Gate Voltage	V _{DG}	-35	Vdc
Gate-Source Voltage	V _{GS}	-35	Vdc
Gate Current	I _G	50	mAdc
Total Device Dissipation @ $T_A = 25^{\circ}C$ Derate above = $25^{\circ}C$	P _D	350 2.8	mW mW/°C
Lead Temperature	TL	300	°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.



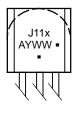
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MARKING DIAGRAM



J11x = Device Code x = 1 or 2 A = Assembly Location Y = Year WW = Work Week = = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

J111, J112

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS			•	•	•
Gate – Source Breakdown Voltage ($I_G = -1.0 \ \mu Adc$)		V _{(BR)GSS}	35	-	Vdc
Gate Reverse Current (V _{GS} = -15 Vdc)		I _{GSS}	-	-1.0	nAdc
Gate Source Cutoff Voltage (V _{DS} = 5.0 Vdc, I _D = 1.0 μAdc)	J111 J112	V _{GS(off)}	-3.0 -1.0	-10 -5.0	Vdc
Drain–Cutoff Current (V _{DS} = 5.0 Vdc, V _{GS} = -10 Vdc)		I _{D(off)}	-	1.0	nAdc
ON CHARACTERISTICS					
Zero-Gate-Voltage Drain Current ⁽¹⁾ (V _{DS} = 15 Vdc)	J111 J112	I _{DSS}	20 5.0 2.0	- - -	mAdc
Static Drain–Source On Resistance (V _{DS} = 0.1 Vdc)	J111 J112	r _{DS(on)}		30 50	Ω
Drain Gate and Source Gate On–Capacitance $(V_{DS} = V_{GS} = 0, f = 1.0 \text{ MHz})$		C _{dg(on)} + C _{sg(on)}	-	28	pF
Drain Gate Off–Capacitance (V _{GS} = -10 Vdc, f = 1.0 MHz)		C _{dg(off)}	-	5.0	pF
Source Gate Off–Capacitance (V _{GS} = -10 Vdc, f = 1.0 MHz)		C _{sg(off)}	-	5.0	pF

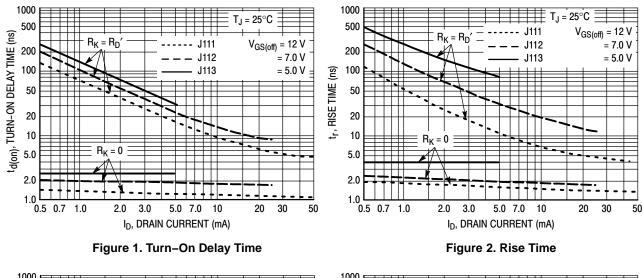
1. Pulse Width = 300 μ s, Duty Cycle = 3.0%.

ORDERING INFORMATION

Device	Package	Shipping [†]	
J111RL1	TO-92		
J111RL1G	TO-92 (Pb-Free)	2000 Units / Tape & Reel	
J111RLRA	TO-92		
J111RLRAG	TO-92 (Pb-Free)	2000 Units / Tape & Reel	
J111RLRP	TO-92		
J111RLRPG	TO-92 (Pb-Free)	2000 Units / Tape & Reel	
J112	TO-92		
J112G	TO-92 (Pb-Free)	1000 Units / Bulk	
J112RL1	TO-92		
J112RL1G	TO-92 (Pb-Free)	2000 Units / Tape & Reel	
J112RLRA	TO-92		
J112RLRAG	TO-92 (Pb-Free)	2000 Units / Tape & Reel	

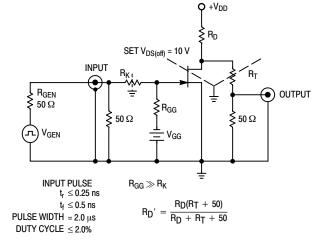
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

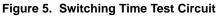
J111, J112



1000 1000 T_J = 25°C T_J = 25°C 500 500 (us) R_D′ Rĸ V_{GS(off)} = 12 V J111 V_{GS(off)} = 12 V J111 t_{d(off)}, TURN-OFF DELAY TIME 200 200 J112 ______ = 7.0 V – J112 = 5.0 V = 5.0 V J113 J113 100 100 (us) $R_{K} = R_{D}$ FALL TIME 50 50 20 20 R_K 10 10 $R_{K} = 0$ 5.0 5.0 2.0 2.0 1.0 1.0 0.5 0.7 1.0 2.0 3.0 5.0 7.0 10 20 30 50 0.5 0.7 1.0 2.0 3.0 5.0 7.0 10 20 30 ID, DRAIN CURRENT (mA) ID, DRAIN CURRENT (mA)

Figure 3. Turn–Off Delay Time





NOTE 1

Figure 4. Fall Time

50

The switching characteristics shown above were measured using a test circuit similar to Figure 5. At the beginning of the switching interval, the gate voltage is at Gate Supply Voltage ($-V_{GG}$). The Drain–Source Voltage (V_{DS}) is slightly lower than Drain Supply Voltage (V_{DD}) due to the voltage divider. Thus Reverse Transfer Capacitance (C_{rss}) or Gate–Drain Capacitance (C_{gd}) is charged to $V_{GG} + V_{DS}$.

During the turn–on interval, Gate–Source Capacitance (C_{gs}) discharges through the series combination of R_{Gen} and R_K . C_{gd} must discharge to $V_{DS(on)}$ through R_G and R_K in series with the parallel combination of effective load impedance (R'_D) and Drain–Source Resistance (r_{ds}). During the turn–off, this charge flow is reversed.

Predicting turn–on time is somewhat difficult as the channel resistance r_{ds} is a function of the gate–source voltage. While C_{gs} discharges, V_{GS} approaches zero and r_{ds} decreases. Since C_{gd} discharges through r_{ds} , turn–on time is non–linear. During turn–off, the situation is reversed with r_{ds} increasing as C_{gd} charges.

The above switching curves show two impedance conditions; 1) R_K is equal to R_D , which simulates the switching behavior of cascaded stages where the driving source impedance is normally the load impedance of the previous stage, and 2) $R_K = 0$ (low impedance) the driving source impedance is that of the generator.

TYPICAL SWITCHING CHARACTERISTICS

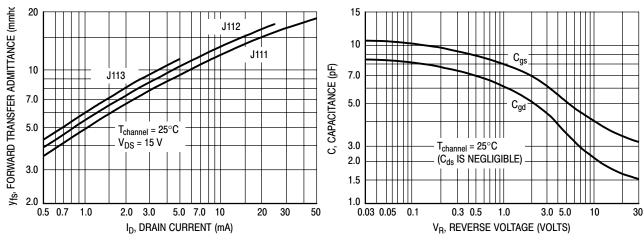
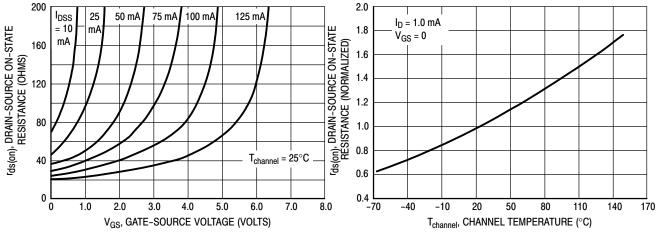


Figure 6. Typical Forward Transfer Admittance







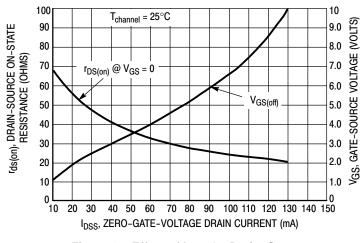


Figure 10. Effect of I_{DSS} On Drain–Source Resistance and Gate–Source Voltage

Figure 9. Effect of Temperature On Drain–Source On–State Resistance

NOTE 2

The Zero–Gate–Voltage Drain Current (I_{DSS}), is the principle determinant of other J-FET characteristics. Figure 10 shows the relationship of Gate–Source Off Voltage (V_{GS(off)} and Drain–Source On Resistance ($r_{ds(on)}$) to I_{DSS}. Most of the devices will be within±10% of the values shown in Figure 10. This data will be useful in predicting the characteristic variations for a given part number.

For example:

Unknown

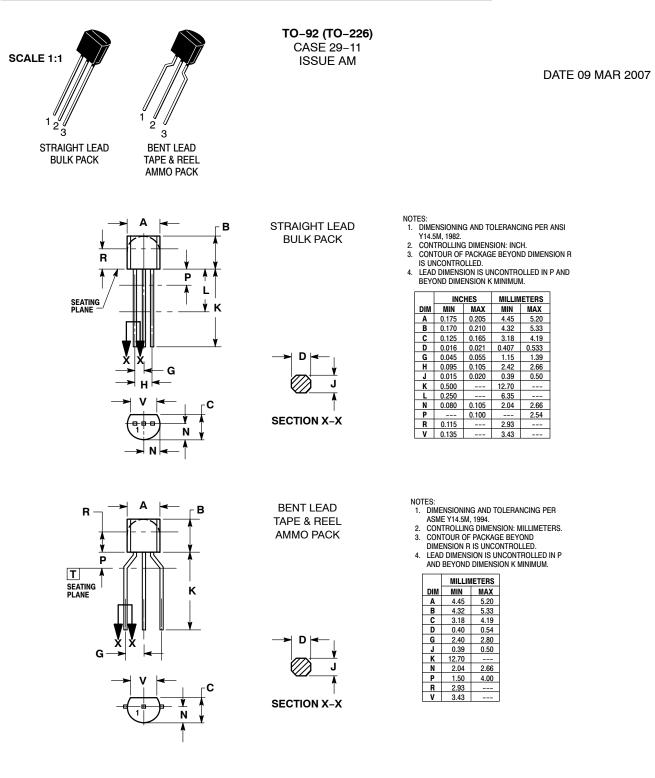
rds(on) and VGS range for an J112

The electrical characteristics table indicates that an J112 has an I_{DSS} range of 25 to 75 mA. Figure 10, shows $r_{ds(on)} = 52 \ \Omega$ for I_{DSS} = 25 mA and 30 Ω for I_{DSS} = 75 mA. The corresponding V_{GS} values are 2.2 V and 4.8 V.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

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STYLES ON PAGE 2

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DATE 09 MAR 2007

STYLE 1: PIN 1. EMITTER 2. BASE 3. COLLECTOR STYLE 6: PIN 1. GATE 2. SOURCE & SUBSTRATE 3. DRAIN STYLE 11: PIN 1. ANODE 2. CATHODE & ANODE 3. CATHODE STYLE 16: PIN 1. ANODE 2. GATE 3. CATHODE STYLE 21: PIN 1. COLLECTOR 2. EMITTER 3. BASE STYLE 22: PIN 1. VCC 2. GROUND 2 3. OUTPUT STYLE 31: PIN 1. GATE 2. DRAIN 3. SOURCE

	BASE EMITTER COLLECTOR
2.	SOURCE DRAIN GATE
2.	MAIN TERMINAL 1 Gate Main Terminal 2
2.	COLLECTOR BASE EMITTER
2.	SOURCE GATE DRAIN

2	1.	ANODE ANODE CATHODE
2	1. 2.	DRAIN Gate Source & Substrate
2	1. 2.	ANODE 1 GATE CATHODE 2
2	1. 2.	ANODE CATHODE NOT CONNECTED
2	1. 2.	GATE SOURCE DRAIN
2	1. 2.	CATHODE ANODE GATE

STYLE 33: PIN 1. RETURN 2. INPUT 3. OUTPUT

2.	CATHODE CATHODE ANODE
2.	BASE 1 EMITTER BASE 2
2.	EMITTER COLLECTOR BASE
	GATE ANODE CATHODE
2.	EMITTER Collector/Anode Cathode
2.	NOT CONNECTED ANODE CATHODE
2.	INPUT GROUND LOGIC

STYLE 4:

STYLE 5: PIN 1. DRAIN 2. SOURCE 3. GATE STYLE 10: PIN 1. CATHODE 2. GATE 3. ANODE STYLE 15: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 STYLE 20: PIN 1. NOT CONNECTED 2. CATHODE 3. ANODE STYLE 25: PIN 1. MT 1 2. GATE 3. MT 2 STYLE 30: PIN 1. DRAIN 2. GATE 3. SOURCE STYLE 35: PIN 1. DRAIN 2. GATE 3. SOURCE STYLE 35: PIN 1. GATE 2. COLLECTOR 3. EMITTER

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