

# MOSFET - N-Channel QFET®

600 V, 3.4 Ω, 3.0 A

## FQP3N60C

### General Description

This N-Channel enhancement mode power MOSFET is produced using ON Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

### Features

- 3.0 A, 600 V,  $R_{DS(on)} = 3.4 \Omega$  (Max.) at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 1.5 \text{ A}$
- Low Gate Charge (Typ. 10.5 nC)
- Low  $C_{rss}$  (Typ. 5.0 pF)
- 100% Avalanche Tested
- This is a Pb-Free Device

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit	
$V_{DSS}$	Drain-Source Voltage	600	V	
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V	
$I_D$	Drain Current	Continuous ( $T_C = 25^\circ\text{C}$ )	3	A
		Continuous ( $T_C = 100^\circ\text{C}$ )	1.8	
$I_{DM}$	Drain Current	Pulsed (Note 1)	12	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	150	mJ	
$I_{AR}$	Avalanche Current (Note 1)	3	A	
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	7.5	mJ	
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns	
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	75	W
		Derate above $25^\circ\text{C}$	0.62	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$	
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature
2.  $L = 30 \text{ mH}$ ,  $I_{AS} = 3 \text{ A}$ ,  $V_{DD} = 50 \text{ V}$ ,  $R_G = 25 \Omega$ , starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 3 \text{ A}$ ,  $di/dt \leq 200 \text{ A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$

### THERMAL CHARACTERISTICS

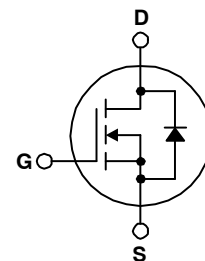
Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Maximum Thermal Resistance, Junction to Case	1.67	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient	62.5	$^\circ\text{C}/\text{W}$



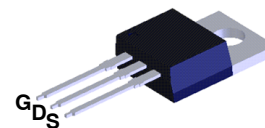
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$V_{DS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
600 V	$3.4 \Omega @ 10 \text{ V}$	3.0 A

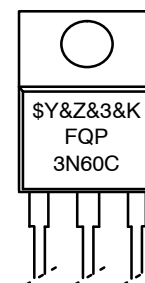


N-Channel MOSFET



TO-220-3LD  
CASE 340AT

### MARKING DIAGRAM



- $\$Y$  = ON Semiconductor Logo
- $\&Z$  = Assembly Plant Code
- $\&3$  = Data Code (Year & Week)
- $\&K$  = Lot Code
- FQP3N60C = Specific Device Code

### ORDERING INFORMATION

Device	Package	Shipping
FQP3N60C	TO-220-3LD (Pb-Free)	50 Units/Tube

# FQP3N60C

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	600	–	–	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	–	0.6	–	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V	–	–	1	μA
		V <sub>DS</sub> = 480 V, T <sub>C</sub> = 125 °C	–	–	10	
I <sub>GSSF</sub>	Gate –Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	–	–	100	nA
I <sub>GSSR</sub>	Gate –Body Leakage Current, Reverse	V <sub>GS</sub> = –30 V, V <sub>DS</sub> = 0 V			–100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	2.0	–	4.0	V
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.5 A	–	2.8	3.4	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 1.5 A	–	3.5	–	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	–	435	565	pF
C <sub>oss</sub>	Output Capacitance		–	45	60	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		–	5	8	pF

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 3 A, R <sub>G</sub> = 25 Ω (Note 4)	–	12	34	ns
t <sub>r</sub>	Turn–On Rise Time		–	30	70	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		–	35	80	ns
t <sub>f</sub>	Turn–Off Fall Time		–	35	80	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 480 V, I <sub>D</sub> = 3 A, V <sub>GS</sub> = 10 V (Note 4)	–	10.5	14	nC
Q <sub>gs</sub>	Gate–Source Charge		–	2.1	–	nC
Q <sub>gd</sub>	Gate–Drain Charge		–	4.5	–	nC

### DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I <sub>S</sub>	Maximum Continuous Drain–Source Diode Forward Current		–	–	3	A
I <sub>SM</sub>	Maximum Pulsed Drain–Source Diode Forward Current		–	–	12	A
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 3 A	–	–	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 3 A, dI <sub>F</sub> /dt = 100 A/μs	–	260	–	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	1.6	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature.

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## TYPICAL PERFORMANCE CHARACTERISTICS

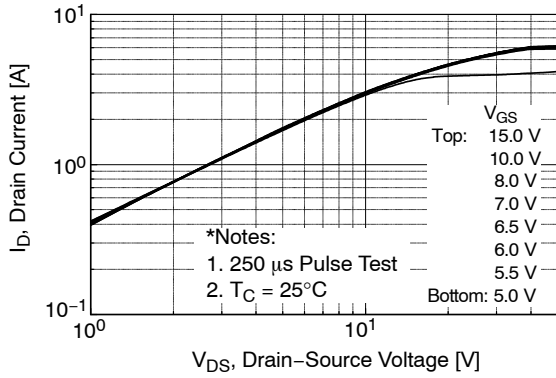


Figure 1. On-Region Characteristics

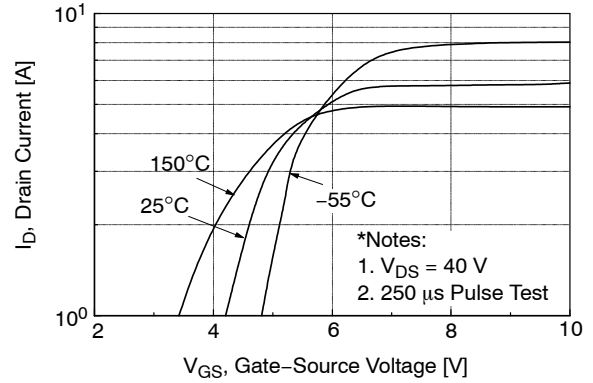


Figure 2. Transfer Characteristics

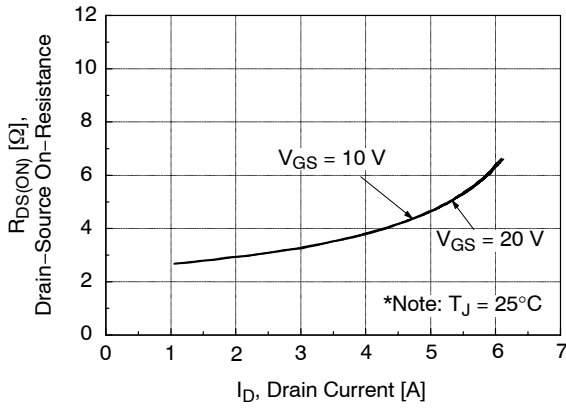


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

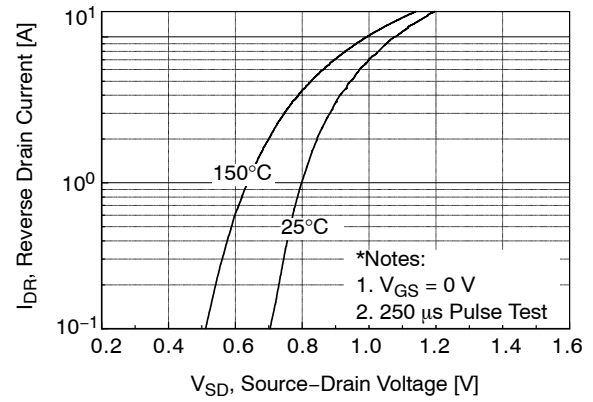


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

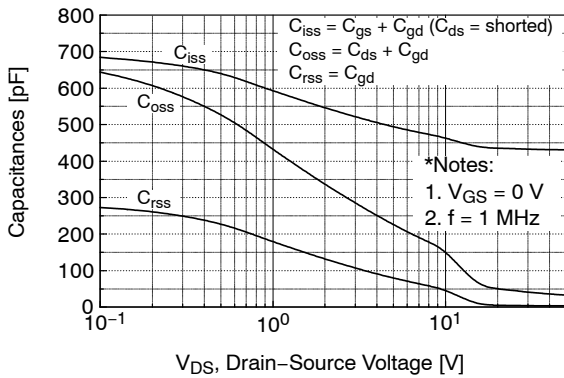


Figure 5. Capacitance Characteristics

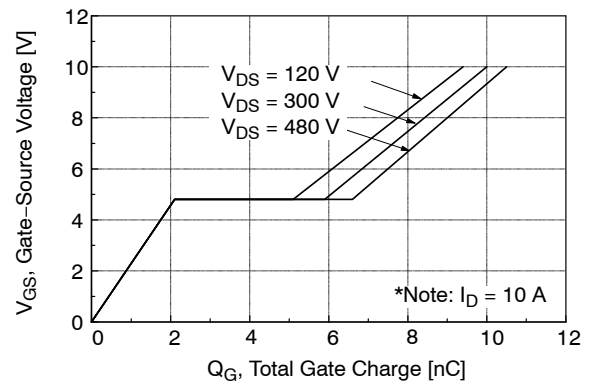
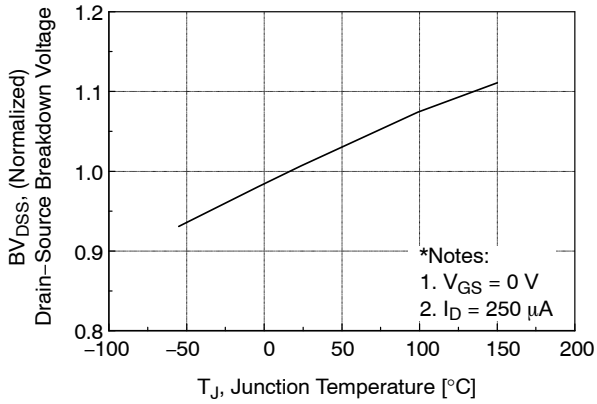


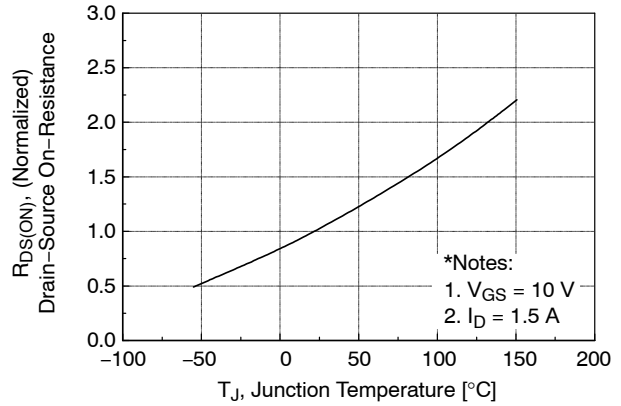
Figure 6. Gate Charge Characteristics

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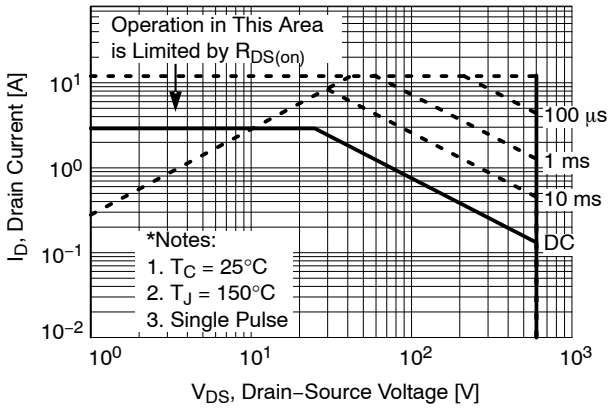
## TYPICAL PERFORMANCE CHARACTERISTICS



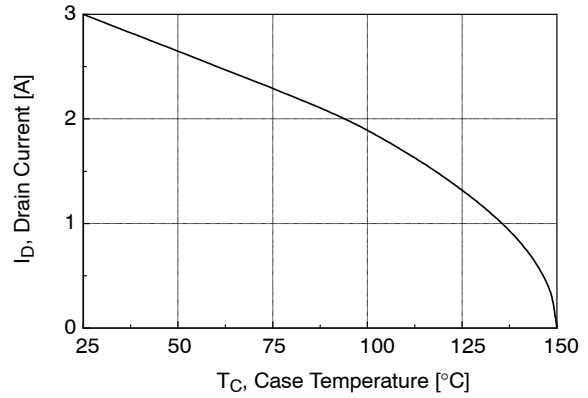
**Figure 7. Breakdown Voltage Variation vs. Temperature**



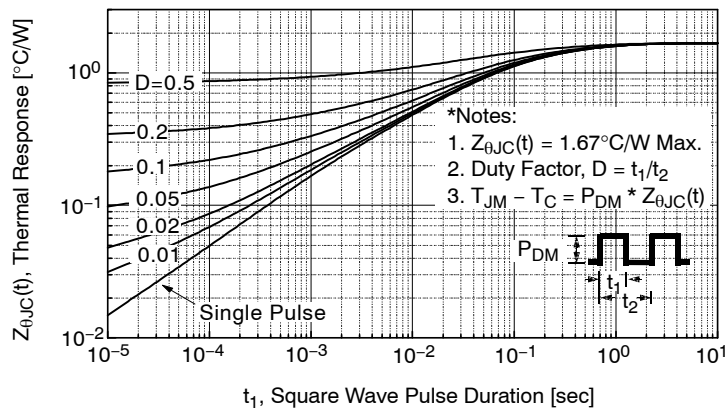
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

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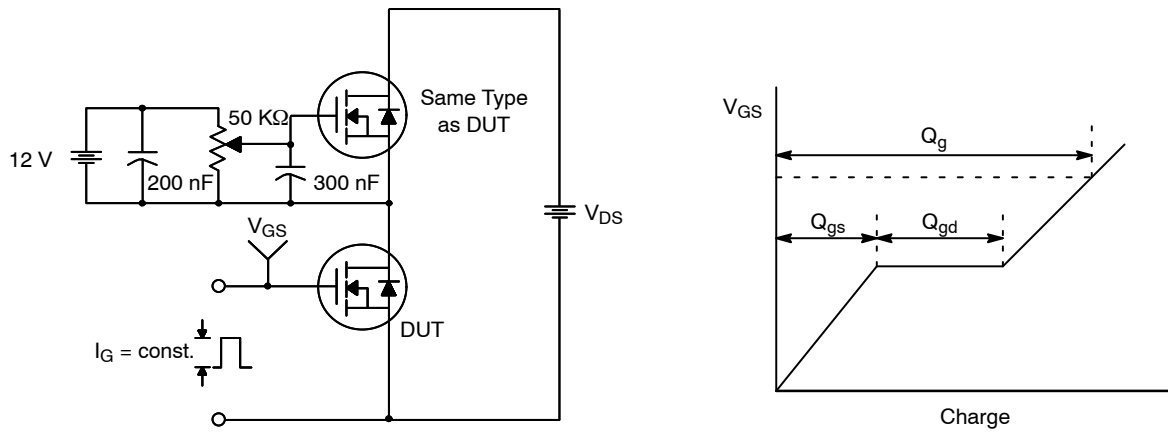


Figure 12. Gate Charge Test Circuit & Waveform

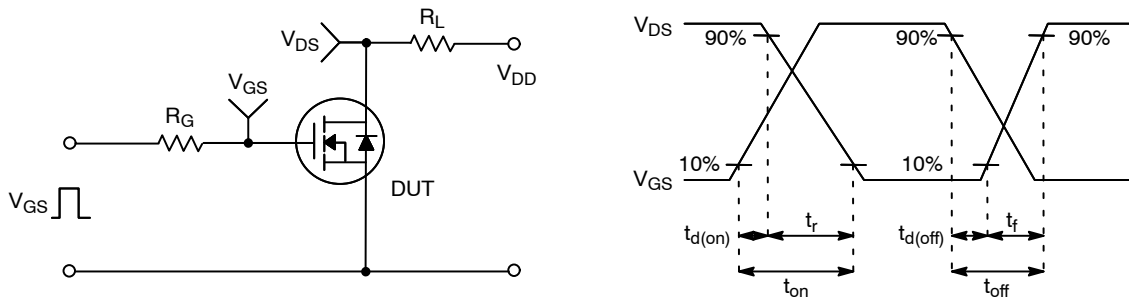


Figure 13. Resistive Switching Test Circuit & Waveforms

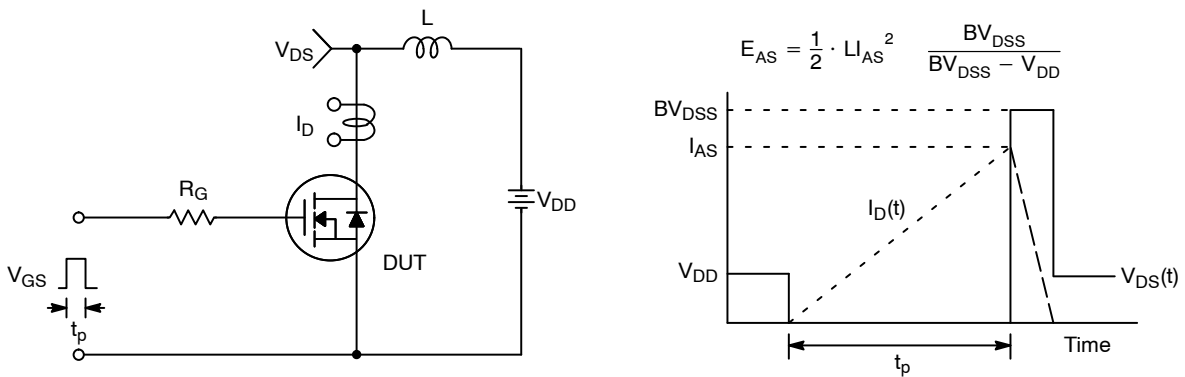
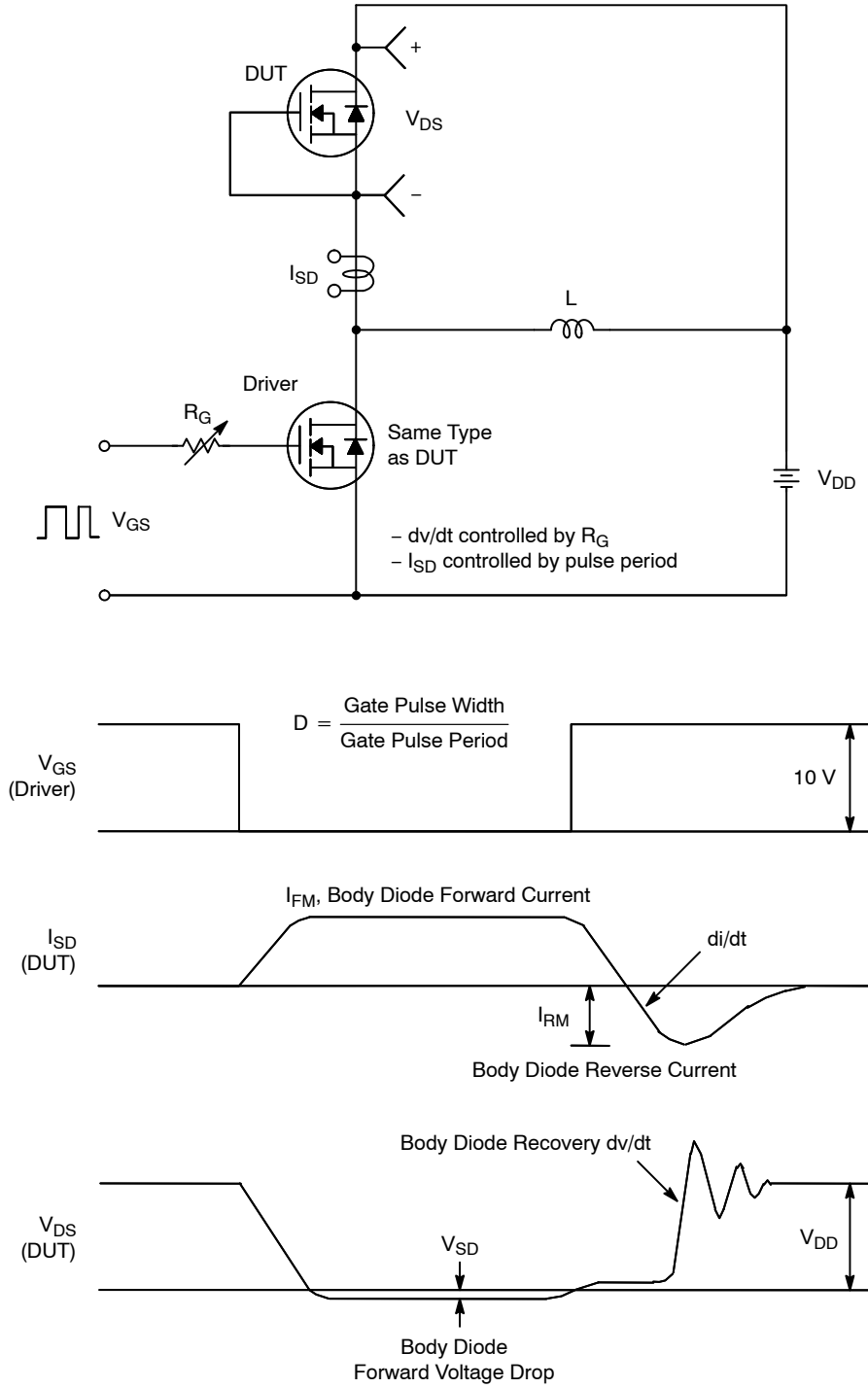


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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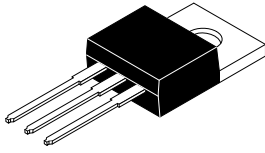


**Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms**

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

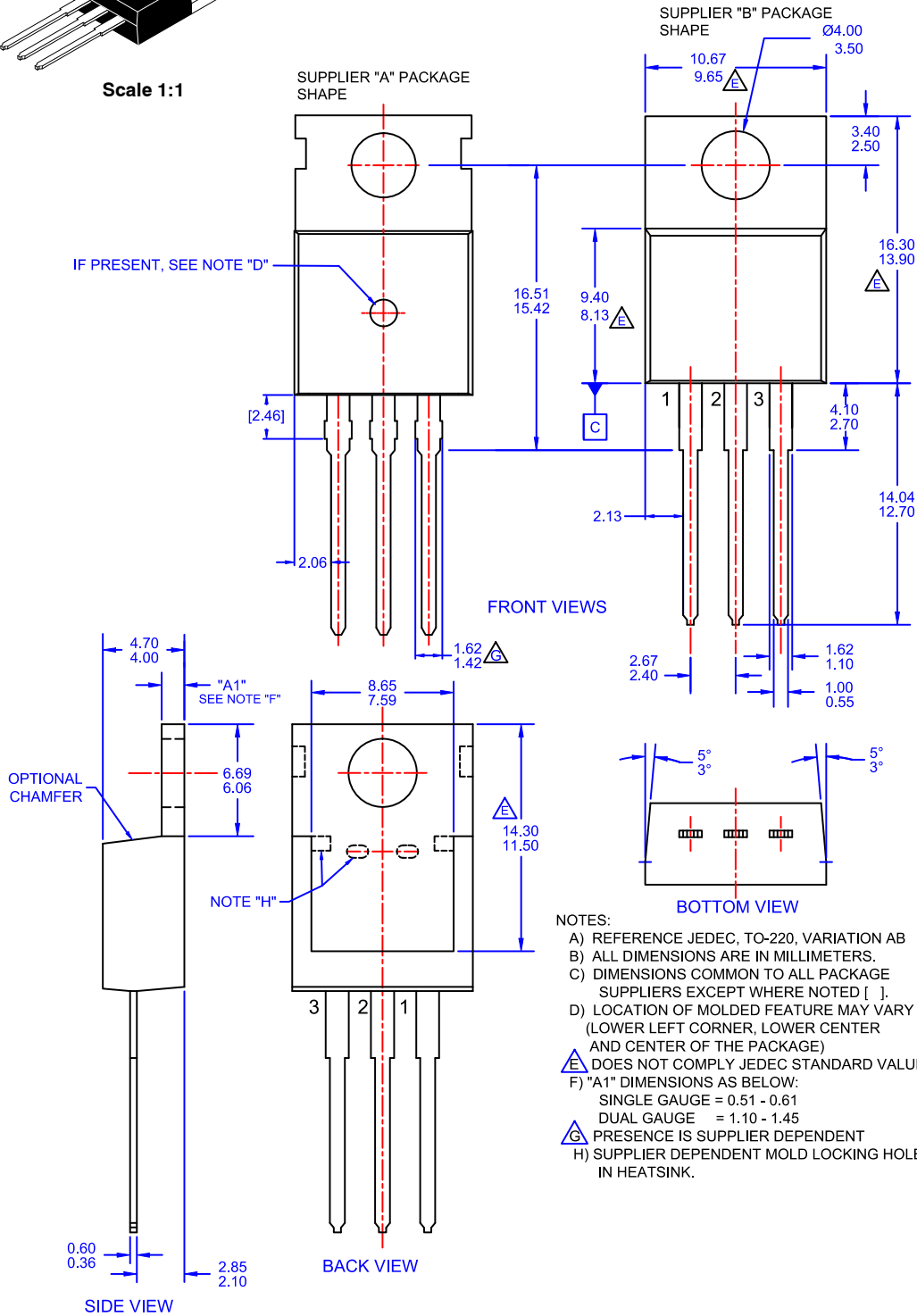
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Scale 1:1

### TO-220-3LD CASE 340AT ISSUE A

DATE 03 OCT 2017



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