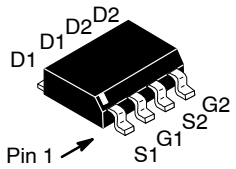
MOSFET – N-Channel, POWERTRENCH®

30 V, 7.5 A, 18 mΩ

FDS8978, FDS8978-F40

V_{DSS} MAX	$r_{DS(on)}$ MAX	I_D MAX
30 V	18 mΩ @ 10 V	7.5 A
	21 mΩ @ 4.5 V	



SOIC8
CASE 751EB

General Description

This N−Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$ and fast switching speed.

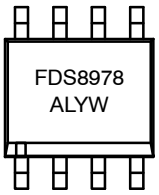
Features

- $r_{DS(on)}$ = 18 mΩ, V_{GS} = 10 V, I_D = 7.5 A
- $r_{DS(on)}$ = 21 mΩ, V_{GS} = 4.5 V, I_D = 6.9 A
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$
- Low Gate Charge
- High Power and Current Handling Capability
- 100% Rg Tested
- These Devices are Pb−Free and are RoHS Compliant

Applications

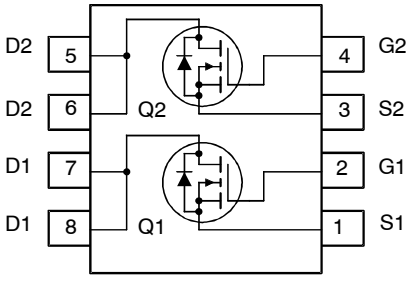
- DC/DC Converters

MARKING DIAGRAM



FDS8978 = Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

PIN CONNECTIONS



MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter		Ratings	Unit
V_{DSS}	Drain to Source Voltage		30	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current	Continuous (T_A = 25°C, V_{GS} = 10 V, $R_{\theta JA}$ = 50°C/W)	7.5	A
		Continuous (T_A = 25°C, V_{GS} = 4.5 V, $R_{\theta JA}$ = 50°C/W)	6.9	A
		Pulsed	49	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)		57	mJ
P_D	Power Dissipation		1.6	W
	Derate above 25°C		13	mW/°C
T_J, T_{STG}	Operating and Storage Temperature		−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Starting T_J = 25°C, L = 1 mH, I_{AS} = 7.5 A, V_{DD} = 30 V, V_{GS} = 10 V.

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

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THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 2)	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 2a)	78	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 2b)	135	°C/W

2. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.
   a. 78°C/W when mounted on a 0.5 in^2 pad of 2 oz copper.
   b. 125°C/W when mounted on a 0.02 in^2 pad of 2 oz copper.
   c. 135°C/W when mounted on a minimum pad.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	30	–	–	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J = 150°C	–	–	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.2	–	2.5	V
$r_{DS(on)}$	Drain to Source On Resistance	I_D = 7.5 A, V_{GS} = 10 V	–	14	18	mΩ
		I_D = 6.9 A, V_{GS} = 4.5 V	–	17	21	
		I_D = 7.5 A, V_{GS} = 10 V, T_J = 150°C	–	22	29	
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	–	907	1270	pF
C_{OSS}	Output Capacitance		–	191	–	pF
C_{RSS}	Reverse Transfer Capacitance		–	112	–	pF
R_G	Gate Resistance	V_{GS} = 0.5 V, f = 1 MHz	–	1.2	4.0	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10 V	V_{GS} = 0 V to 10 V, V_{DD} = 15 V, I_D = 7.5 A	–	17	26	nC
$Q_{g(5)}$	Total Gate Charge at 5 V	V_{GS} = 0 V to 5 V, V_{DD} = 15 V, I_D = 7.5 A	–	9	14	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 15 V, I_D = 7.5 A	–	2.3	–	nC
Q_{gs2}	Gate Charge Threshold to Plateau		–	1.5	–	nC
Q_{gd}	Gate to Drain "Miller" Charge		–	3.3	–	nC
SWITCHING CHARACTERISTICS (V_{GS} = 10 V)						
t_{ON}	Turn−On Time	V_{DD} = 15 V, I_D = 7.5 A, V_{GS} = 10 V, R_{GS} = 16 Ω	–	44	66	ns
$t_{d(ON)}$	Turn−On Delay Time		–	7	10.5	ns
t_r	Rise Time		–	37	55.5	ns
$t_{d(OFF)}$	Turn−Off Delay Time		–	48	72	ns
t_f	Fall Time		–	24	36	ns
t_{OFF}	Turn−Off Time		–	72	108	ns
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 7.5 A	–	–	1.25	V
		I_{SD} = 2.1 A	–	–	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 7.5 A, dI_{SD}/dt = 100 A/μs	–	19	25	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 7.5 A, dI_{SD}/dt = 100 A/μs	–	10	13	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

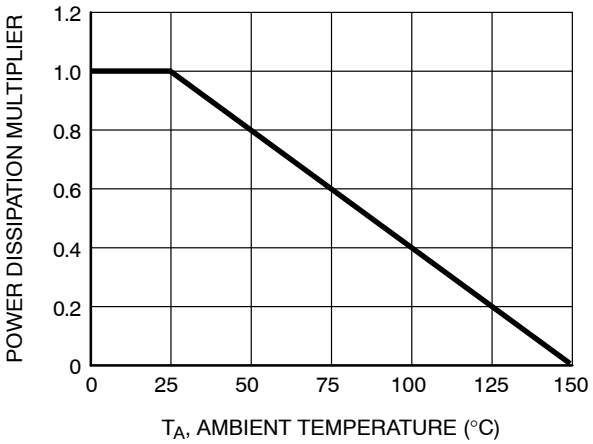


Figure 1. Normalized Power Dissipation vs. Ambient Temperature

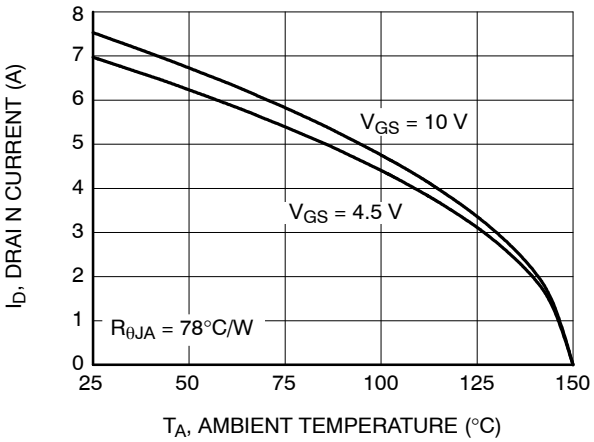


Figure 2. Maximum Continuous Drain Current vs. Ambient Temperature

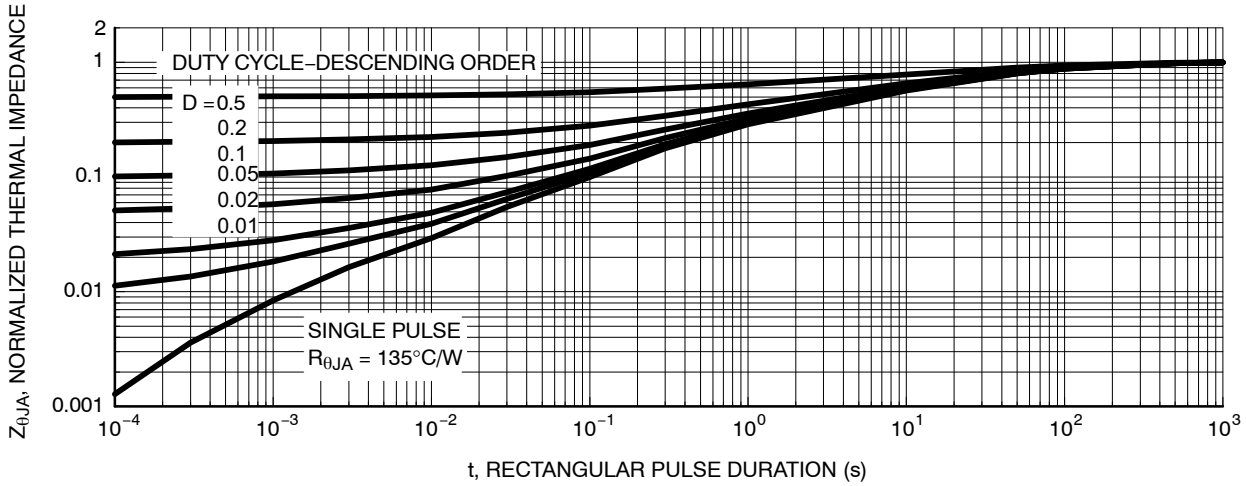


Figure 3. Normalized Maximum Transient Thermal Impedance

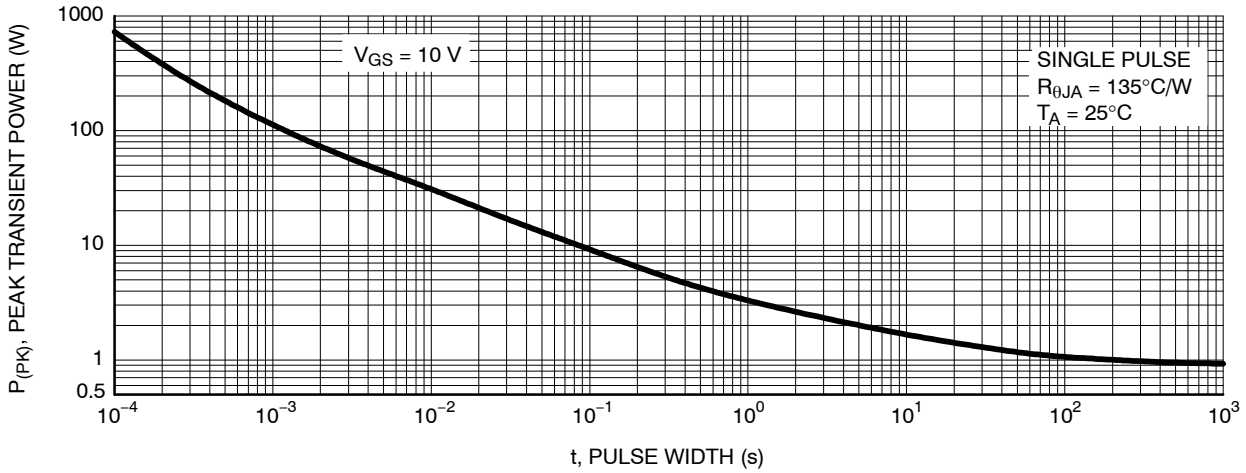
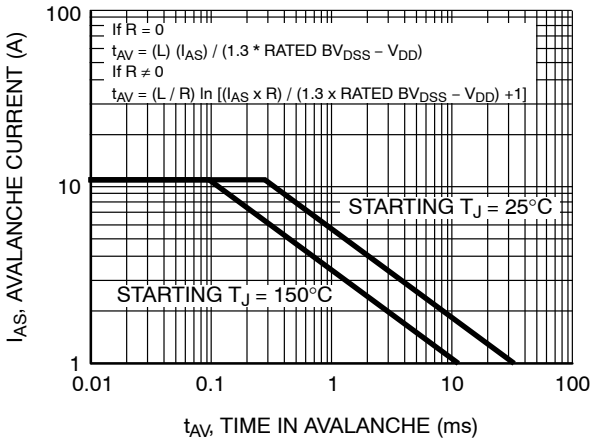


Figure 4. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted) (continued)



NOTE: Refer to **onsemi** Application Notes AN−7514 and AN−7515

Figure 5. Unclamped Inductive Switching Capability

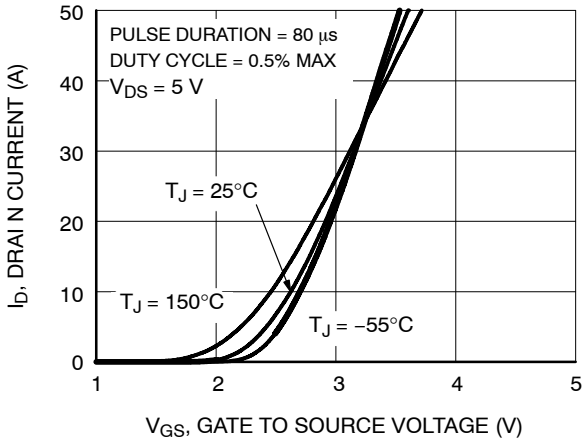


Figure 6. Transfer Characteristics

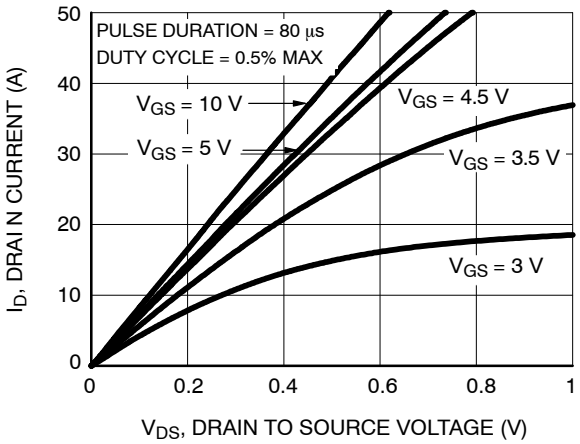


Figure 7. Saturation Characteristics

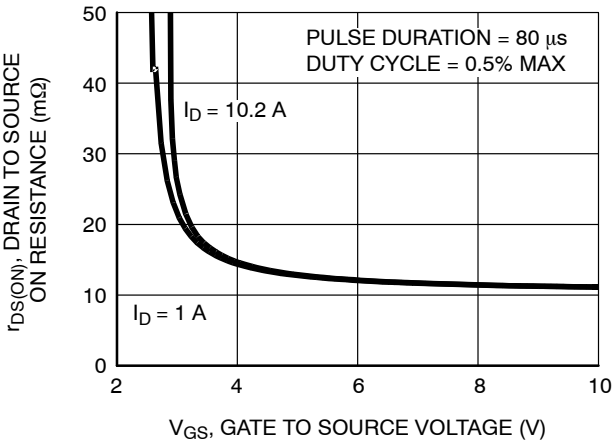


Figure 8. Drain to Source On Resistance vs. Gate Voltage and Drain Current

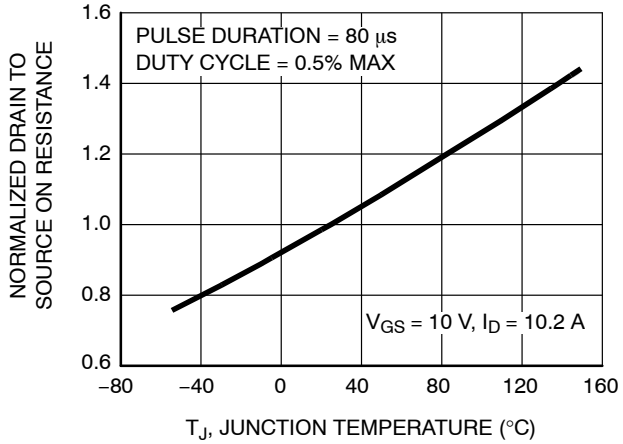


Figure 9. Normalized Drain to Source On Resistance vs. Junction Temperature

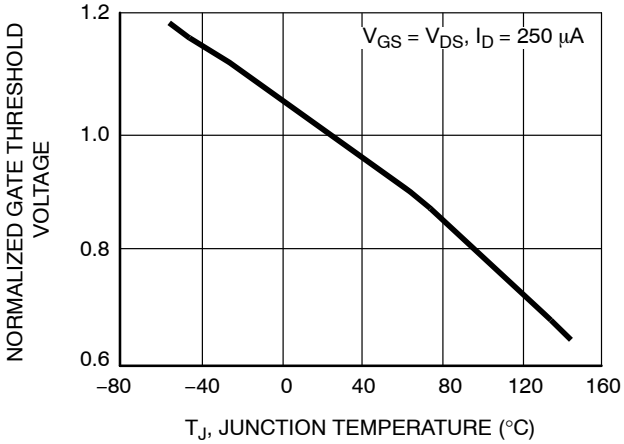


Figure 10. Normalized Gate Threshold Voltage vs. Junction Temperature

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted) (continued)

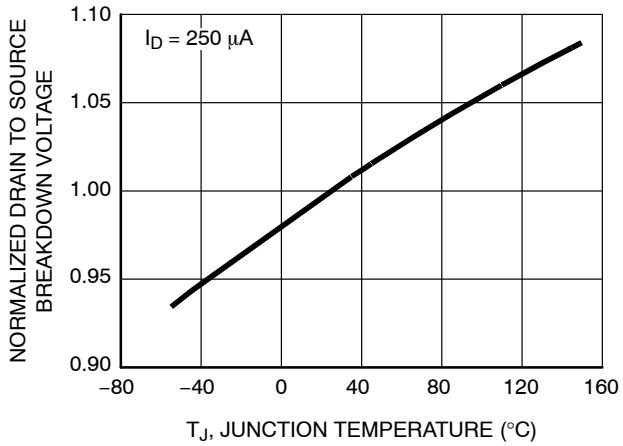


Figure 11. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

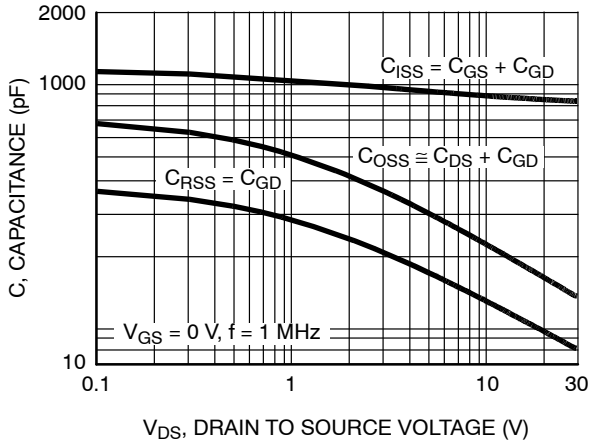


Figure 12. Capacitance vs. Drain to Source Voltage

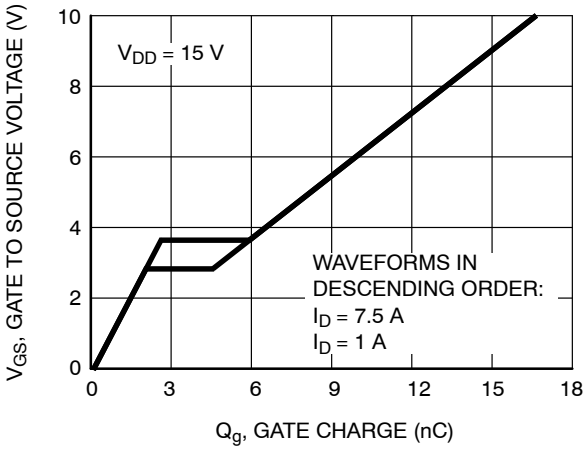


Figure 13. Gate Charge Waveforms for Constant Gate Currents

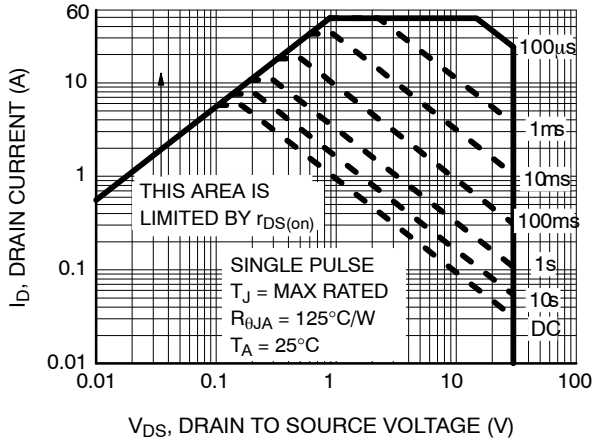


Figure 14. Forward Bis Safe Operating Area

TEST CIRCUITS AND WAVEFORMS

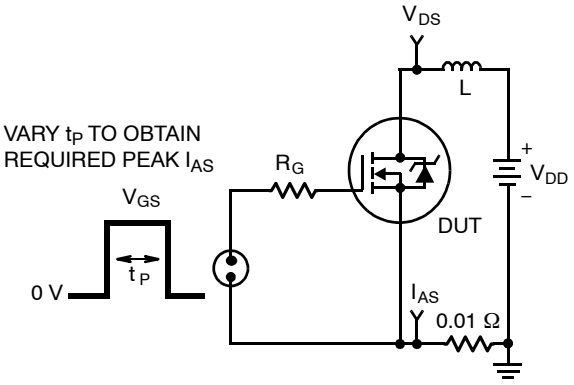


Figure 15. Unclamped Energy Test Circuit

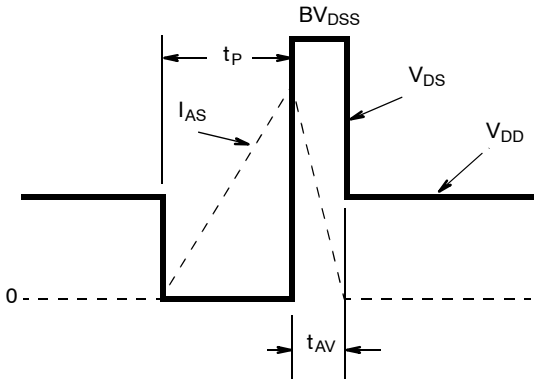


Figure 16. Unclamped Energy Waveforms

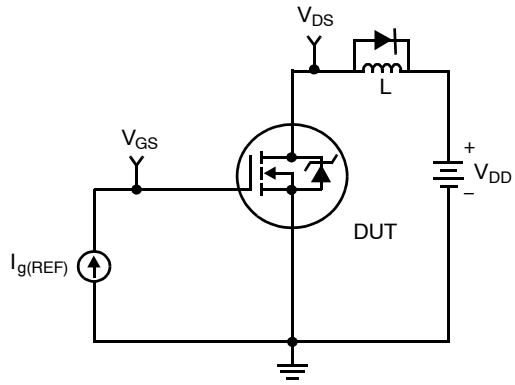


Figure 17. Gate Charge Test Circuit

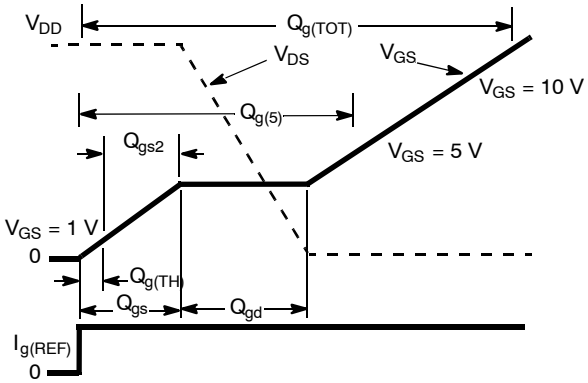


Figure 18. Gate Charge Waveforms

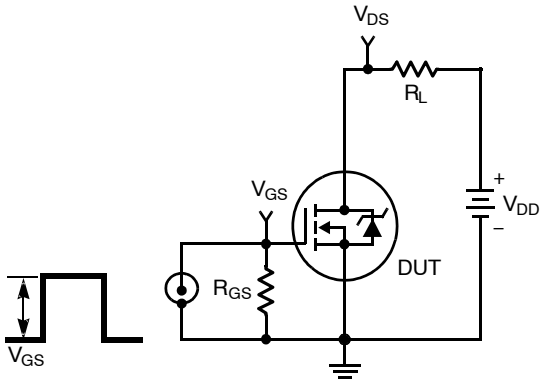


Figure 19. Switching Time Test Circuit

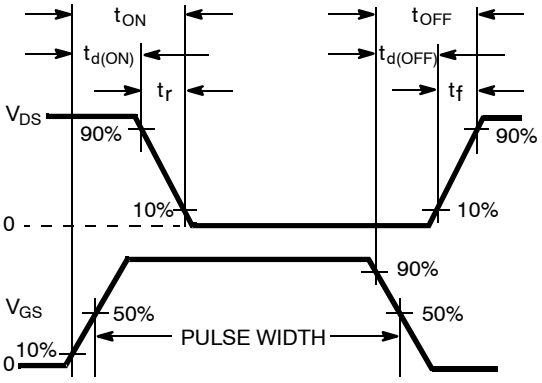


Figure 20. Switching Time Waveforms

THERMAL RESISTANCE VS. MOUNTING PAD AREA

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A (°C), and thermal resistance $R_{\theta JA}$ (°C/W) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad \text{(eq. 1)}$$

In using surface mount devices such as the SO8 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

onsemi provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR−4 board with 1 oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the **onsemi** device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 64 + \frac{26}{0.23 + \text{Area}} \quad \text{(eq. 2)}$$

The transient thermal impedance ($Z_{\theta JA}$) is also effected by varied top copper board area. Figure 22 shows the effect of copper pad area on single pulse transient thermal impedance. Each trace represents a copper pad area in square inches corresponding to the descending list in the graph. Spice and SABER thermal models are provided for each of the listed pad areas.

Copper pad area has no perceivable effect on transient thermal impedance for pulse widths less than 100 ms. For pulse widths less than 100 ms the transient thermal impedance is determined by the die and package. Therefore, CTHERM1 through CTHERM5 and RTHERM1 through RTHERM5 remain constant for each of the thermal models. A listing of the model component values is available in Table 1.

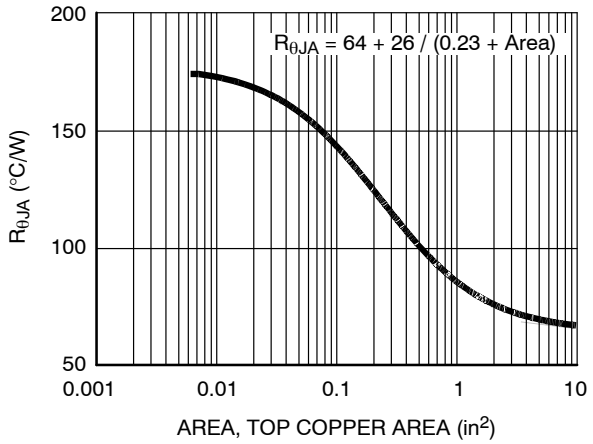


Figure 21. Thermal Resistance vs. Mounting Pad Area

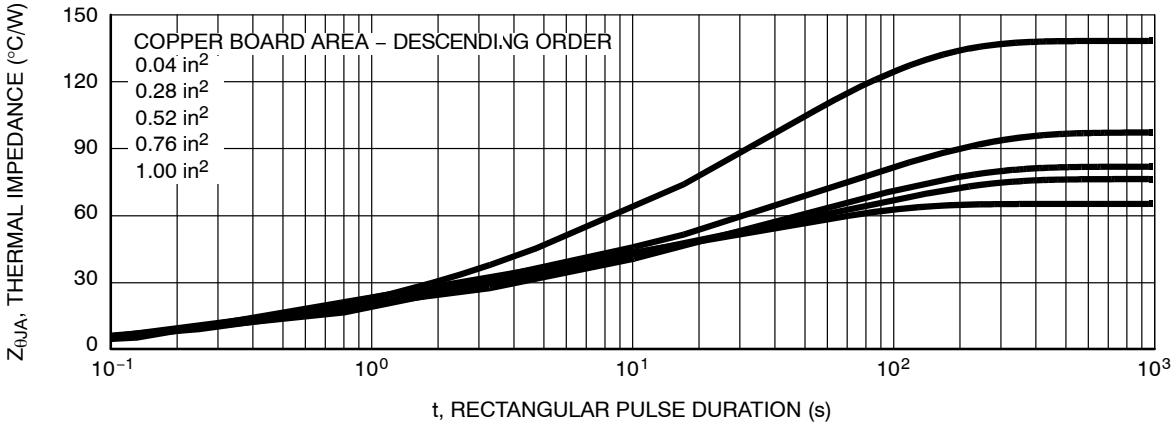


Figure 22. Thermal Impedance vs. Mounting Pad Area

PSPICE ELECTRICAL MODEL

```
.SUBCKT FDS8978 2 1 3
*February 2005

Ca 12 8 7.8e−10
Cb 15 14 7.8e−10
Cin 6 8 .78e−9
Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 32.9
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 5.29e−9
Ldrain 2 5 1.0e−9
Lsource 3 7 0.18e−9

RLgate 1 9 52.9
RLdrain 2 5 10
RLsource 3 7 1.8

Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 1.6e−3
Rgate 9 20 2.3
RSLC1 5 51 RSLCMOD 1e−6
RSLC2 5 50 1e3
Rsource 8 7 RsourceMOD 8.9e−3
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e−6*170),5))}

.MODEL DbodyMOD D (IS=2.0E−12 IKF=10 N=1.01 RS=7.0e−3 TRS1=8e−4 TRS2=2e−7
+CJO=3.5e−10 M=0.55 TT=7e−11 XTI=2)
.MODEL DbreakMOD D (RS=0.2 TRS1=1e−3 TRS2=−8.9e−6)
.MODEL DplcapMOD D (CJO=3.8e−10 IS=1e−30 N=10 M=0.45)

.MODEL MstroMOD NMOS (VTO=2.36 KP=150 IS=1e−30 N=10 TOX=1 L=1u W=1u)
.MODEL MmedMOD NMOS (VTO=1.95 KP=5.0 IS=1e−30 N=10 TOX=1 L=1u W=1u RG=2.3)
.MODEL MweakMOD NMOS (VTO=1.57 KP=0.02 IS=1e−30 N=10 TOX=1 L=1u W=1u RG=23 RS=0.1)
```

.MODEL RbreakMOD RES (TC1=8.3e−4 TC2=−8e−7)
.MODEL RdrainMOD RES (TC1=15e−3 TC2=0.1e−5)
.MODEL RSLCMOD RES (TC1=1e−4 TC2=1e−6)
.MODEL RsourceMOD RES (TC1=1e−3 TC2=3e−6)
.MODEL RvtempMOD RES (TC1=−1.8e−3 TC2=2e−7)
.MODEL RvthresMOD RES (TC1=−2.0e−3 TC2=−6e−6)
.MODEL S1AMOD VSWITCH (RON=1e−5 ROFF=0.1 VON=−4 VOFF=−3.5)
.MODEL S1BMOD VSWITCH (RON=1e−5 ROFF=0.1 VON=−3.5 VOFF=−4)
.MODEL S2AMOD VSWITCH (RON=1e−5 ROFF=0.1 VON=−1.5 VOFF=−1.0)
.MODEL S2BMOD VSWITCH (RON=1e−5 ROFF=0.1 VON=−1.0 VOFF=−1.5)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub−Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

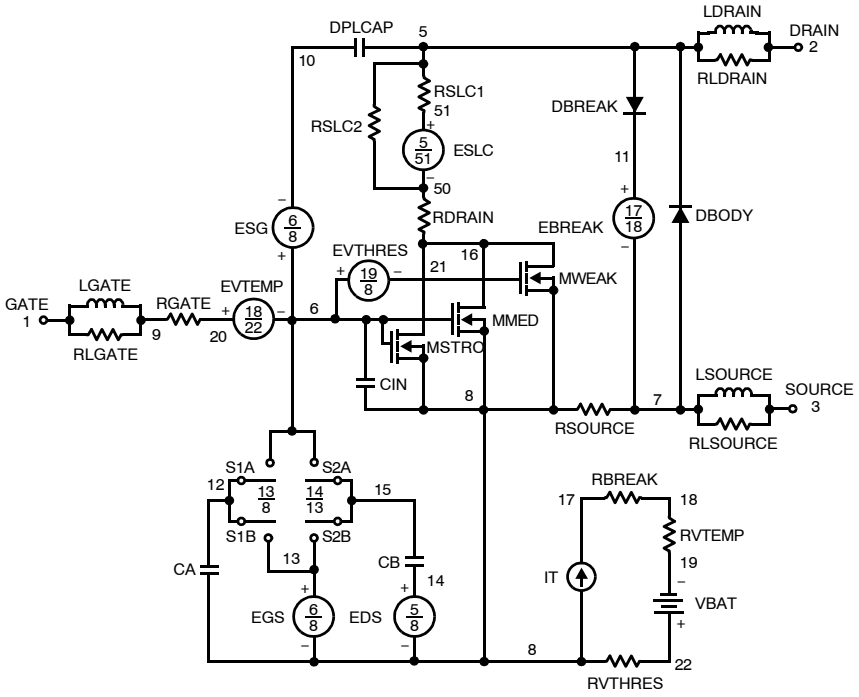


Figure 23.

SABER ELECTRICAL MODEL

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REV February 2005
template FDS8978 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod = (isl=2.0e−12,ikf=10,nl=1.01,rs=7.0e−3,trs1=8e−4,trs2=2e−7,cjo=3.5e−10,m=0.55,tt=7e−11,xti=2)
dp..model dbreakmod = (rs=0.2,trs1=1e−3,trs2=−8.9e−6)
dp..model dplcapmod = (cjo=3.8e−10,isl=10e−30,nl=10,m=0.45)
m..model mstrongmod = (type=_n,vto=2.36,kp=150,is=1e−30, tox=1)
m..model mmedmod = (type=_n,vto=1.95,kp=5.0,is=1e−30, tox=1)
m..model mweakmod = (type=_n,vto=1.57,kp=0.02,is=1e−30, tox=1,rs=0.1)
sw_vcsp..model s1amod = (ron=1e−5,roff=0.1,von=−4,voff=−3.5)
sw_vcsp..model s1bmod = (ron=1e−5,roff=0.1,von=−3.5,voff=−4)
sw_vcsp..model s2amod = (ron=1e−5,roff=0.1,von=−1.5,voff=−1.0)
sw_vcsp..model s2bmod = (ron=1e−5,roff=0.1,von=−1.0,voff=−1.5)
c.ca n12 n8 = 7.8e−10
c.cb n15 n14 = 7.8e−10
c.cin n6 n8 = .78e−9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 32.9
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

l.lgate n1 n9 = 5.29e−9
l.ldrain n2 n5 = 1.0e−9
l.lsource n3 n7 = 0.18e−9

res.rlgate n1 n9 = 52.9
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 1.8

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1=8.3e−4,tc2=−8e−7
res.rdrain n50 n16 = 1.6e−3, tc1=15e−3,tc2=0.1e−5
res.rgate n9 n20 = 2.3
res.rslc1 n5 n51 = 1e−6, tc1=1e−4,tc2=1e−6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 8.9e−3, tc1=1e−3,tc2=3e−6
res.rvthres n22 n8 = 1, tc1=−2.0e−3,tc2=−6e−6
res.rvtemp n18 n19 = 1, tc1=−1.8e−3,tc2=2e−7
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod
```

```
v.vbat n22 n19 = dc=1
equations {
i (n51−>n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e−9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/170))** 5))
}
}
```

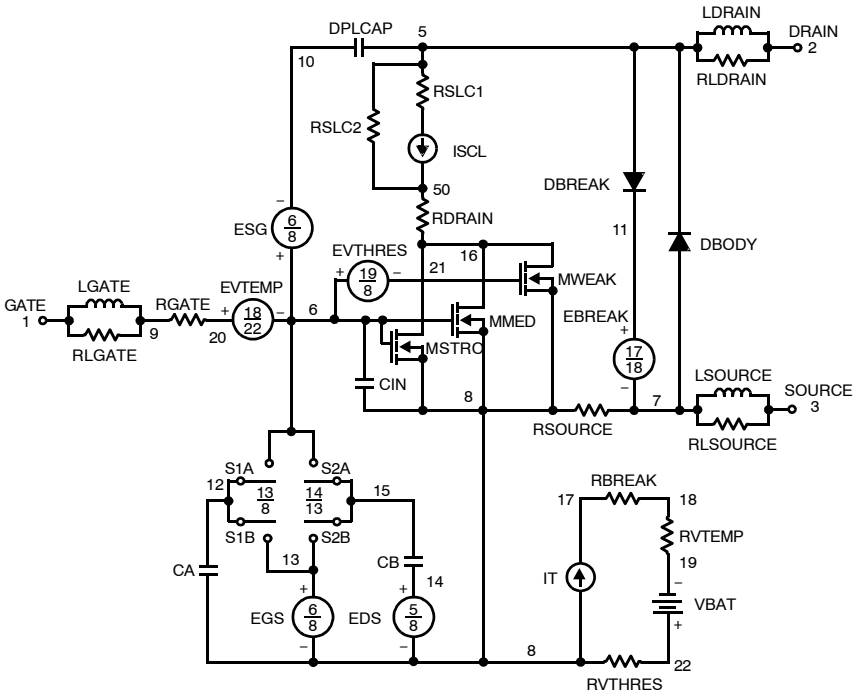

Figure 24.

SPICE THERMAL MODEL

REV February 2005
template FDS8878 n2,n1,n3
Copper Area =1.0 in^2
CTHERM1 TH 8 2.0e−3
CTHERM2 8 7 5.0e−3
CTHERM3 7 6 1.0e−2
CTHERM4 6 5 4.0e−2
CTHERM5 5 4 9.0e−2
CTHERM6 4 3 2e−1
CTHERM7 3 2 1
CTHERM8 2 TL 3

RTHERM1 TH 8 1e−1
RTHERM2 8 7 5e−1
RTHERM3 7 6 1
RTHERM4 6 5 5
RTHERM5 5 4 8
RTHERM6 4 3 12
RTHERM7 3 2 18
RTHERM8 2 TL 25

SABER THERMAL MODEL

Copper Area = 1.0 in^2
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 8 =2.0e−3
ctherm.ctherm2 8 7 =5.0e−3
ctherm.ctherm3 7 6 =1.0e−2
ctherm.ctherm4 6 5 =4.0e−2
ctherm.ctherm5 5 4 =9.0e−2
ctherm.ctherm6 4 3 =2e−1
ctherm.ctherm7 3 2 1
ctherm.ctherm8 2 tl 3

rtherm.rtherm1 th 8 =1e−1
rtherm.rtherm2 8 7 =5e−1
rtherm.rtherm3 7 6 =1
rtherm.rtherm4 6 5 =5
rtherm.rtherm5 5 4 =8
rtherm.rtherm6 4 3 =12
rtherm.rtherm7 3 2 =18
rtherm.rtherm8 2 tl =25
}

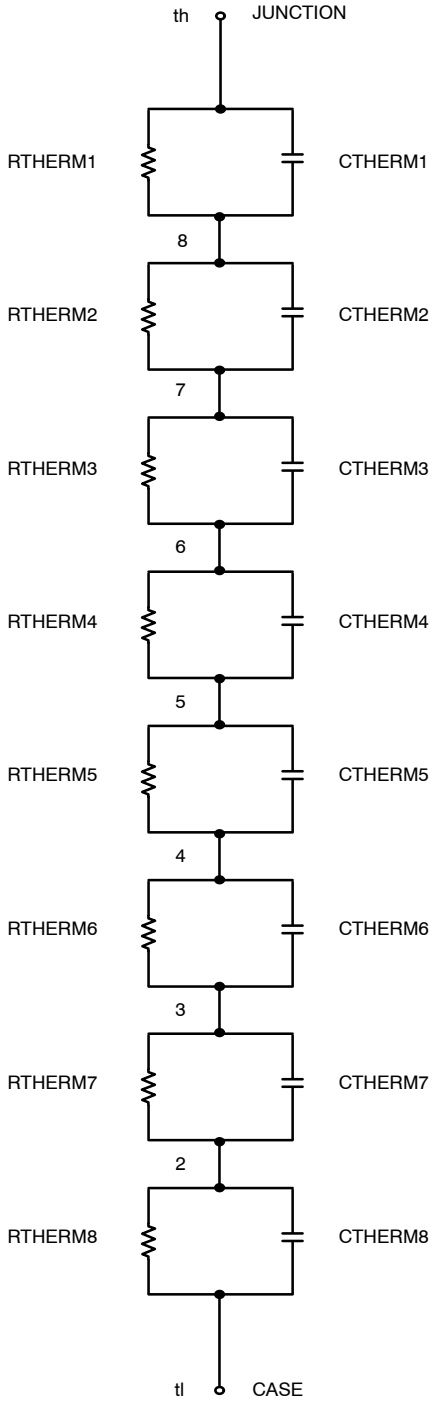

Figure 25.

Table 1. THERMAL MODELS

COMPONANT	0.04 in^2	0.28 in^2	0.52 in^2	0.76 in^2	1.0 in^2
CTHERM6	1.2e−1	1.5e−1	2.0e−1	2.0e−1	2.0e−1
CTHERM7	0.5	1.0	1.0	1.0	1.0
CTHERM8	1.3	2.8	3.0	3.0	3.0
RTHERM6	26	20	15	13	12
RTHERM7	39	24	21	19	18
RTHERM8	55	38.7	31.3	29.7	25

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package Type	Shipping†
FDS8978	FDS8978	SOIC8 (Pb−Free)	2500 / Tape & Reel
FDS8978−F40	FDS8978	SOIC8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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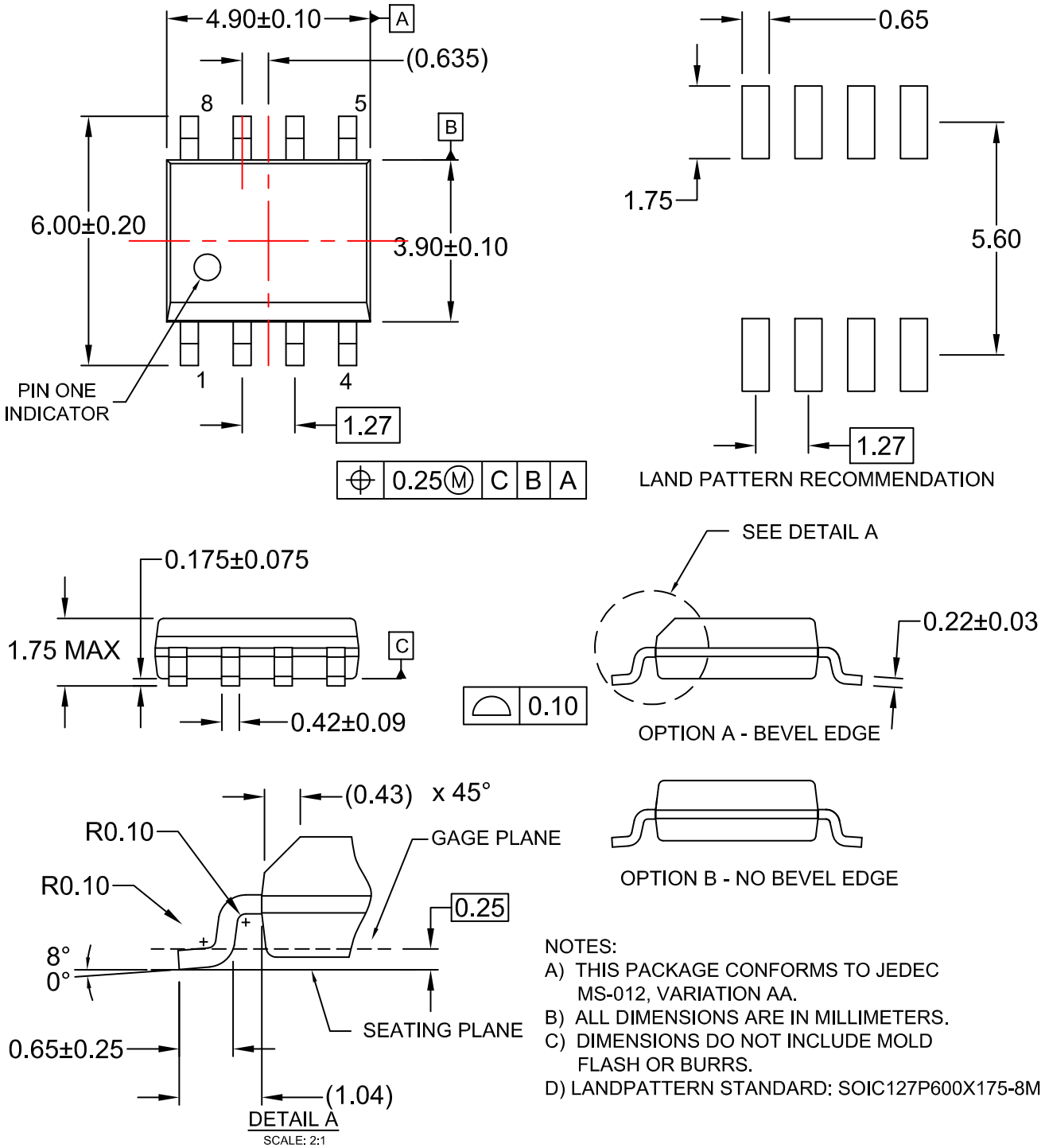
SOIC8
CASE 751EB
ISSUE A

DATE 24 AUG 2017



NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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