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# FDMS86181E

## MOSFET, N-Channel, Shielded Gate, POWERTRENCH®

100 V, 124 A, 4.2 mΩ

### General Description

This N-Channel MV MOSFET is produced using ON Semiconductor's advanced POWERTRENCH® process that incorporates Shielded Gate technology. This process has been optimized to minimise on-state resistance and yet maintain superior switching performance with best in class soft body diode.

### Features

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 4.2 mΩ at  $V_{GS} = 10$  V,  $I_D = 44$  A
- Max  $r_{DS(on)}$  = 12 mΩ at  $V_{GS} = 6$  V,  $I_D = 22$  A
- ADD
- 50% lower  $Q_{rr}$  than other MOSFET suppliers
- Lowers switching noise/EMI
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

### Applications

- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive
- Solar

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

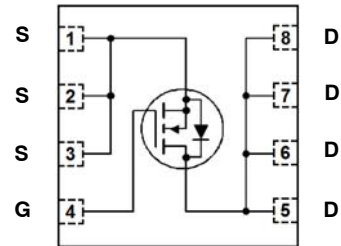
Symbol	Parameter	Value	Unit
$V_{DS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current:		A
	- Continuous $T_C = 25^\circ\text{C}$ (Note 5)	124	
	- Continuous $T_C = 100^\circ\text{C}$ (Note 5)	78	
	- Pulsed (Note 4)	510	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	337	mJ
$P_D$	Power Dissipation:		W
	$T_C = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$ (Note 1a)	125 2.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

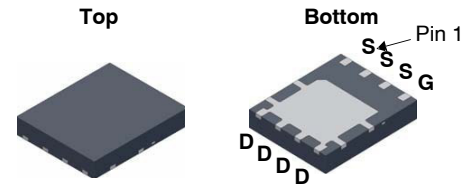


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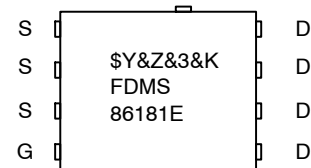


N-Channel MOSFET



Power 56  
(PQFN8)  
CASE 483AE

### MARKING DIAGRAM



\$Y = ON Semiconductor Logo  
 &Z = Assembly Plant Code  
 &3 = Data Code (Year & Week)  
 &K = Lot  
 FDMS86181E = Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FDMS86181E

## PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Quantity
FDMS86181E	FDMS86181E	Power 56 (PQFN8) (Pb-Free / Halogen Free)	3000/Tape&Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$ , $V_{GS} = 0 \text{ V}$	100			V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		60		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}$ , $V_{GS} = 0 \text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current, Forward	$V_{GS} = \pm 20 \text{ V}$ , $V_{DS} = 0 \text{ V}$			100	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250 \mu\text{A}$	2.0	3.1	4.0	V
$\Delta V_{GS(th)} / \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		-9		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}$ , $I_D = 44 \text{ A}$		3.3	4.2	m $\Omega$
		$V_{GS} = 6 \text{ V}$ , $I_D = 22 \text{ A}$		5.3	12	
		$V_{GS} = 10 \text{ V}$ , $I_D = 44 \text{ A}$ , $T_J = 125^\circ\text{C}$		5.7	7.8	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10 \text{ V}$ , $I_D = 44 \text{ A}$		116		S

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 50 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $f = 1 \text{ MHz}$		2945	4125	pF
$C_{oss}$	Output Capacitance			1730	2425	pF
$C_{rss}$	Reverse Transfer Capacitance			20	40	pF
$R_g$	Gate Resistance	$f = 1 \text{ MHz}$	0.1	1.3	2.6	$\Omega$

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50 \text{ V}$ , $I_D = 44 \text{ A}$ , $V_{GS} = 10 \text{ V}$ , $R_{GEN} = 6 \Omega$		17	31	ns
$t_r$	Rise Time			9	18	ns
$t_{d(off)}$	Turn-Off Delay Time			25	40	ns
$t_f$	Fall Time			6	12	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0 \text{ V}$ to $10 \text{ V}$ , $V_{DD} = 50 \text{ V}$ , $I_D = 44 \text{ A}$		42	59	nC
		$V_{GS} = 0 \text{ V}$ to $6 \text{ V}$ , $V_{DD} = 50 \text{ V}$ , $I_D = 44 \text{ A}$		27	38	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = 50 \text{ V}$ , $I_D = 44 \text{ A}$		13		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			9.3		nC

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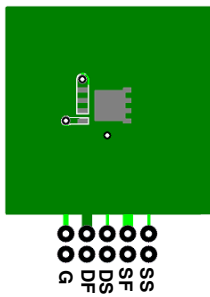
## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.1\text{ A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 44\text{ A}$ (Note 2)		0.8	1.3	
$t_{rr}$	Reverse Recovery Time	$I_F = 20\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		32	52	ns
$Q_{rr}$	Reverse Recovery Charge			57	92	
$t_{rr}$	Reverse Recovery Time	$I_F = 20\text{ A}, di/dt = 1000\text{ A}/\mu\text{s}$		25	40	ns
$Q_{rr}$	Reverse Recovery Charge			158	253	

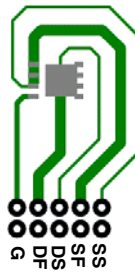
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



a. 50 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- $E_{AS}$  of 337 mJ is based on starting  $T_J = 25^\circ\text{C}$ , N-ch:  $L = 3\text{ mH}$ ,  $I_{AS} = 15\text{ A}$ ,  $V_{DD} = 100\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 49\text{ A}$ .
- Pulsed  $I_D$  please refer to Figure 11 SOA graph for more details.
- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

## TYPICAL CHARACTERISTICS

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

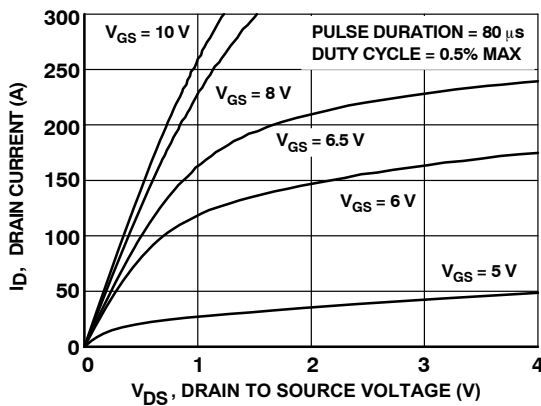


Figure 1. On Region Characteristics

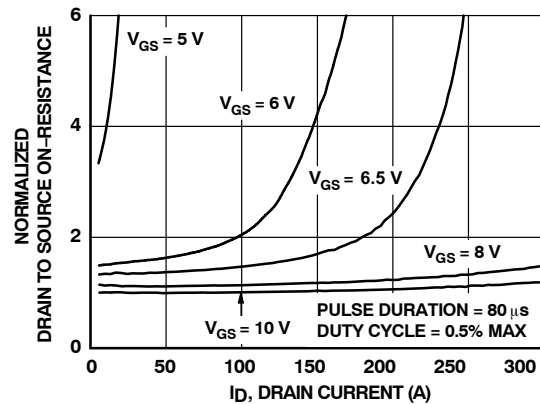


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

TYPICAL CHARACTERISTICS (continued)

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

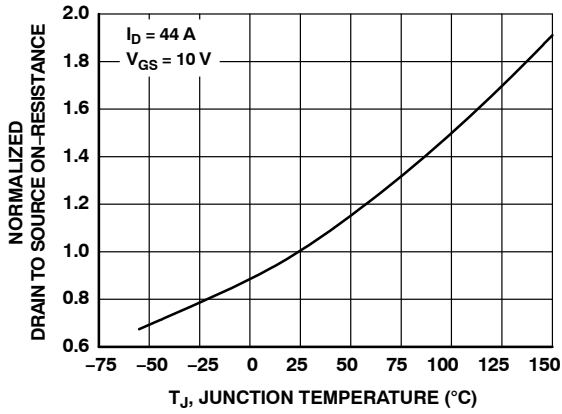


Figure 3. Normalized On Resistance vs. Junction Temperature

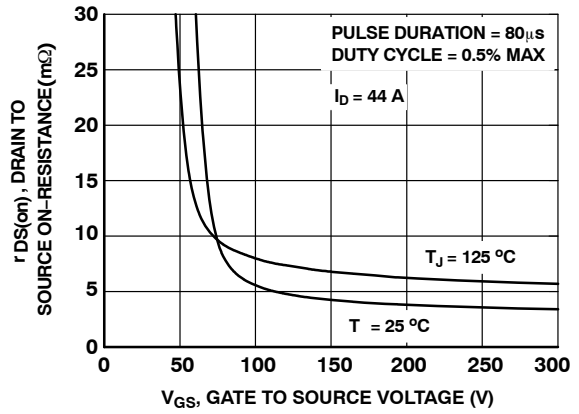


Figure 4. On-Resistance vs. Gate to Source Voltage

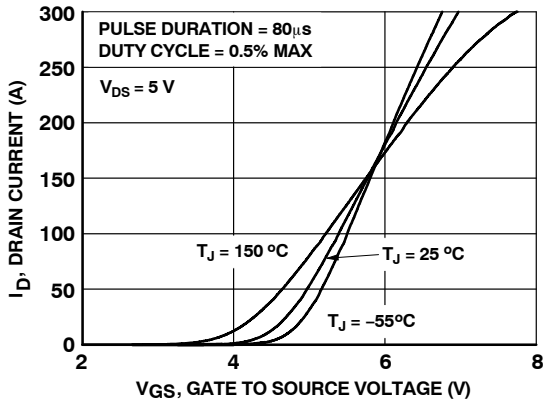


Figure 5. Transfer Characteristics

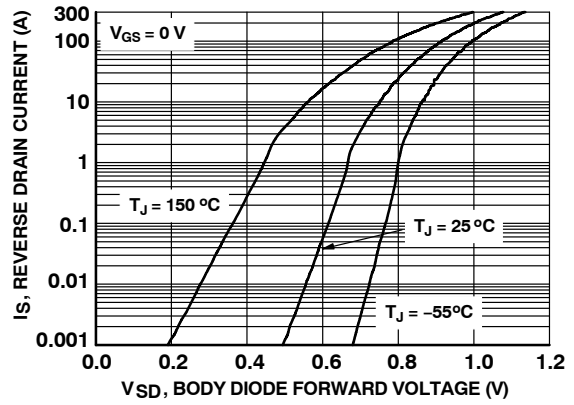


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

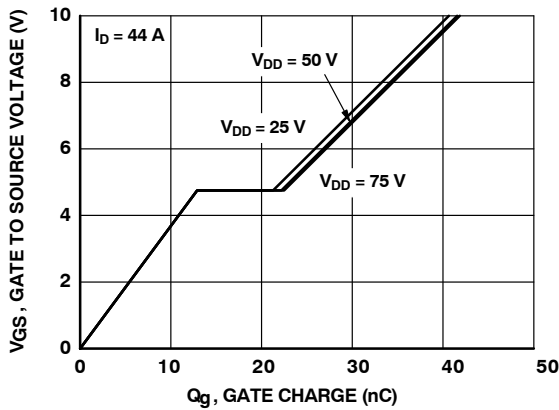


Figure 7. Gate Charge Characteristics

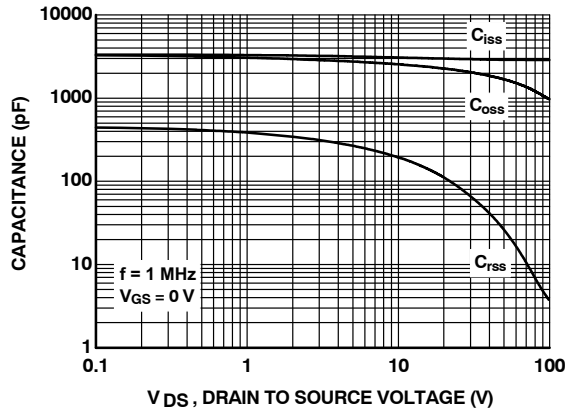


Figure 8. Capacitance vs. Drain to Source Voltage

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## TYPICAL CHARACTERISTICS (continued)

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

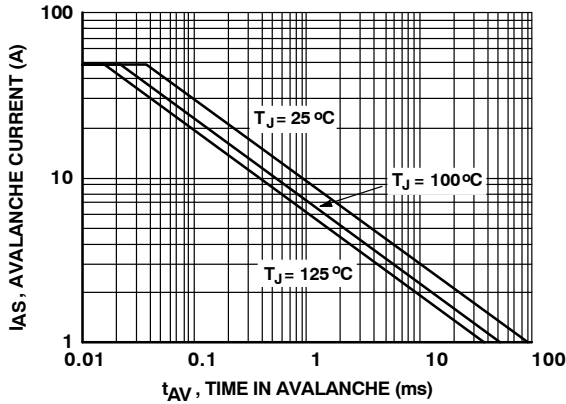


Figure 9. Unclamped Inductive Switching Capability

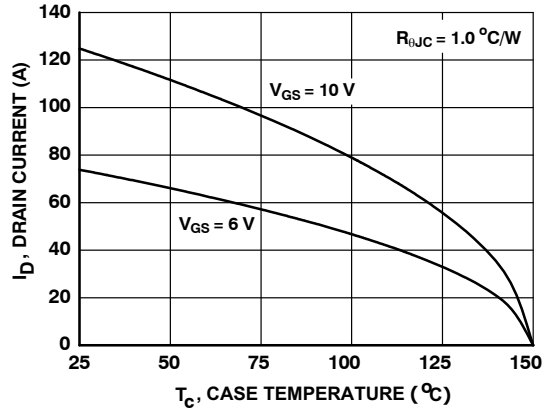


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

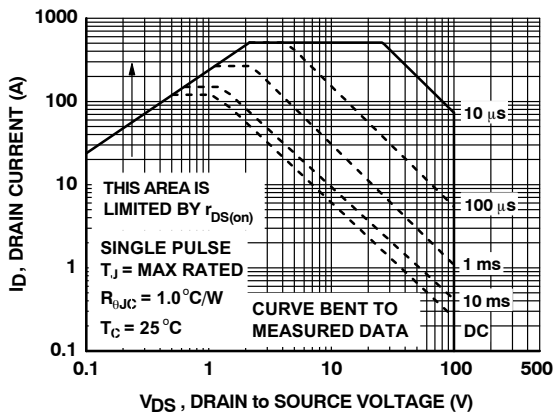


Figure 11. Forward Bias Safe Operating Area

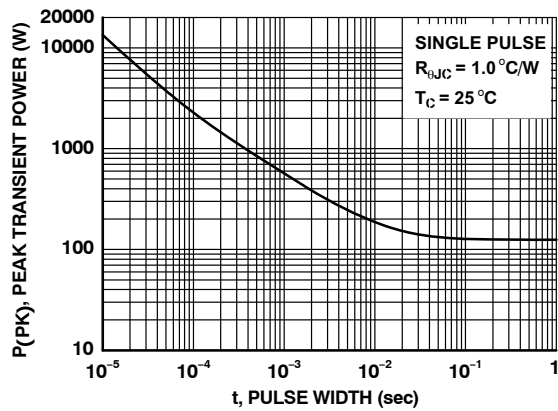


Figure 12. Single Pulse Maximum Power Dissipation

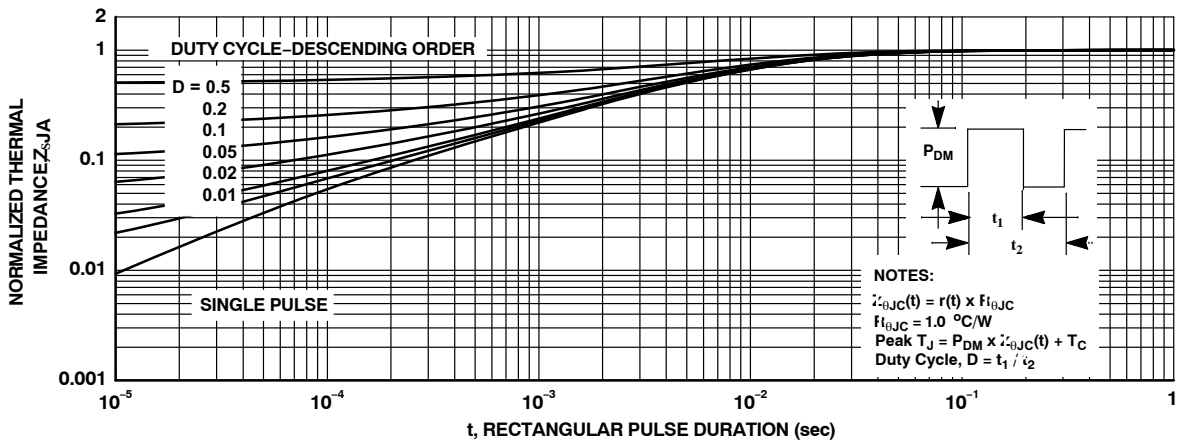
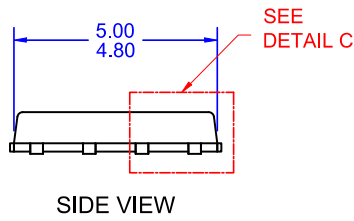
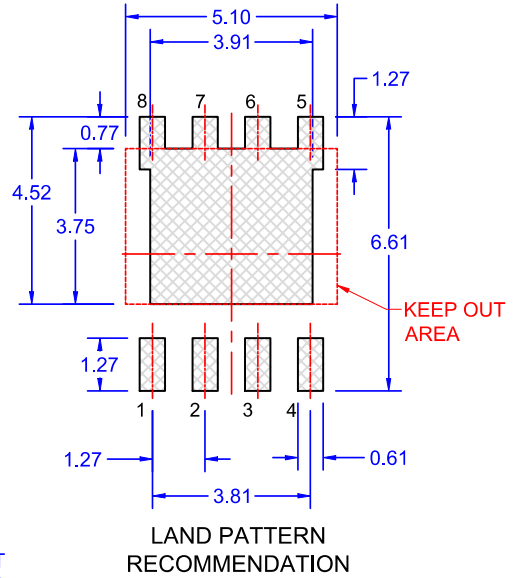
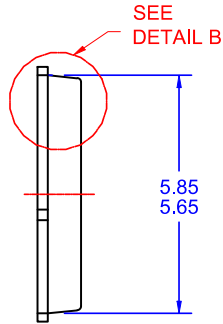
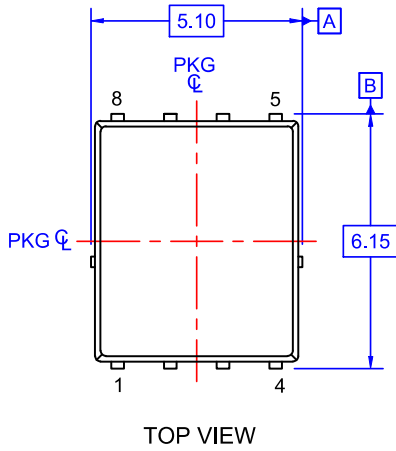


Figure 13. Transient Thermal Response Curve

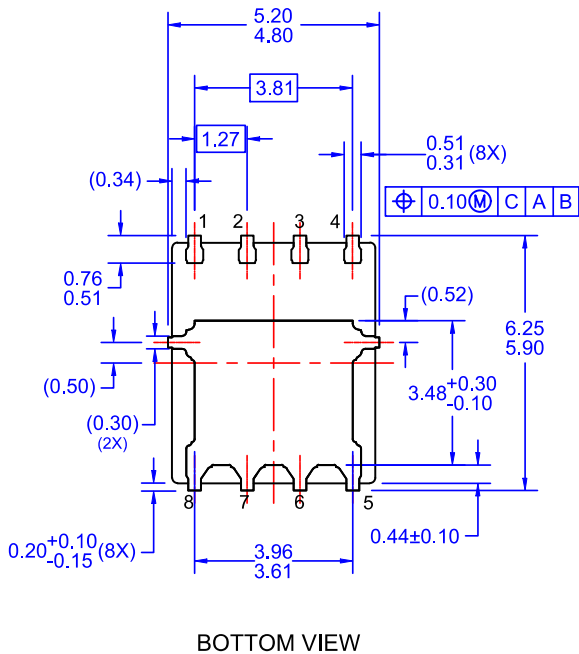
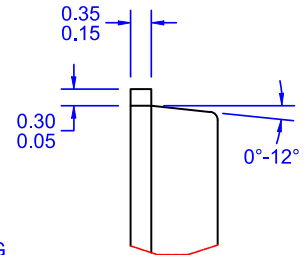
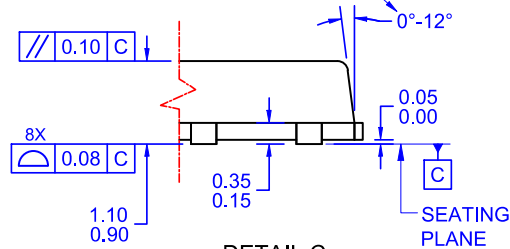
# FDMS86181E

## PACKAGE DIMENSIONS

PQFN8 5X6, 1.27P  
CASE 483AE  
ISSUE A




OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA..
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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