ESD Protection Diode
Ultra−Low Capacitance
ESDR0502B, SZESDR0502B

The ESDR0502B is designed to protect voltage sensitive components from damage due to ESD in applications that require ultra low capacitance to preserve signal integrity. Excellent clamping capability, low leakage and fast response time are combined with an ultra low diode capacitance of 0.5 pF to provide best in class protection from IC damage due to ESD. The small SC−75 package is ideal for designs where board space is at a premium. The ESDR0502B can be used to protect two uni−directional lines or one bi−directional line. When used to protect one bi−directional line, the effective capacitance is 0.25 pF. Because of its low capacitance, it is well suited for protecting high frequency signal lines such as USB2.0 high speed and antenna line applications.

Specification Features:

- Low Capacitance 0.5 pF Typical
- Low Clamping Voltage, Low Leakage
- Small Body Outline Dimensions:
  0.063” x 0.063” (1.60 mm x 1.60 mm)
- Stand−off Voltage: 5 V
- Response Time is Typically < 1.0 ns
- IEC61000−4−2 Level 4 ESD Protection
  ISO10605 330 pF/2 kΩ ±17 kV (Contact)
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- This is a Pb−Free Device

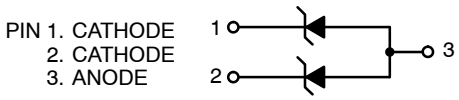
Mechanical Characteristics:

CASE: Void-free, transfer-molded, thermosetting plastic
Epoxy Meets UL 94 V−0
LEAD FINISH: 100% Matte Sn (Tin)
MOUNTING POSITION: Any
QUALIFIED MAX REFLOW TEMPERATURE: 260°C
Device Meets MSL 1 Requirements

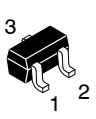
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IEC 61000−4−2 Contact (ESD) IEC 61000−4−2 Air (ESD)	ESD	±11 ±15	kV
Peak Surge Power (8 x 20 μs)	P_{pk}	20	W
Peak Surge Current (8 x 20 μs)	I_{pp}	2.0	A
Total Power Dissipation on FR−5 Board (Note 1) @ T_A = 25°C	P_D	150	mW
Storage Temperature Range	T_{stg}	−55 to +150	°C
Junction Temperature Range	T_J	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Second Duration)	T_L	260	°C

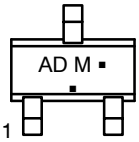
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. FR−5 = 1.0 x 0.75 x 0.62 in.



MARKING DIAGRAM



SC−75
CASE 463
STYLE 4



AD = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
ESDR0502BT1G	SC−75 (Pb−Free)	3000/Tape & Reel
SZESDR0502BT1G	SC−75 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

See Application Note AND8308/D for further description of survivability specs.

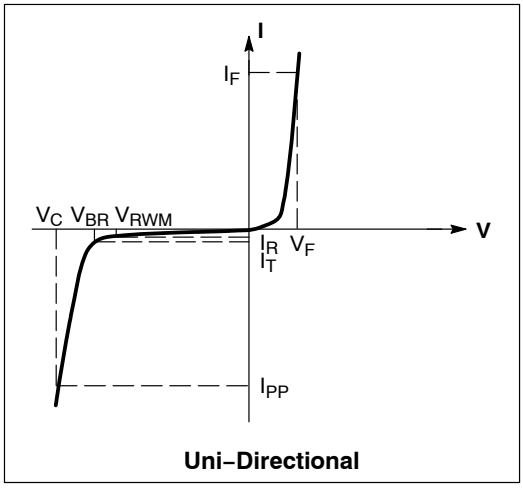
DEVICE MARKING INFORMATION

See specific marking information in the device marking column of the Electrical Characteristics tables starting on page 2 of this data sheet.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Capacitance @ V_R = 0 and f = 1.0 MHz



Uni−Directional

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, V_F = 1.1 V Max. @ I_F = 10 mA for all types)

Device*	Device Marking	V_{RWM} (V) Max	I_R (μA) @ V_{RWM} Max	V_{BR} (V) @ I_T (Note 2) Min	I_T mA	C (pF), uni−directional (Note 3) Typ	C (pF), uni−directional (Note 3) Max	C (pF), bi−directional (Note 4) Typ	C (pF), bi−directional (Note 4) Max	V_C (V) @ I_{PP} = 1 A (Note 5) Max	V_C Per IEC61000−4−2 (Note 6)
ESDR0502B	AD	5.0	1.0	5.8	1.0	0.5	0.9	0.25	0.45	15	Figures 1 and 2

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*Include SZ−prefix devices where applicable.

2. V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C.
3. Uni−directional capacitance at f = 1 MHz, V_R = 0 V, T_A = 25°C (pin1 to pin 3; pin 2 to pin 3).
4. Bi−directional capacitance at f = 1 MHz, V_R = 0 V, T_A = 25°C (pin1 to pin 2).
5. Surge current waveform per Figure 5.
6. Typical waveform. For test procedure see Figures 3 and 4 and Application Note AND8307/D.

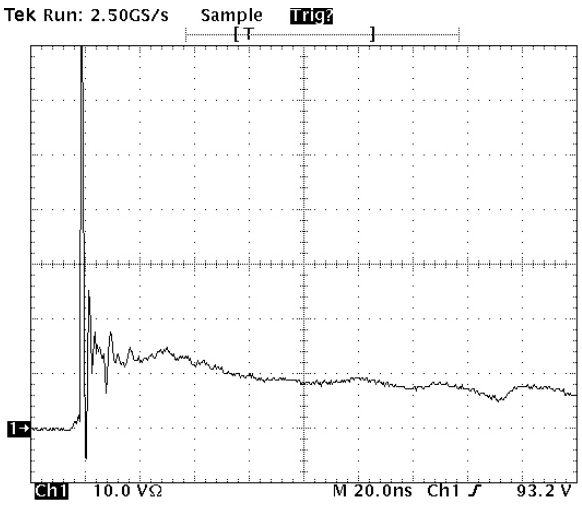


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV contact per IEC 61000−4−2

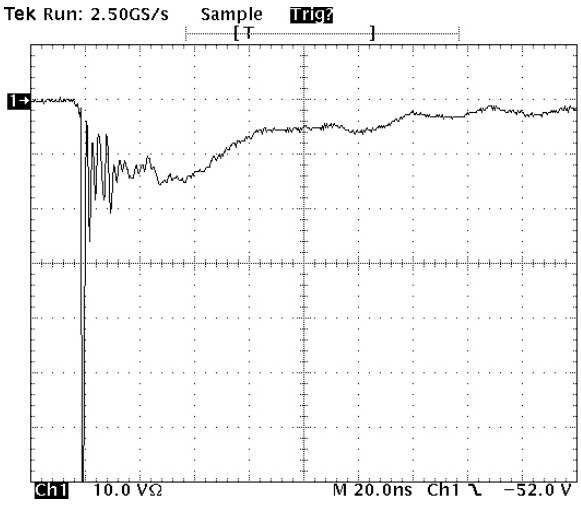


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV contact per IEC 61000−4−2

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

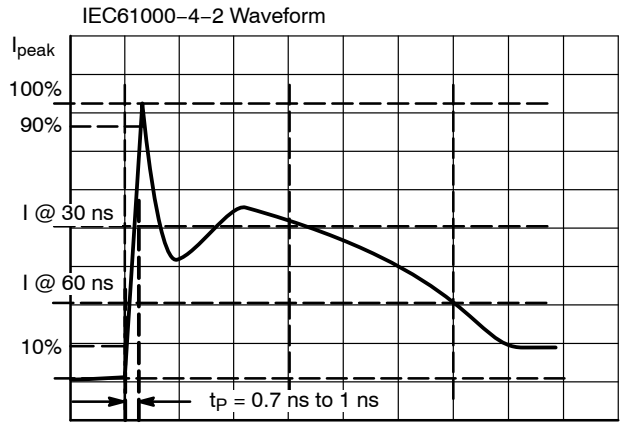


Figure 3. IEC61000−4−2 Spec

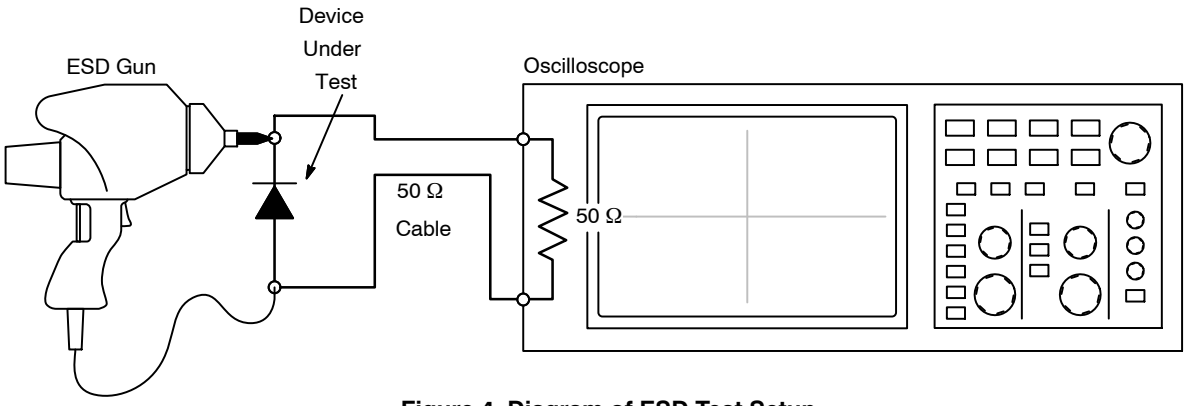


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. **onsemi** has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how **onsemi** creates these screenshots and how to interpret them please refer to AND8307/D.

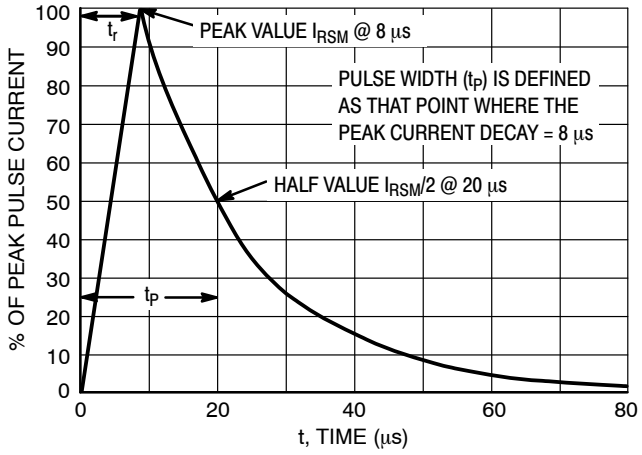
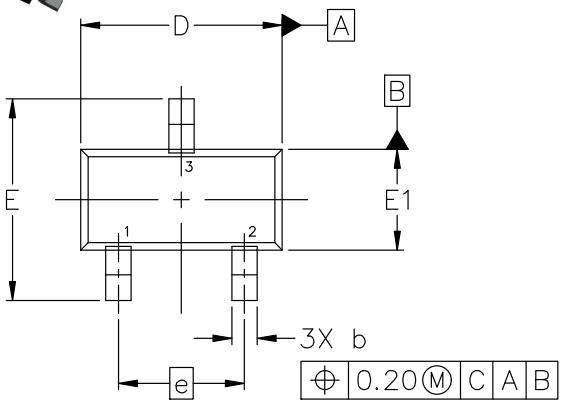


Figure 5. 8 x 20 μs Pulse Waveform

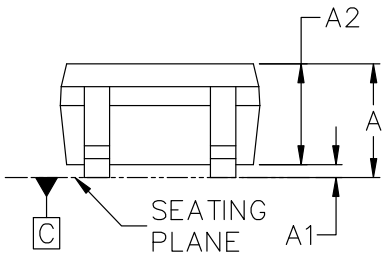
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SC75−3 1.60x0.80x0.80, 1.00P
CASE 463
ISSUE H

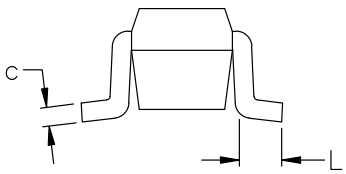
DATE 01 FEB 2024



TOP VIEW



SIDE VIEW



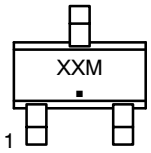
END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.

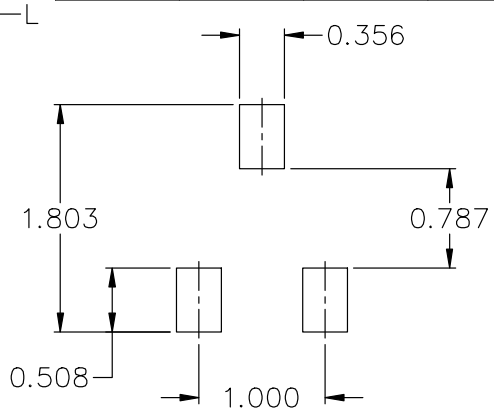
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.80	0.90
A1	0.00	0.05	0.10
A2		0.80 REF.	
b	0.15	0.20	0.30
c	0.10	0.15	0.25
D	1.55	1.60	1.65
E	1.50	1.60	1.70
E1	0.70	0.80	0.90
e		1.00 BSC	
L	0.10	0.15	0.20

GENERIC
MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. GATE
2. SOURCE
3. DRAIN

DOCUMENT NUMBER:	98ASB15184C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SC75−3 1.60x0.80x0.80, 1.00P	PAGE 1 OF 1

ADDITIONAL INFORMATION

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Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales