

MOSFET – Power, N-Channel, Dual EFCP

12 V, 6 A, 29.5 m Ω

EFC4627R

Features

- 2.5 V Drive
- Protection Diode In
- Common-Drain Type
- This Device is Pb–Free, Halogen Free/BFR Free and is RoHS Compliant

Applications

• Lithium-ion Battery Charging and Discharging Switch

Specifications

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Conditions	Value	Unit
Source to Source Voltage	V _{SSS}		12	V
Gate to Source Voltage	V _{GSS}		±10	V
Source Current (DC)	I _S		6	Α
Source Current (Pulse)	I _{SP}	PW ≤ 10 μs, Duty Cycle ≤1%	60	Α
Total Dissipation	P _T	When mounted on ceramic substrate (5000 mm² x 0.8 mm)	1.4	W
Junction Temperature	TJ		150	°C
Storage Temperature	T _{stg}		– 55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction to Ambient When mounted on ceramic substrate (5000 mm ² x 0.8 mm)	$R_{\theta JA}$	84	٧



CSP4 1.01x1.01 CASE 568AK

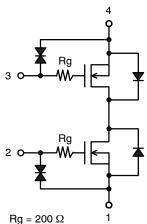
MARKING DIAGRAM



C = Specific Device CodeY = Year of Production

M = Assembly Operation MonthZZ = Assembly Lot Number

ELECTRICAL CONNECTION



ORDERING INFORMATION

Device	Package	Shipping [†]
EFC4627R-TR	CSP4 (Pb-Free and Halogen Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Parameter	Symbol	Conditions		Min	Тур	Max	Unit
Source to Source Breakdown Voltage	V _{(BR)SSS}	I _S = 1 mA, V _{GS} = 0 V	Test Circuit 1	12	-	_	V
Zero-Gate Voltage Source Current	I _{SSS}	V _{SS} = 10 V, V _{GS} = 0 V	Test Circuit 1	-	-	1	μΑ
Gate to Source Leakage Current	I _{GSS}	$V_{GS} = \pm 8 \text{ V}, V_{SS} = 0 \text{ V}$	Test Circuit 2	-	-	±1	μΑ
Gate Threshold Voltage	V _{GS} (th)	V _{SS} = 6 V, I _S = 1 mA	Test Circuit 3	0.5	-	1.3	V
Forward Transconductance	9 _{FS}	V _{SS} = 6 V, I _S = 2 A	Test Circuit 4	-	4.8	_	S
Static Source to Source On–State Resistance	R _{SS} (on)1	I _S = 2 A, V _{GS} = 4.5 V	Test Circuit 5	18.5	23.9	29.5	mΩ
	R _{SS} (on)2	I _S = 2 A, V _{GS} = 4.0 V	Test Circuit 5	19.7	25.4	31.3	mΩ
	R _{SS} (on)3	I _S = 2 A, V _{GS} = 3.8 V	Test Circuit 5	20.3	26.1	32.3	mΩ
	R _{SS} (on)4	I _S = 2 A, V _{GS} = 3.1 V	Test Circuit 5	23.5	30.3	39.0	mΩ
	R _{SS} (on)5	I _S = 2 A, V _{GS} = 2.5 V	Test Circuit 5	29.3	37.7	50.5	mΩ
Turn-On Delay Time	t _d (on)	$V_{SS} = 6 \text{ V}, V_{GS} = 4.5 \text{ V},$	Test Circuit 6	-	75	_	ns
Rise Time	t _r	I _S = 2 A		-	740	_	ns
Turn-Off Delay Time	t _d (off)			-	2340	_	ns
Fall Time	t _f			-	2320	_	ns
Total Gate Charge	Qg	V _{SS} = 6 V, V _{GS} = 4.5 V, I _S = 6 A	Test Circuit 7	-	13.4	-	nC
Forward Source to Source Voltage	V _{F(S-S)}	I _S = 3 A, V _{GS} = 0 V	Test Circuit 8	-	0.76	_	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Test Circuits are Example of Measuring FET1 Side.

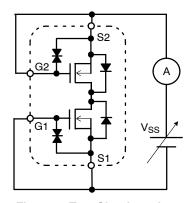
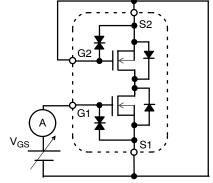


Figure 1. Test Circuit 1 - I_{SSS}



When FET1 is measured, Gate and Source of FET2 are short-circuited.

Figure 2. Test Circuit 2 - I_{GSS}

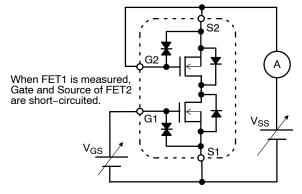


Figure 3. Test Circuit 3 - V_{GS}(th)

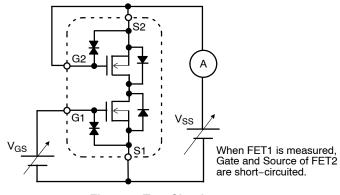
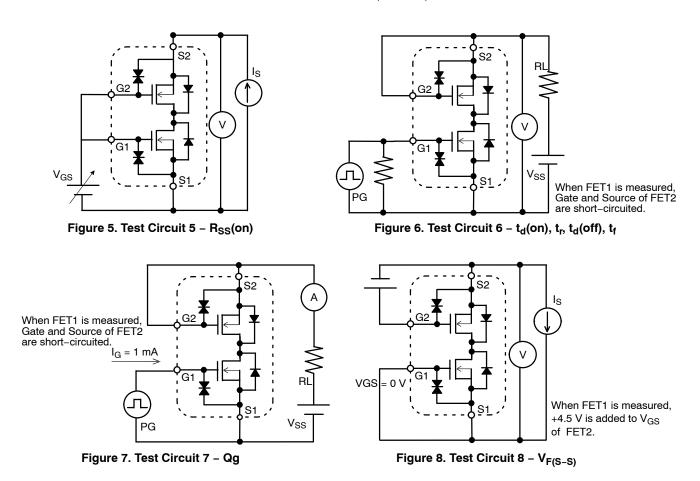


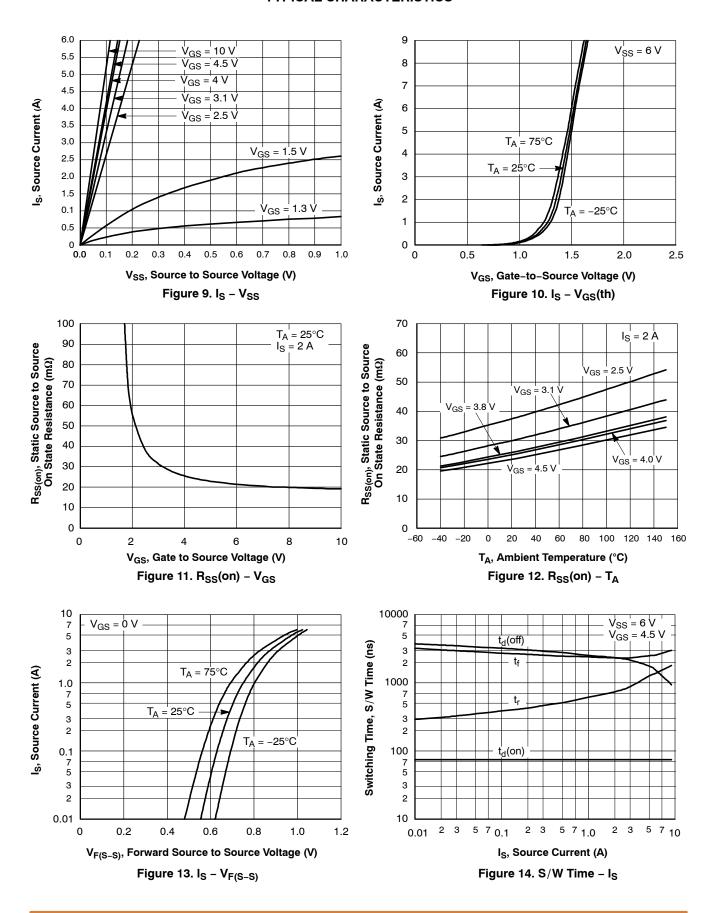
Figure 4. Test Circuit 4 - g_{FS}

TEST CIRCUITS (continued)

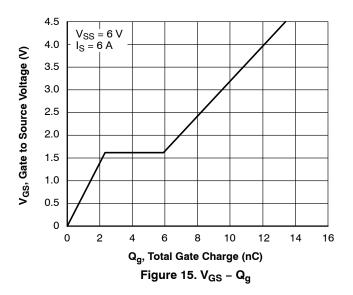


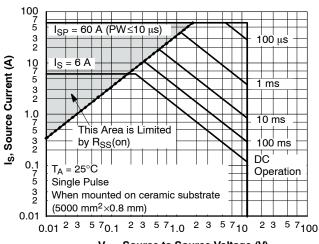
NOTE: When FET2 is measured, the position of FET1 and FET2 is switched.

TYPICAL CHARACTERISTICS

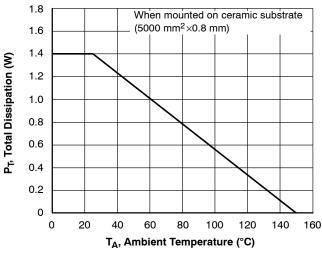


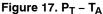
TYPICAL CHARACTERISTICS (continued)





 V_{SS} , Source to Source Voltage (V) Figure 16. SOA





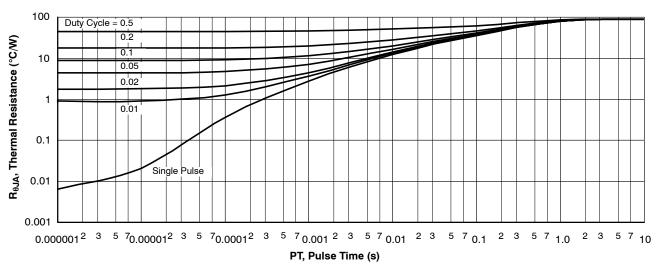


Figure 18. $R_{\theta JA}$ – Pulse Time

PACKAGE DIMENSION

EFC4627R-TR (Unit: mm)

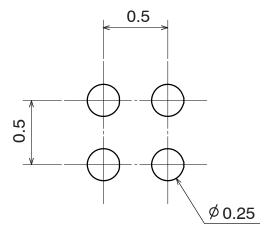


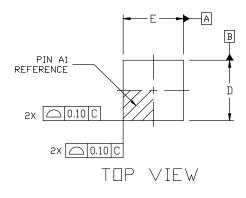
Figure 19. Recommended Soldering Footprint

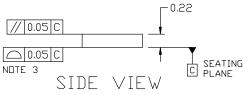


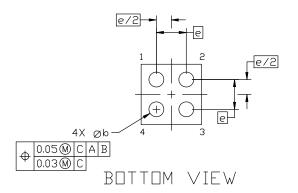


WLCSP4, 1.01x1.01x0.22, 0.50P CASE 568AK ISSUE B

DATE 14 NOV 2023



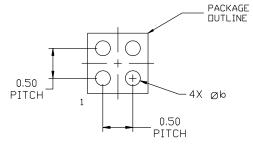




NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
- P. CONTROLLING DIMENSION: MILLIMETERS
- 3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

	MILLIMETERS					
DIM	MILLIME LEKS					
	MIN.	N□M.	MAX.			
Α			0.22			
b	0.22	0.25	0.28			
D	0.99	1.01	0.11			
E	0.99	1.01	0.11			
е		0.50 BS0				



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCES MANUAL, SOLDERRM/D.

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