Complementary Bias Resistor Transistors R1 = 22 k Ω , R2 = 47 k Ω

NPN and PNP Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable*
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

 $(T_A = 25^{\circ}C \text{ both polarities } Q_1 (PNP) \& Q_2 (NPN), unless otherwise noted)$

Rating	Symbol	Max	Unit
Collector-Base Voltage	V _{CBO}	50	Vdc
Collector-Emitter Voltage	V _{CEO}	50	Vdc
Collector Current – Continuous	Ι _C	100	mAdc
Input Forward Voltage	V _{IN(fwd)}	40	Vdc
Input Reverse Voltage	V _{IN(rev)}	7	Vdc

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

Device	Package	Shipping [†]
MUN5334DW1T1G, NSVMUN5334DW1T1G*	SOT-363	3,000/Tape & Reel
NSBC124XPDXV6T1G, NSVBC124XPDXV6T1G*	SOT-563	4,000/Tape & Reel

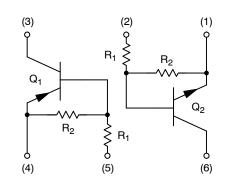
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



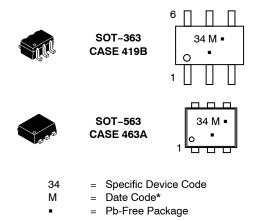
ON Semiconductor®

www.onsemi.com

PIN CONNECTIONS



MARKING DIAGRAMS



(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

THERMAL CHARACTERISTICS

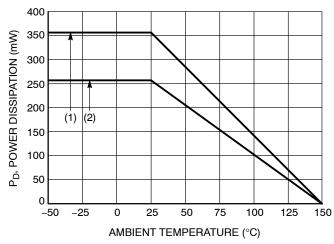
	Characteristic	Symbol	Max	Unit		
MUN5334DW1 (SOT-363) ONE JUNCTION HEATED						
$\begin{array}{l} \mbox{Total Device Dissipation} \\ T_A = 25^\circ C \qquad (Note 1) \\ (Note 2) \\ \mbox{Derate above } 25^\circ C \qquad (\\ (Note 2) \end{array}$	Note 1)	PD	187 256 1.5 2.0	mW mW/°C		
	Note 1) Note 2)	$R_{ ext{ heta}JA}$	670 490	°C/W		
MUN5334DW1 (SOT-363) BOT	H JUNCTION HEATED (Note 3)					
$\begin{array}{l} \mbox{Total Device Dissipation} \\ T_A = 25^\circ C \qquad (Note 1) \\ (Note 2) \\ \mbox{Derate above } 25^\circ C \qquad (\\ (Note 2) \end{array}$	Note 1)	PD	250 385 2.0 3.0	mW mW/°C		
Thermal Resistance, Junction to Ambient ((Note 2)	Note 1)	R _{θJA}	493 325	°C/W		
Thermal Resistance, Junction to Lead (Note 1) (Note 2)		R _{θJL}	188 208	°C/W		
Junction and Storage Temperat	ure Range	T _J , T _{stg}	-55 to +150	°C		
NSBC124XPDXV6 (SOT-563) (ONE JUNCTION HEATED					
$ Total Device Dissipation \\ T_A = 25^\circ C \qquad (Note 1) \\ Derate above 25^\circ C \qquad ($	Note 1)	PD	357 2.9	mW mW/°C		
Thermal Resistance, Junction to Ambient (Note 1)	$R_{ ext{ heta}JA}$	350	°C/W		
NSBC124XPDXV6 (SOT-563) E	SOTH JUNCTION HEATED (Note 3)					
$ Total Device Dissipation \\ T_A = 25^\circ C \qquad (Note 1) \\ Derate above 25^\circ C \qquad ($	Note 1)	P _D	500 4.0	mW mW/°C		
Thermal Resistance, Junction to Ambient (Note 1)	R _{θJA}	250	°C/W		
Junction and Storage Temperat	ure Range	T _J , T _{stg}	-55 to +150	°C		

FR-4 @ Minimum Pad.
 FR-4 @ 1.0 × 1.0 Inch Pad.
 Both junction heated values assume total power is sum of two equally powered channels.

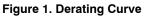
ELECTRICAL CHARACTERISTICS	$(T_A = 25^{\circ}C \text{ both polarities } Q_1 \text{ (PNP) } \& C$	Q_2 (NPN), unless otherwise noted)
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Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS				•	
Collector-Base Cutoff Current $(V_{CB} = 50 \text{ V}, I_E = 0)$	I _{CBO}	-	_	100	nAdc
Collector-Emitter Cutoff Current $(V_{CE} = 50 \text{ V}, I_B = 0)$	I _{CEO}	-	_	500	nAdc
Emitter-Base Cutoff Current $(V_{EB} = 6.0 \text{ V}, I_C = 0)$	I _{EBO}	-	_	0.13	mAdc
Collector-Base Breakdown Voltage $(I_C = 10 \ \mu A, I_E = 0)$	V _{(BR)CBO}	50	-	-	Vdc
Collector-Emitter Breakdown Voltage (Note 4) $(I_{C} = 2.0 \text{ mA}, I_{B} = 0)$	V _{(BR)CEO}	50	_	_	Vdc
ON CHARACTERISTICS					
DC Current Gain (Note 4) ($I_C = 5.0 \text{ mA}, V_{CE} = 10 \text{ V}$)	h _{FE}	80	150	_	
Collector-Emitter Saturation Voltage (Note 4) $(I_{C} = 10 \text{ mA}, I_{B} = 1.0 \text{ mA})$	V _{CE(sat)}	-	_	0.25	V
Input Voltage (Off) (V _{CE} = 5.0 V, I _C = 100 μ A) (NPN) (V _{CE} = 5.0 V, I _C = 100 μ A) (PNP)	V _{i(off)}	-	0.8 0.9		Vdc
Input Voltage (On) ($V_{CE} = 0.2 \text{ V}, I_C = 3.0 \text{ mA}$) (NPN) ($V_{CE} = 0.2 \text{ V}, I_C = 3.0 \text{ mA}$) (PNP)	V _{i(on)}	- -	1.3 1.3		Vdc
Output Voltage (On) (V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 k Ω)	V _{OL}	-	_	0.2	Vdc
Output Voltage (Off) (V _{CC} = 5.0 V, V _B = 0.5 V, R _L = 1.0 k Ω)	V _{OH}	4.9	_	-	Vdc
Input Resistor	R1	15.4	22	28.6	kΩ
Resistor Ratio	R ₁ /R ₂	0.38	0.47	0.56	

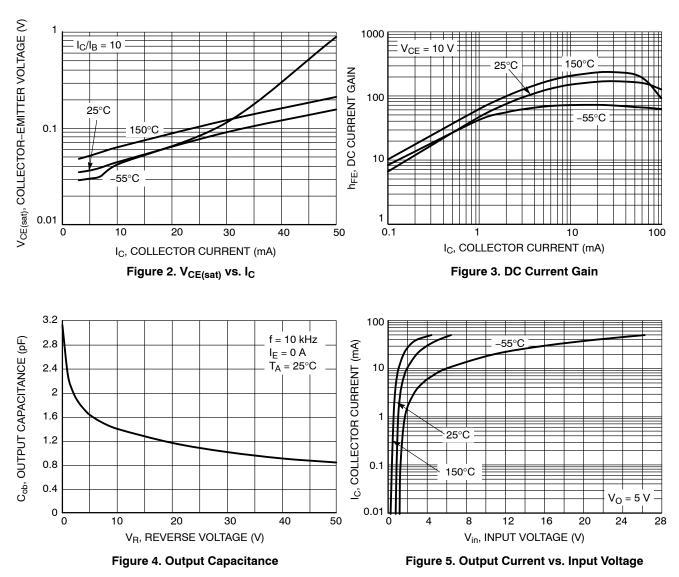
4. Pulsed Condition: Pulse Width = 300 ms, Duty Cycle $\leq 2\%$.

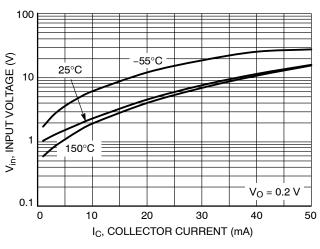


(1) SOT–363; 1.0 \times 1.0 Inch Pad (2) SOT–563; Minimum Pad



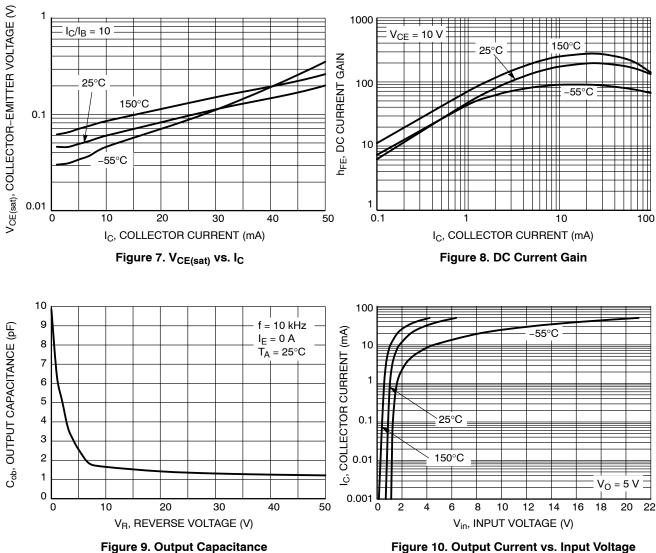


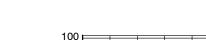




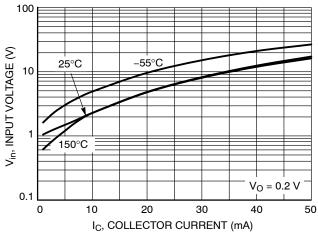








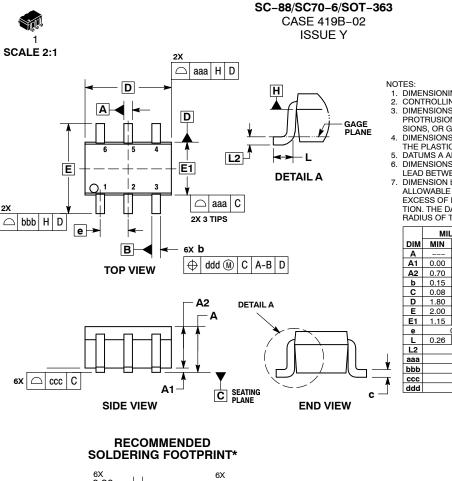






NSEM

DATE 11 DEC 2012



6X 0.30 0.66 2 50 0.65 PITCH DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 CONTROLLING DIMENSION MILLIMETERS
- CONTROLLING DIMENSION: MILLIMETERS. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH,
- PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRU-SIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END. SIONS, OH GATE BUHHS SHALL NOT EXCEED 0.20 PEH END. DIMENSIONS D AND ET AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H. DATUMS A AND B ARE DETERMINED AT DATUM H. DIMENSIONS 5 AND 6 APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION 6 AT MAXIMUM MATERIAL CONDI-TION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

	MILLIMETERS			INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
Α			1.10			0.043	
A1	0.00		0.10	0.000		0.004	
A2	0.70	0.90	1.00	0.027	0.035	0.039	
b	0.15	0.20	0.25	0.006	0.008	0.010	
С	0.08	0.15	0.22	0.003	0.006	0.009	
D	1.80	2.00	2.20	0.070	0.078	0.086	
Е	2.00	2.10	2.20	0.078	0.082	0.086	
E1	1.15	1.25	1.35	0.045	0.049	0.053	
е	(0.65 BS	С	0.026 BSC			
L	0.26	0.36	0.46	0.010	0.014	0.018	
L2	0.15 BSC			0.006 BSC			
aaa	0.15			0.006			
bbb	0.30			0.012			
ccc	0.10			0.004			
ddd	0.10			0.004			

GENERIC **MARKING DIAGRAM***



XXX = Specific Device Code

- Μ = Date Code*
- = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SC-88/SC70-6/SOT-363 CASE 419B-02 ISSUE Y

DATE 11 DEC 2012

STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 2: CANCELLED	STYLE 3: CANCELLED	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	STYLE 8: CANCELLED	STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
STYLE 13:	STYLE 14:	STYLE 15:	STYLE 16:	STYLE 17:	STYLE 18:
PIN 1. ANODE	PIN 1. VREF	PIN 1. ANODE 1	PIN 1. BASE 1	PIN 1. BASE 1	PIN 1. VIN1
2. N/C	2. GND	2. ANODE 2	2. EMITTER 2	2. EMITTER 1	2. VCC
3. COLLECTOR	3. GND	3. ANODE 3	3. COLLECTOR 2	3. COLLECTOR 2	3. VOUT2
4. EMITTER	4. IOUT	4. CATHODE 3	4. BASE 2	4. BASE 2	4. VIN2
5. BASE	5. VEN	5. CATHODE 2	5. EMITTER 1	5. EMITTER 2	5. GND
6. CATHODE	6. VCC	6. CATHODE 1	6. COLLECTOR 1	6. COLLECTOR 1	6. VOUT1
STYLE 19:	STYLE 20:	STYLE 21:	STYLE 22:	STYLE 23:	STYLE 24:
PIN 1. I OUT	PIN 1. COLLECTOR	PIN 1. ANODE 1	PIN 1. D1 (i)	PIN 1. Vn	PIN 1. CATHODE
2. GND	2. COLLECTOR	2. N/C	2. GND	2. CH1	2. ANODE
3. GND	3. BASE	3. ANODE 2	3. D2 (i)	3. Vp	3. CATHODE
4. V CC	4. EMITTER	4. CATHODE 2	4. D2 (c)	4. N/C	4. CATHODE
5. V EN	5. COLLECTOR	5. N/C	5. VBUS	5. CH2	5. CATHODE
6. V REF	6. COLLECTOR	6. CATHODE 1	6. D1 (c)	6. N/C	6. CATHODE
STYLE 25:	STYLE 26:	STYLE 27:	STYLE 28:	STYLE 29:	STYLE 30:
PIN 1. BASE 1	PIN 1. SOURCE 1	PIN 1. BASE 2	PIN 1. DRAIN	PIN 1. ANODE	PIN 1. SOURCE 1
2. CATHODE	2. GATE 1	2. BASE 1	2. DRAIN	2. ANODE	2. DRAIN 2
3. COLLECTOR 2	3. DRAIN 2	3. COLLECTOR 1	3. GATE	3. COLLECTOR	3. DRAIN 2
4. BASE 2	4. SOURCE 2	4. EMITTER 1	4. SOURCE	4. EMITTER	4. SOURCE 2
5. EMITTER	5. GATE 2	5. EMITTER 2	5. DRAIN	5. BASE/ANODE	5. GATE 1
6. COLLECTOR 1	6. DRAIN 1	6. COLLECTOR 2	6. DRAIN	6. CATHODE	6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



ONSEMI

DATE 15 FEB 2024 NTES 1.1 ENDESCONG AND TOLERANCING CONFORM TO ASME 1.2 ENDESCONG AND TOLERANCING CONFORMATION TOLERANCING 2. ENDESCONG AND TOLERANCING CONFORMATION TOLERANCING 2. ENDESCONG AND TOLERANCING CONFORMATION TOLERANCING 2. ENDESCONG AND TOLERANCING TOLERANCING TOLERANCING TOLERANCING 2. ENDESCONG AND TOLERANCING TOLERANCING TOLERANCING 2. ENDESCONG AND TOLERANCING TOLERANCING TOLERANCING TOLERANCING TOLERANCING TOLERANCING TOLERANCING 2. ENDESCONG AND TOLERANCING TOLERANCING 2. ENDESCONG AND TOLERANCING TOLERANCING TOLERANCING TOLERANCI				ISSUE J				
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PIN 1 FIN 1 <th< th=""><th>-</th><th>D</th><th>A -</th><th> - − 6X </th><th>DIM</th><th>М</th><th>ILLIMETE</th><th>RS</th></th<>	-	D	A -	 - − 6X	DIM	М	ILLIMETE	RS
PIN 1 0 <th></th> <th>B</th> <th></th> <th></th> <th></th> <th>MIN.</th> <th>NDM.</th> <th>MAX.</th>		B				MIN.	NDM.	MAX.
PIN 1 Image: Construction of the second schedule schedule of the second schedule of the sec					А	0.50	0.55	0.60
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SOT-563-6 1.60x1.20x0.55, 0.50P CASE 463A

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