Dual PNP Bias Resistor Transistors R1 = 10 k\Omega, R2 = \infty k\Omega

PNP Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

 $(T_A = 25^{\circ}C, \text{ common for } Q_1 \text{ and } Q_2, \text{ unless otherwise noted})$

Rating	Symbol	Max	Unit
Collector-Base Voltage	V _{CBO}	50	Vdc
Collector-Emitter Voltage	V _{CEO}	50	Vdc
Collector Current – Continuous	Ι _C	100	mAdc
Input Forward Voltage	V _{IN(fwd)}	40	Vdc
Input Reverse Voltage	V _{IN(rev)}	5	Vdc

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

Device	Package	Shipping [†]
MUN5115DW1T1G, SMUN5115DW1T1G	SOT-363	3,000/Tape & Reel
NSBA114TDXV6T1G	SOT-563	4,000/Tape & Reel
NSBA114TDXV6T5G	SOT-563	8,000/Tape & Reel
NSBA114TDP6T5G	SOT-963	8,000/Tape & Reel

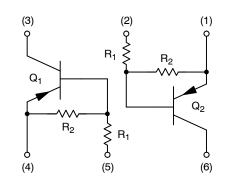
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



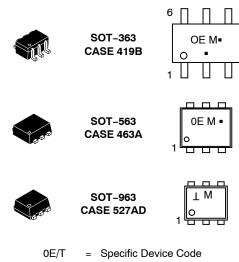
ON Semiconductor®

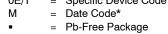
www.onsemi.com

PIN CONNECTIONS



MARKING DIAGRAMS





(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

THERMAL CHARACTERISTICS

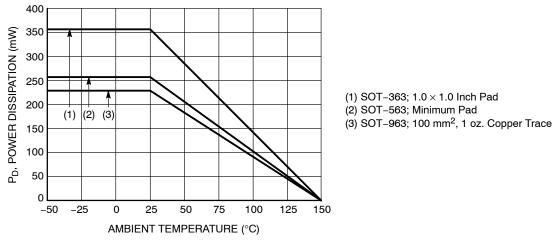
	Characteristic	Symbol	Max	Unit
MUN5115DW1 (SOT-363) ON	E JUNCTION HEATED			
Total Device Dissipation $T_A = 25^{\circ}C$ (Note 1) (Note 2) Derate above 25^{C} (Note 2)	(Note 1)	PD	187 256 1.5 2.0	mW mW/°C
Thermal Resistance, Junction to Ambient	(Note 1) (Note 2)	$R_{ heta JA}$	670 490	°C/W
MUN5115DW1 (SOT-363) BO	TH JUNCTION HEATED (Note 3)			
Total Device Dissipation $T_A = 25^{\circ}C$ (Note 1) (Note 2) Derate above 25^{C} (Note 2)	(Note 1)	PD	250 385 2.0 3.0	mW mW/°C
Thermal Resistance, Junction to Ambient (Note 2)	(Note 1)	R _{θJA}	493 325	°C/W
Thermal Resistance, Junction to Lead (Note 1) (Note 2)		R _{θJL}	188 208	°C/W
Junction and Storage Temperation	ature Range	T _J , T _{stg}	-55 to +150	°C
NSBA114TDXV6 (SOT-563) C	ONE JUNCTION HEATED			
$\begin{array}{l} \mbox{Total Device Dissipation} \\ T_A = 25^\circ C \qquad (Note 1) \\ \mbox{Derate above } 25^\circ C \end{array}$	(Note 1)	PD	357 2.9	mW mW/°C
Thermal Resistance, Junction to Ambient	(Note 1)	R _{θJA}	350	°C/W
NSBA114TDXV6 (SOT-563) E	BOTH JUNCTION HEATED (Note 3)		· · · ·	
$\begin{array}{l} \mbox{Total Device Dissipation} \\ T_A = 25^\circ C & (Note 1) \\ \mbox{Derate above } 25^\circ C \end{array}$	(Note 1)	PD	500 4.0	mW mW/°C
Thermal Resistance, Junction to Ambient	(Note 1)	R _{θJA}	250	°C/W
Junction and Storage Tempera	ature Range	T _J , T _{stg}	-55 to +150	°C
NSBA114TDP6 (SOT-963) Of	IE JUNCTION HEATED			
Total Device Dissipation $T_A = 25^{\circ}C$ (Note 4) (Note 5) Derate above 25^{C} (Note 5)	(Note 4)	PD	231 269 1.9 2.2	MW mW/°C
Thermal Resistance, Junction to Ambient (Note 5)	(Note 4)	R _{θJA}	540 464	°C/W
NSBA114TDP6 (SOT-963) BC	OTH JUNCTION HEATED (Note 3)		· · · ·	
$\begin{array}{l} \mbox{Total Device Dissipation} \\ T_A = 25^\circ C \qquad (Note 4) \\ (Note 5) \\ \mbox{Derate above } 25^\circ C \\ (Note 5) \end{array}$	(Note 4)	PD	339 408 2.7 3.3	MW mW/°C
Thermal Resistance, Junction to Ambient (Note 5)	(Note 4)	R _{θJA}	369 306	°C/W
Junction and Storage Temperation	atura Danas	T _J , T _{stg}	-55 to +150	°C

FR-4 @ 1.0 × 1.0 Inch Pad.
 FR-4 @ 1.0 × 1.0 Inch Pad.
 Both junction heated values assume total power is sum of two equally powered channels.
 FR-4 @ 100 mm², 1 oz. copper traces, still air.
 FR-4 @ 500 mm², 1 oz. copper traces, still air.

ELECTRICAL CHARACTERISTICS (T _A = 25°	C, common for Q ₁ and Q ₂ , unless otherwise noted)
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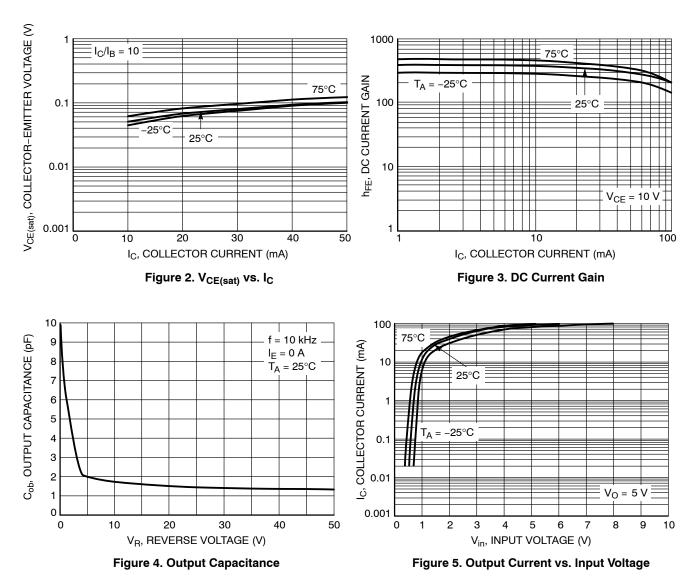
Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Cutoff Current $(V_{CB} = 50 \text{ V}, I_E = 0)$	I _{СВО}	_	_	100	nAdc
Collector-Emitter Cutoff Current $(V_{CE} = 50 \text{ V}, I_B = 0)$	I _{CEO}	-	-	500	nAdc
Emitter-Base Cutoff Current $(V_{EB} = 6.0 \text{ V}, I_C = 0)$	I _{EBO}	-	-	0.9	mAdc
Collector-Base Breakdown Voltage $(I_C = 10 \ \mu A, I_E = 0)$	V _{(BR)CBO}	50	_	-	Vdc
Collector-Emitter Breakdown Voltage (Note 6) $(I_{C} = 2.0 \text{ mA}, I_{B} = 0)$	V _{(BR)CEO}	50	-	-	Vdc
ON CHARACTERISTICS					
DC Current Gain (Note 6) $(I_C = 5.0 \text{ mA}, V_{CE} = 10 \text{ V})$	h _{FE}	160	250	-	
Collector-Emitter Saturation Voltage (Note 6) $(I_{C} = 10 \text{ mA}, I_{B} = 0.3 \text{ mA})$	V _{CE(sat)}	-	-	0.25	V
Input Voltage (Off) (V _{CE} = 5.0 V, I _C = 100 μA)	V _{i(off)}	-	0.6	_	Vdc
Input Voltage (On) (V _{CE} = 0.2 V, I _C = 10 mA)	V _{i(on)}	-	1.4	_	Vdc
Output Voltage (On) (V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 k Ω)	V _{OL}	_	-	0.2	Vdc
Output Voltage (Off) (V _{CC} = 5.0 V, V _B = 0.25 V, R _L = 1.0 k Ω)	V _{OH}	4.9	-	_	Vdc
Input Resistor	R1	7.0	10	13	kΩ
Resistor Ratio	R ₁ /R ₂	-	-	-	

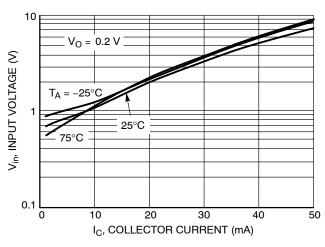
6. Pulsed Condition: Pulse Width = 300 ms, Duty Cycle \leq 2%.

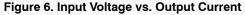


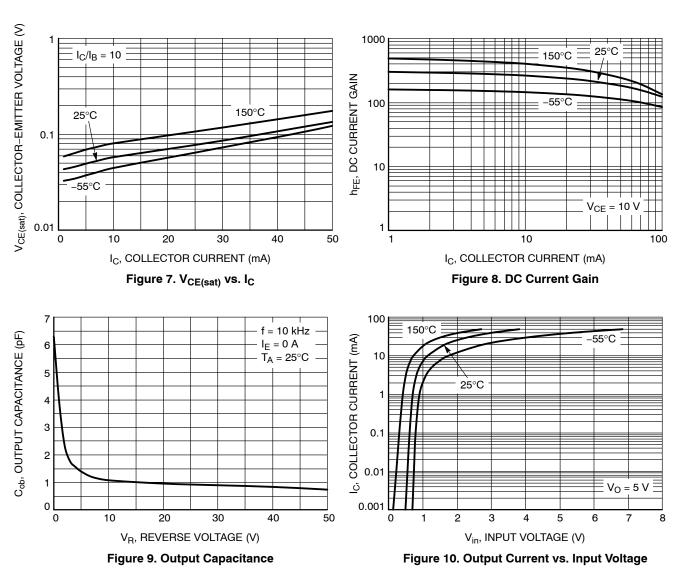


TYPICAL CHARACTERISTICS MUN5115DW1, NSBA114TDXV6

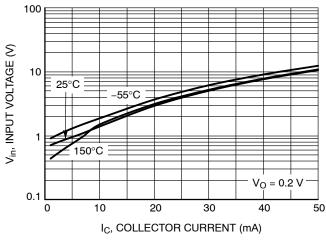










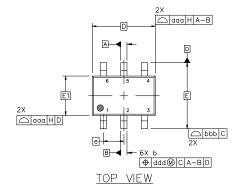




SC-88 2.00x1.25x0.90, 0.65P CASE 419B-02 **ISSUE Z**

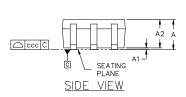
DATE 18 APR 2024

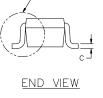
DUSEM



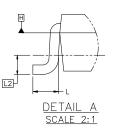
NOTES:

- DIMENSIONING AND TOLERANCING CONFORM TO ASME 1. Y14.5-2018.
- 2.
- ALL DIMENSION ARE IN MILLIMETERS. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 3. PER END.
- 4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF DATUMS A AND B ARE DETERMINED AT DATUM H.
- 5.
- DIMENSIONS & AND C APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP. 6.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. 7 ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION & AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

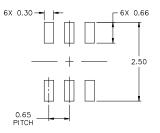




DETAIL A



	MI	LLIMETER	S		
DIM	MIN.	NOM.	MAX.		
A			1.10		
A1	0.00		0.10		
A2	0.70	0.90	1.00		
b	0.15	0.20	0.25		
с	0.08	0.15	0.22		
D	2.00 BSC				
E	2.10 BSC				
E1	1.25 BSC				
е		0.65 BSC)		
L	0.26	0.36	0.46		
L2		0.15 BSC			
aaa	0.15				
bbb	0.30				
ccc	0.10				
ddd		0.10			



RECOMMENDED MOUNTING FOOTPRINT*

FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

XXX = Specific Device Code = Date Code* Μ

GENERIC **MARKING DIAGRAM***

XXXM-

0

6

= Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DATE 18 APR 2024

STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 2: CANCELLED	STYLE 3: CANCELLED	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	STYLE 8: CANCELLED	STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
STYLE 13:	STYLE 14:	STYLE 15:	STYLE 16:	STYLE 17:	STYLE 18:
PIN 1. ANODE	PIN 1. VREF	PIN 1. ANODE 1	PIN 1. BASE 1	PIN 1. BASE 1	PIN 1. VIN1
2. N/C	2. GND	2. ANODE 2	2. EMITTER 2	2. EMITTER 1	2. VCC
3. COLLECTOR	3. GND	3. ANODE 3	3. COLLECTOR 2	3. COLLECTOR 2	3. VOUT2
4. EMITTER	4. IOUT	4. CATHODE 3	4. BASE 2	4. BASE 2	4. VIN2
5. BASE	5. VEN	5. CATHODE 2	5. EMITTER 1	5. EMITTER 2	5. GND
6. CATHODE	6. VCC	6. CATHODE 1	6. COLLECTOR 1	6. COLLECTOR 1	6. VOUT1
STYLE 19:	STYLE 20:	STYLE 21:	STYLE 22:	STYLE 23:	STYLE 24:
PIN 1. I OUT	PIN 1. COLLECTOR	PIN 1. ANODE 1	PIN 1. D1 (i)	PIN 1. Vn	PIN 1. CATHODE
2. GND	2. COLLECTOR	2. N/C	2. GND	2. CH1	2. ANODE
3. GND	3. BASE	3. ANODE 2	3. D2 (i)	3. Vp	3. CATHODE
4. V CC	4. EMITTER	4. CATHODE 2	4. D2 (c)	4. N/C	4. CATHODE
5. V EN	5. COLLECTOR	5. N/C	5. VBUS	5. CH2	5. CATHODE
6. V REF	6. COLLECTOR	6. CATHODE 1	6. D1 (c)	6. N/C	6. CATHODE
STYLE 25:	STYLE 26:	STYLE 27:	STYLE 28:	STYLE 29:	STYLE 30:
PIN 1. BASE 1	PIN 1. SOURCE 1	PIN 1. BASE 2	PIN 1. DRAIN	PIN 1. ANODE	PIN 1. SOURCE 1
2. CATHODE	2. GATE 1	2. BASE 1	2. DRAIN	2. ANODE	2. DRAIN 2
3. COLLECTOR 2	3. DRAIN 2	3. COLLECTOR 1	3. GATE	3. COLLECTOR	3. DRAIN 2
4. BASE 2	4. SOURCE 2	4. EMITTER 1	4. SOURCE	4. EMITTER	4. SOURCE 2
5. EMITTER	5. GATE 2	5. EMITTER 2	5. DRAIN	5. BASE/ANODE	5. GATE 1
6. COLLECTOR 1	6. DRAIN 1	6. COLLECTOR 2	6. DRAIN	6. CATHODE	6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



ONSEMI

DATE 15 FEB 2024 NTES 1.1 ENDESCONG AND TOLERANCING CONFORM TO ASME 1.2 ENDESCONG AND TOLERANCING CONFORMATION TOLERANCING 2. ENDESCONG AND TOLERANCING CONFORMATION TOLERANCING 2. ENDESCONG AND TOLERANCING CONFORMATION TOLERANCING 2. ENDESCONG AND TOLERANCING TOLERANCING TOLERANCING TOLERANCING 2. ENDESCONG AND TOLERANCING TOLERANCING TOLERANCING 2. ENDESCONG AND TOLERANCING TOLERANCING TOLERANCING TOLERANCING TOLERANCING TOLERANCING TOLERANCING 2. ENDESCONG AND TOLERANCING TOLERANCING 2. ENDESCONG AND TOLERANCING TOLERANCING TOLERANCING TOLERANCI				ISSUE J				
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THICKNESS MINIMUM LEAD THICKNESS IS THE MINIMUM HICKNESS OF BASE MATERIAL. THICKNESS OF BASE AND THE						MILLIMET	ERS.	
PIN 1 PIN 1 <td< th=""><th></th><th></th><th></th><th>THICKNESS</th><th>. MINIMUM LEA</th><th>AD THICK</th><th></th><th></th></td<>				THICKNESS	. MINIMUM LEA	AD THICK		
PIN 1 FIN 1 <th< th=""><th>-</th><th>D</th><th>A -</th><th> - − 6X </th><th>DIM</th><th>М</th><th>ILLIMETE</th><th>RS</th></th<>	-	D	A -	 - − 6X	DIM	М	ILLIMETE	RS
PIN 1 0 <th></th> <th>B</th> <th></th> <th></th> <th></th> <th>MIN.</th> <th>NDM.</th> <th>MAX.</th>		B				MIN.	NDM.	MAX.
PIN 1 Image: Construction of the second schedule schedule of the second schedule of the sec					А	0.50	0.55	0.60
C 0.08 0.13 0.18 D D 0.10 1.20 1.30 D D 0.10 0.20 0.30 PIN 1 EMTTRE 1 STYLE 3 FIVE 4 0.10 0.20 0.30 STYLE 1 PIN 1 EMTTRE 1 STYLE 3 AMDE 4 0.30 0.30 0.30 0.30 J AMDE 5 SASE 1 SAME 7 SAME 7 <th></th> <th>•</th> <th></th> <th></th> <th>b</th> <th>0.17</th> <th>0.22</th> <th>0.27</th>		•			b	0.17	0.22	0.27
STYLE I: TOP VIEW STYLE 3: TOP VIEW STYLE 3: SIDE VIEW D 1.50 1.60 1.70 STYLE I: TOP VIEW SIDE VIEW SIDE VIEW D 1.50 1.60 1.70 STYLE I: TOP VIEW SIDE VIEW SIDE VIEW D 1.50 1.60 1.70 STYLE I: TOP VIEW STYLE 3: SIDE VIEW SIDE VIEW D 1.50 1.60 1.70 STYLE I: TOP VIEW STYLE 3: SIDE VIEW SIDE VIEW D 1.50 1.60 1.70 STYLE 1: SIDE VIEW SIDE VIEW SIDE VIEW D 0.30	REFERENCE				C	80.0	0.13	0.18
STYLE 1: TOP_WEW SIDE_VIEW Image: Construct of the second se	الک ب				D	1.50	1.60	1.70
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DESCRIPTION: SOT-563-6 1.60x1.20x0.55, 0.50P PAGE 1 OF 1				Printed versions are un				COPY" in red.
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SOT-563-6 1.60x1.20x0.55, 0.50P CASE 463A

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SOT-963 1.00x1.00x0.37, CASE 527AD	0.35P			
ISSUE F			DATE	20 FEB 2024
NDTES:		м	LLIMETE	RS
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2. CONTROLLING DIMENSION: MILLIMETERS.	2018. DIM	MIN.	NDM.	MAX.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIM		0,34	0.37	0,40
THICKNESS OF BASE MATERIAL.	h	0.10	0.15	0.20
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. PROTRUSIONS, OR GATE BURRS.	с	0.07	0.12	0.17
	D	0.95	1.00	1.05
	E	0.75	0.80	0.85
	e		0.35 BSC	2
+-+-+ Ė ⊢ Ĥ	Н	0.95	1.00	1.05
	L		0.19 REF	-
$T \Pi P V I F W$	L2	0.05	0.10	0.15
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4. COLLECTOR 2 4. COLLECTOR 2 4. CATHODE 2 5. BASE 2 5. CATHODE 2 6. COLLECTOR 1 6. ANODE/ANODE 1				
STYLE 4: STYLE 5: STYLE 6:				
PIN 1. COLLECTOR PIN 1. CATHODE PIN 1. CATHODE 2. COLLECTOR 2. CATHODE 2. ANODE 3. BASE 3. ANODE 3. CATHODE	G	ENERIC		
4. EMITTER4. ANODE4. CATHODE5. COLLECTOR5. CATHODE5. CATHODE		NG DIAGF	RAM*	
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STYLE 10: PIN 1. CATHODE 1 2. N/C 3. CATHODE 2 4. ANODE 2 5. N/C 6. ANODE 1	*This information device data she Pb-Free indicate or may not be pr not follow the Ge	et for actua or, "G" or m esent. Som	l part marki crodot "∎", n e products n	ing. nay
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