Product Overview

NB3N853501E: Input Mux - 2:1, LVTTL / LVCMOS, 3.3 V, Fanout Buffer - 1:4 LVPECL

For complete documentation, see the data sheet

Product Description

The NB3N853501E is a low skew 3.3 V supply 2:1:4 clock distribution fanout buffer. An Input MUX selects one of two LVCMOS/LVTTL CLK lines by the CLK_SEL pin (HIGH for CLK1, LOW for CLK0) using LVCMOS/LVTTL levels. A CLK_EN pin can enable or disable the outputs synchronously to eliminate runt pulses using LVCMOS/LVTTL levels (HIGH to enable outputs, LOW to disable output).

Features

- Four differential LVPECL Outputs
- Operating range: VCC = 3.3 5% V(3.135 to 3.465 V)
- Two Selectable LVCMOS/LVTTL CLOCK Inputs
- Up to 266 MHz Clock Operation
- Output to Output Skew: 30 ps
- Device to Device Skew 250 ps (Max.)
- Propagation Delay 1.9 ns (Max.)
- Additive Phase Jitter, RMS: 0.023 ps (Typ)
- Industrial Temp. Range (40C to 85C)

Benefits

- Multiple copies of the Clock
- Ensures operation in the majority of designs

Applications

- Teleconmmunications
- Networking
- Computing Systems
- SONET/SDH

End Products

- LAN/WAN
- Enterprise Servers
- ATE
- Test and Measurement

Part Electrical Specifications

Product	Compliance	Status	Type	Channels	Input / Output Ratio	Input Level	Output Level	V_{CC} Typ (V)	t_{Jitter} RMS Typ (ps)	$t_{skew(o-o)}$ Max (ps)	t_{pd} Typ (ns)	t_R & t_F Max (ps)	f_{max} Clock Typ (MHz)	f_{max} Data Typ (Mbps)	Package Type
NB3N853501EDTG	Pb-free / Halide free	Active	Buffer	1	2:1:4	LVCMOS / LVTTL	LVPECL	3.3	0.062	30		700	266		TSSOP-20
NB3N853501EDTR2G	Pb-free / Halide free	Active	Buffer	1	2:1:4	LVCMOS / LVTTL	LVPECL	3.3	0.062	30		700	266		TSSOP-20

For more information please contact your local sales support at www.onsemi.com

Created on: 7/11/2015