# Product Overview

## NB3L8543S: 2.5 V/3.3 V Differential 2:1 MUX to 4 LVDS Clock Fanout Buffer Outputs with Clock Enable and Clock Select

**For complete documentation, see the data sheet**

## Product Description

The NB3L8543S is a high performance, low skew 1-to-4 LVDS Clock Fanout Buffer.
The NB3L8543S features a multiplexed input which can be driven by either a differential or single-ended input to allow for the distribution of a lower speed clock along with the high speed system clock.
The CLK_SEL pin will select the differential CLK and CLKb inputs when LOW (or left open and pulled LOW by the internal pull-down resistor). When CLK_SEL is HIGH, the differential PCLK and PCLKb inputs are selected.
The common clock enable pin, CLK_EN, is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse on the outputs during asynchronous assertion/deassertion of the clock enable pin. The internal flip flop is clocked on the falling edge of the input clock; therefore, all associated specification limits are referenced to the negative edge of the clock input.

## Features

- Four Differential LVDS Output Pairs
- Two Selectable Differential Clock Inputs
- CLK/CLKb Can Accept LVPECL, LVDS, HCSL, HSTL and SSTL
- PCLK/PCLK Can Accept LVPECL, LVDS, CML and SSTL
- Maximum Output Frequency: 650 MHz
- Additive Phase Jitter, RMS: 50 fs (typical)
- Output Skew: 40 ps (maximum)
- Part-to-part Skew: 200 ps (maximum)
- Propagation Delay: 1.9 ns (maximum)

## Applications

- Computing
- Telecom
- Backplanes

## End Products

- Routers
- Servers
- Switches

## Part Electrical Specifications

| Product | Compliance | Status | Type | Channels | Input / Output Ratio | Input Level | Output Level | $V_{CC}$ Typ (V) | $t_{JitterRMS}$ Typ (ps) | $t_{skew(o-o)}$ Max (ps) | $t_{pd}$ Typ (ns) | $t_R$ & $t_F$ Max (ps) | $f_{max}$ Clock Typ (MHz) | $f_{max}$ Data Typ (Mbps) | Package Type |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NB3L8543SDTG | Pb-free<br>Halide free | Active | Buffer | 1 | 2:1:4 | CML<br>HCSL<br>HSTL<br>LVDS<br>LVPECL<br>SSTL | LVDS | 2.5V, 3.3V | 0.05 | 40 | 1.4 | 500<br>550 | 500<br>650 | | TSSOP-20 |
| NB3L8543SDTR2G | Pb-free<br>Halide free | Active | Buffer | 1 | 2:1:4 | CML<br>HCSL<br>HSTL<br>LVDS<br>LVPECL<br>SSTL | LVDS | 2.5V, 3.3V | 0.05 | 40 | 1.4 | 500<br>550 | 500<br>650 | | TSSOP-20 |

**For more information please contact your local sales support at www.onsemi.com**

**Created on: 7/11/2015**