

# Field Effect Transistor - N-Channel, Enhancement Mode

## 2N7002K

### Features

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input / Output Leakage
- Ultra-Small Surface Mount Package
- ESD HBM = 2000 V (Typical: 3000 V) as per JESD22 A114 and ESD CDM = 2000 V as per JESD22 C101
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

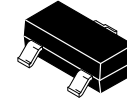
Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain-Source Voltage	60	V
$V_{DGR}$	Drain-Gate Voltage ( $R_{GS} \leq 1.0 \text{ M}\Omega$ )	60	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current	Continuous	300
		Pulsed	800
$T_J$	Operating Junction Temperature Range	-55 to +150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

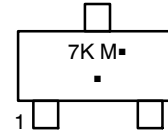
Symbol	Parameter	Value	Unit
$P_D$	Total Device Dissipation	350	mW
	Derate Above $T_A = 25^\circ\text{C}$	2.8	mW/ $^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	350	$^\circ\text{C}/\text{W}$

1. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch; Minimum land pad size.



SOT-23 (TO-236)  
CASE 318-08

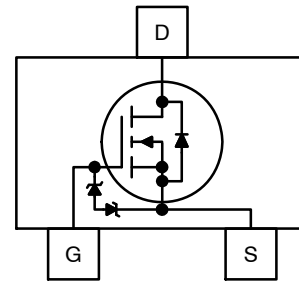
### MARKING DIAGRAM



- 7K = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)  
 \*Date Code orientation may vary depending upon manufacturing location.

### FUNCTIONAL SCHEMATIC



### ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

## 2N7002K

### ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Max	Unit
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#### OFF CHARACTERISTICS (Note 2)

BV <sub>DSS</sub>	Drain–Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 10 μA	60	–	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V	–	1.0	μA
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125°C	–	500	
I <sub>GSS</sub>	Gate–Body Leakage	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V	–	±10	μA

#### ON CHARACTERISTICS (Note 2)

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.0	2.5	V
R <sub>DS(ON)</sub>	Static Drain–Source On–Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.5 A	–	2	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 200 mA	–	4	
I <sub>D(ON)</sub>	On–State Drain Current	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 7.5 V	1.5	–	A
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 0.2 A	200	–	mS

#### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	–	50	pF
C <sub>oss</sub>	Output Capacitance		–	15	pF
C <sub>riss</sub>	Reverse Transfer Capacitance		–	6	pF

#### SWITCHING CHARACTERISTICS

t <sub>D(ON)</sub>	Turn–On Delay Time	V <sub>DD</sub> = 30 V, I <sub>DSS</sub> = 200 mA, R <sub>G</sub> = 10 Ω, V <sub>GS</sub> = 10 V	–	5	ns
t <sub>D(OFF)</sub>	Turn–Off Delay Time		–	30	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Short duration test pulse used to minimize self–heating effect.

TYPICAL PERFORMANCE CHARACTERISTICS

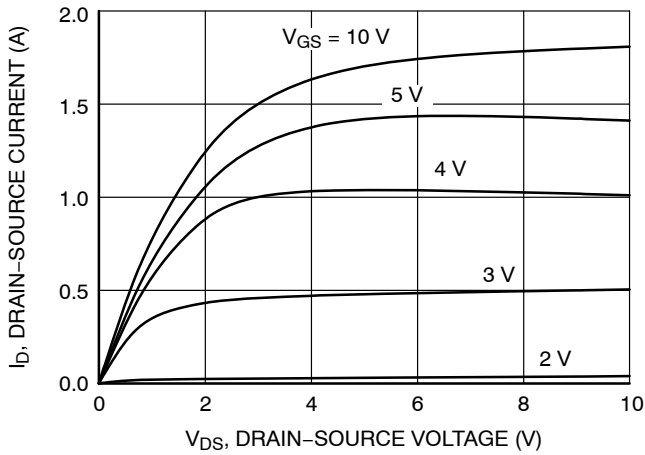


Figure 1. On-Region Characteristics

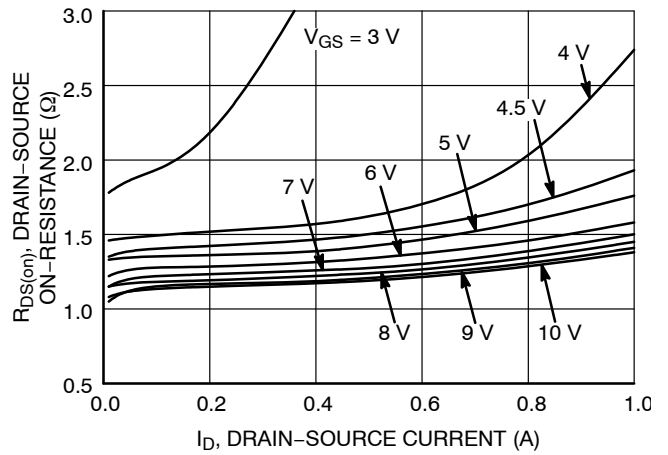


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

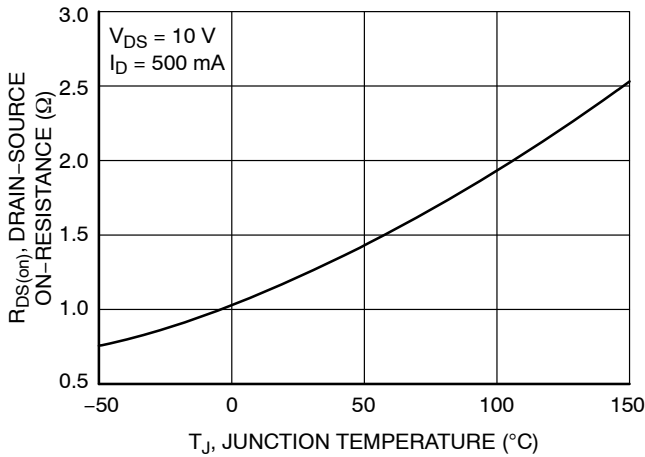


Figure 3. On-Resistance Variation with Temperature

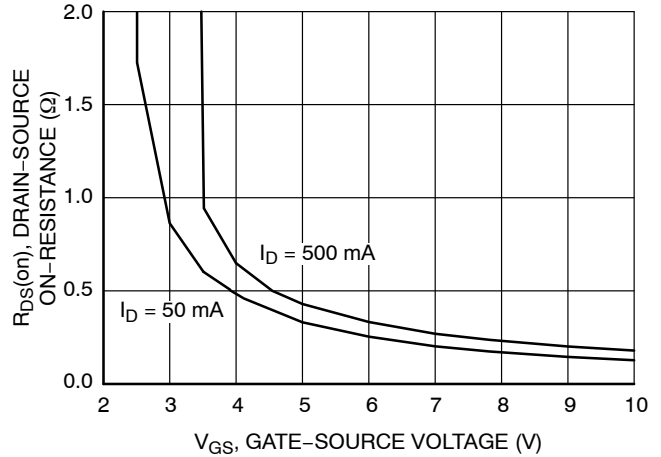


Figure 4. On-Resistance Variation with Gate-Source Voltage

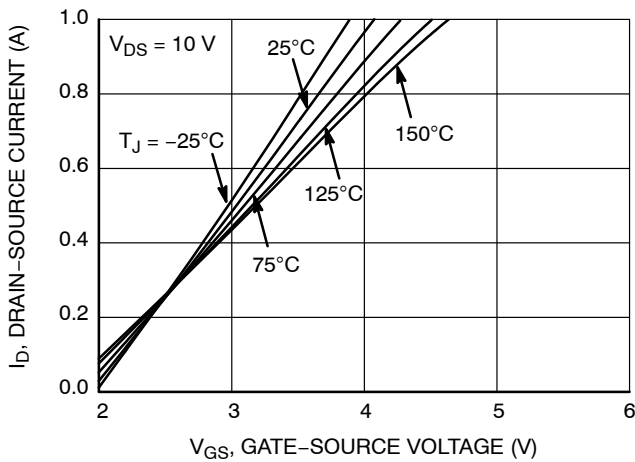


Figure 5. Transfer Characteristics

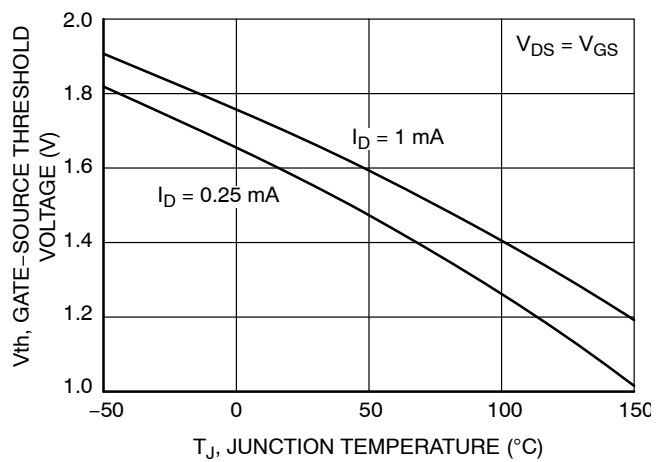
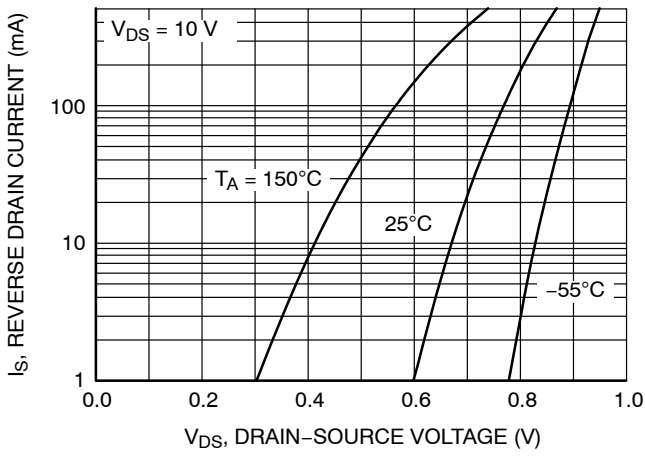
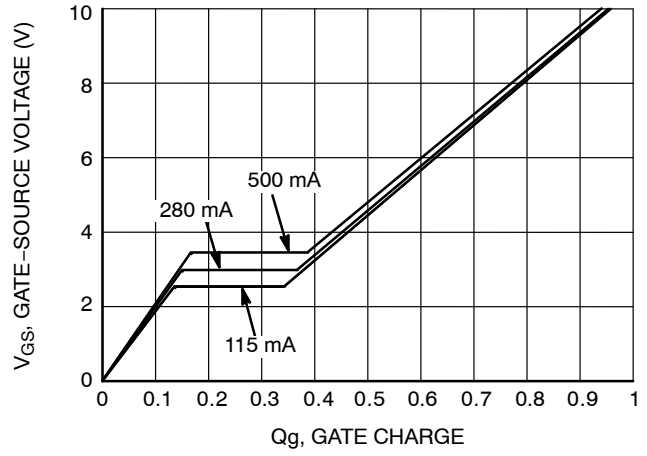


Figure 6. Gate Threshold Variation with Temperature

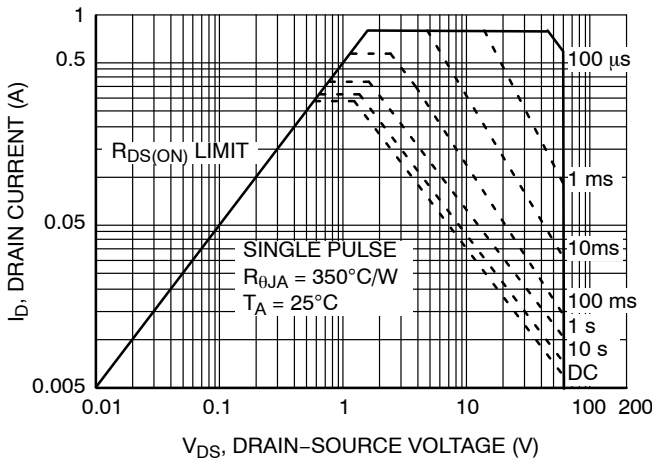
# 2N7002K



**Figure 7. Reverse Drain Current Variation with Diode Forward Voltage and Temperature**



**Figure 8. Gate Charge Characteristics**



**Figure 9. Maximum Safe Operating Area**

## ORDERING INFORMATION

Part Number	Top Mark	Package	Shipping <sup>†</sup>
2N7002K	7K	SOT-23 3L (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**SOT-23 (TO-236)**  
CASE 318  
ISSUE AT

DATE 01 MAR 2023

SCALE 4:1



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H <sub>E</sub>	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

**GENERIC MARKING DIAGRAM\***



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



**RECOMMENDED MOUNTING FOOTPRINT**

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**

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**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**



**SOT-23 (TO-236)**  
**CASE 318**  
**ISSUE AT**

DATE 01 MAR 2023

STYLE 1 THRU 5:  
 CANCELLED

STYLE 6:  
 PIN 1. BASE  
 2. EMITTER  
 3. COLLECTOR

STYLE 7:  
 PIN 1. EMITTER  
 2. BASE  
 3. COLLECTOR

STYLE 8:  
 PIN 1. ANODE  
 2. NO CONNECTION  
 3. CATHODE

STYLE 9:  
 PIN 1. ANODE  
 2. ANODE  
 3. CATHODE

STYLE 10:  
 PIN 1. DRAIN  
 2. SOURCE  
 3. GATE

STYLE 11:  
 PIN 1. ANODE  
 2. CATHODE  
 3. CATHODE-ANODE

STYLE 12:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. ANODE

STYLE 13:  
 PIN 1. SOURCE  
 2. DRAIN  
 3. GATE

STYLE 14:  
 PIN 1. CATHODE  
 2. GATE  
 3. ANODE

STYLE 15:  
 PIN 1. GATE  
 2. CATHODE  
 3. ANODE

STYLE 16:  
 PIN 1. ANODE  
 2. CATHODE  
 3. CATHODE

STYLE 17:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. CATHODE

STYLE 18:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. ANODE

STYLE 19:  
 PIN 1. CATHODE  
 2. ANODE  
 3. CATHODE-ANODE

STYLE 20:  
 PIN 1. CATHODE  
 2. ANODE  
 3. GATE

STYLE 21:  
 PIN 1. GATE  
 2. SOURCE  
 3. DRAIN

STYLE 22:  
 PIN 1. RETURN  
 2. OUTPUT  
 3. INPUT

STYLE 23:  
 PIN 1. ANODE  
 2. ANODE  
 3. CATHODE

STYLE 24:  
 PIN 1. GATE  
 2. DRAIN  
 3. SOURCE

STYLE 25:  
 PIN 1. ANODE  
 2. CATHODE  
 3. GATE

STYLE 26:  
 PIN 1. CATHODE  
 2. ANODE  
 3. NO CONNECTION

STYLE 27:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE

STYLE 28:  
 PIN 1. ANODE  
 2. ANODE  
 3. ANODE

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