Low Side SmartFETs

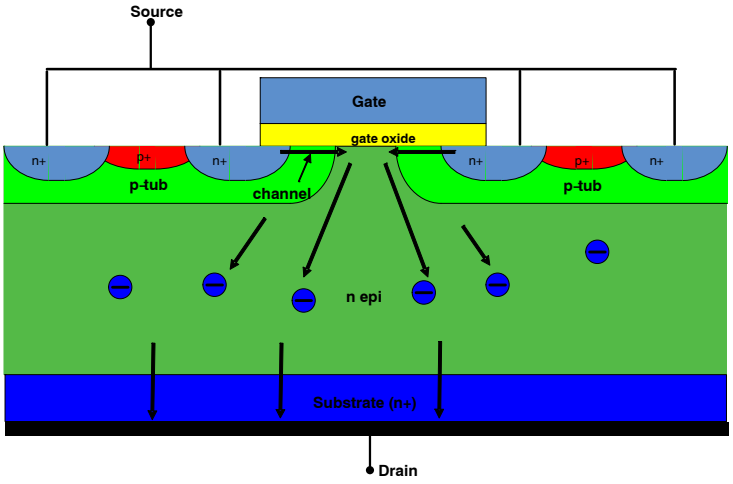
AND8202/D

Introduction

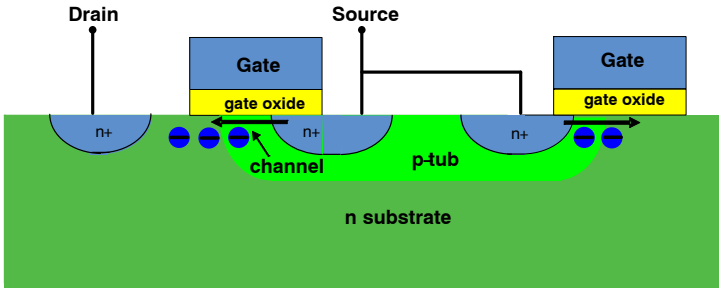
The ever increasing density and complexity of automotive and industrial control electronics requires integration of components, wherever possible, so as to conserve space, reduce cost, and improve reliability. Further, the components in an automotive environment can be often exposed to harsh operating conditions in the form of high voltage and/or high−power transients, cable short circuits, inductive overshoots, electrostatic discharges etc. These factors necessitate self−protection features to be integrated into power FETs used for switching automotive loads. Advancements in power MOSFET processing technology afford an economical marriage of protection features (such as current limitation) and standard MOSFET power transistor switches. This document describes the technological and operational details of **onsemi** Low Side SmartFETs. For any application specific details, it is recommended to refer to High Side SmartFETs with Analog current sense − AND9733.

Process Technology

The power stage in low side devices is realized using a standard vertical DMOS transistor process flow. The control and protection circuitry is monolithically integrated with the power FET. A vertical DMOS allows for greater transconductance, higher breakdowns, improved power densities and consequently better heat dissipation when compared to lateral power FETs. Figure 1(a) and 1(b) below illustrate the advantage in terms of Si area available for power distribution at the drain terminal in a vertical process. The planar gate stack structure, although offering a higher specific $R_{DS(ON)}$ (conduction losses for a given Si area) than its trench counterpart, does ensure greater energy handling capability, superior thermal response. Further, there is a reduced likelihood of current crowding, ease of manufacturability and higher reliability associated with planar gate FETs. Considering these trade−offs for the range of $R_{DS(ON)}$ targeted in the low side Smart−FET family (Refer Table 1), a planar gate with a vertical DMOS constitutes the optimal choice for the power element.



(a) Vertical DMOS Structure and Carrier Flow



(b) Lateral DMOS Structure and Carrier Flow

Figure 1. DMOS Structure and Carrier Flow

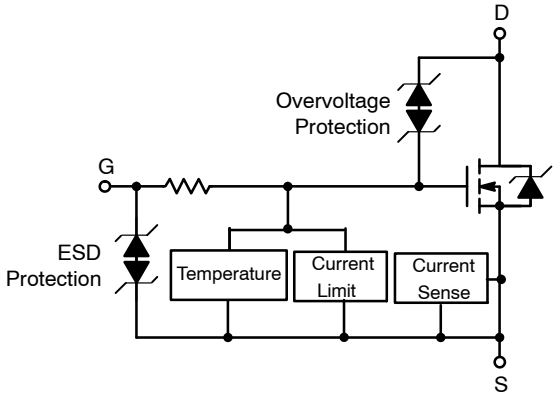


Figure 2. Generic Block Architecture of Low Side SmartFETs

General Topology

Figure 2 depicts the generic block level schematic of **onsemi** low side SmartFETs.

All devices employ ESD protection clamps at the gate input and over−voltage protection clamps between drain and gate to limit the voltage transients observed by the power transistor as well as to enable an active clamping mechanism (described later), while switching inductive loads. The ratings for these protection clamps are described in the Absolute Maximum Rating section of the respective product datasheet. In addition to over−voltage protection, other protection schemes include Over−Temperature shutdown (TSD), Differential Thermal Shutdown (DTSD) and current limitation (I_{LIM}) protections. The TSD protection limits the maximum junction temperature observed by the die by shutting down the device in case of a high temperature operation; DTSD protects the device from stressful thermal gradients and the I_{LIM} protection limits the output current to a pre−defined level in case of a short circuit or an overload condition. It should be noted that the availability of protection features may vary across devices in the portfolio and some devices may not be equipped with one or more of the protections discussed. Refer to product datasheets for available protection schemes and their specifications. All Smart−FETs can drive any type of resistive, inductive load and capacitive loads such as solenoids, heater coils, and filament bulbs limited only by the conduction and thermal capability of the device. Table 1 below lists the low−side family of devices and associated protection scheme.

Table 1. LOW SIDE PRODUCT FAMILY AND FEATURES

Device	Package	TSD	DTSD	I_{LIM}	Clamp Voltage (V) Typ
NCV8411	DPAK	X	X	X	46
NCV8413	DPAK/ SOT−223	X	X	X	46
NCV8412	SOT−223	X	X	X	46
NCV8412D	SO8	X	X	X	46
NCV8415	DPAK/ SOT−223	X	X	X	46
NCV8401A	DPAK/SOT−223	X	–	X	46
NCV8401B*	DPAK	X	–	X	46
NCV8403A	DPAK/SOT−223	X	–	X	46
NCV8403B*	DPAK	X	–	X	46
NCV8402A	SOT−223	X	–	X	46
NCV8402AD	SO8	X	–	X	46
NCV8405A	DPAK/SOT−223	X	–	X	46
NCV8405B*	DPAK	X	–	X	46
NCV8406A	DPAK/SOT−223	X	–	X	65
NCV8406B*	SOT−223	X	–	X	65
NCV8406D**	SO8	X	–	X	65
NCV8408	DPAK	X	–	X	46
NCV8440A	SOT−223	–	–	–	55

*Multiple assembly locations / **Product in development

Normal Operation

Under normal operation, the low-side product family operates the same as any standard power MOSFET device. Many of the data sheet parameters and data sheet curves are identical to those found on standard MOSFET data sheets. Since numerous application notes cover standard power MOSFET operations topics including gate drive control, gate charge, switching characteristics, thermal management, etc., this paper focuses only on load switching and fault condition operation as well as the modes of normal operation affected by fault protection circuitry.

Fault Types

Typical faults as observed in a low side application include short circuit to supply and/or ground, open load, over−voltage, over−temperature and dynamic over−power events.

Perhaps the most common and worrisome fault is a short circuit. This type of fault can take several forms, as detailed below:

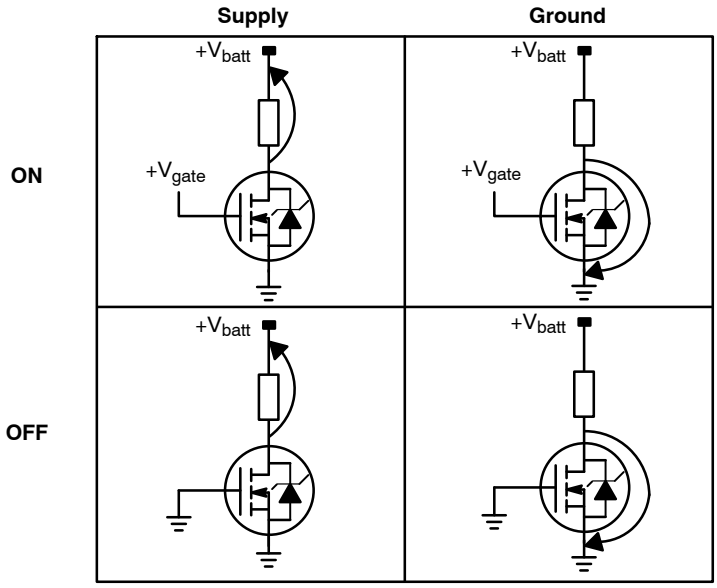


Figure 3. Short Circuit Modes

Such short conditions are further exacerbated since often the short circuits are intermittent and thus can take many forms during even very brief periods. For example, in the case of a short to ground with the MOSFET off, one normally would not worry about the FET since current is diverted through the short. However, if the short is intermittent and the load is inductive, the interruption of the current flow results in a fly-back voltage appearing at the drain node of the FET. The peak current in the load inductance could be higher than normal operation due to the duration of the short and when the resistance of the short is less than the operating resistance of the MOSFET. Thus the device may absorb more energy than expected, and numerous intermittent short events occurring in quick succession could result in elevated peak junction temperature, leading to potential device destruction.

A short circuit to supply with the FET on often results in an overload condition as there is little to no load impedance to limit the current through the device. An over−voltage condition may exist because of electro−static discharges at the device pins, supply line transients and/or an inductive discharge event. An open load does not overstress the device in most cases and consequently protection circuit is not required. Overtemperature failure typically results from another failure such as short circuit which vastly increases device power dissipation, but can also result from extreme ambient conditions or a thermal path anomaly such as a solder void between the device heatsink and circuit board. Finally, a dynamic over−power event can inflict severe thermal transients, or “shocks” to the die. Such stresses, if applied repetitively, affect the reliability and lifetime performance of the device. An example of such use−case is the activation of a capacitive load (such as a bulb), requiring high inrush currents, through the life of the device. The control circuitry of the low-side products can detect and control device operation during many of these failure modes by operating in a safe mode so the device can return to normal function once the fault is remedied. These control features are biased off the input pin and a study of the protection features necessitates a thorough understanding of the gate input operation as explained in later sections.

Gate Input Operation

The gate input pin on the low-side family of products behaves very much like the gate pin of a standard MOSFET. The voltage at the gate input pin is linearly related to the gate of the power MOSFET output transistor and as such, the magnitude of this voltage determines the operation mode of the output stage. At voltages below the device threshold, the device remains off and blocks the load supply voltage. As

the gate voltage increases above threshold, the device channel becomes progressively enhanced, putting the MOSFET into the on state. As in case of standard MOSFET devices, exceeding the rated voltage on the gate pin can result in rupture of the gate oxide, thereby damaging the device. While the input pin of a low side SmartFET can be driven by a standard MOSFET driver, the source and sink capabilities of the driver should be carefully considered accounting for the drive requirements of the control circuitry.

A simplified input circuit is shown in Figure 4. Under normal operation, the voltage supply at the input must be capable of driving the output stage as well as the reference circuit for over−temperature and current limit protection. In a fault mode, the activation of protection circuit can cause the current at this pin to be orders of magnitude higher than that in normal mode as explained below.

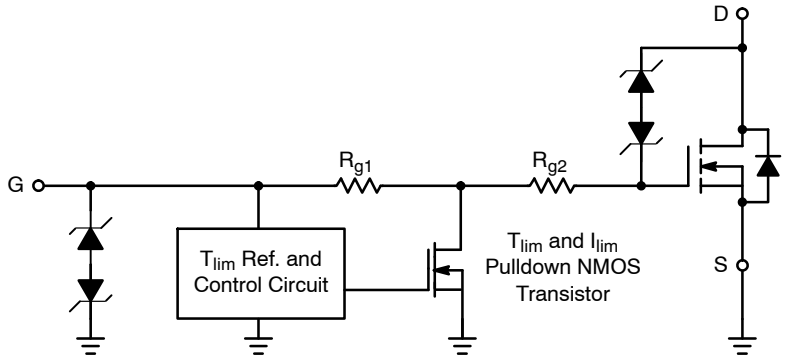


Figure 4. Simplified Input Circuit

When the device is in a current limit operation mode, a feedback loop to the current limit pulldown transistor will drive the gate of the power FET to near threshold voltage, thereby regulating the device in linear mode. Thus in this mode, the gate input supply must be able to source a current equal to $(V_{in} - V_{gate}) / R_{g1}$ plus additional bias current, where V_{gate} is near threshold voltage. During thermal shutdown, the T_{lim} pulldown transistor pulls the gate voltage down to ground potential, thereby shutting off the output stage. Thus, the gate input supply must source current equal to approximately V_{in}/R_{g1} plus some additional bias current. In addition, R_{g1} (and R_{g2}) are negative temperature coefficient devices, thus temperature shutdown operation mode is the worst case condition for determining minimum gate drive current source and sink requirements. This minimum source current must be available during an overtemperature fault. If not, the pulldown transistor may not keep the power FET off, possibly allowing the junction temperature of the power FET to reach the destructive level. The following table lists nominal room temperature values of R_{g1}, R_{g2}, and typical gate input current for normal and T_{lim} fault conditions at elevated temperature by device.

It should be noted that the new generation NCV841X devices incorporate differential thermal shutdown protection (as explained in later sections) as well. While the circuit is slightly different, the principle of gate current variation stays the same, and the gate drive supply must be capable of sourcing the required current in the protection mode.

In some devices, a current monitoring mechanism at the input terminal can provide the feedback on the operation mode. Given that the input current in thermal shutdown is significantly higher than that in nominal operation, externally sensing the gate current can let the customer know if a thermal shutdown has been enforced or not. Such a mechanism is particularly beneficial in devices such as NCV8408 in which the output stage is latched off after thermal shutdown, or in the new generation (NCV841X) low side devices that have distinctly specified gate current ranges for normal and fault mode operations (Refer datasheets). In devices with auto−retry, the gate current will continuously be changing as the output stage is toggled on and off. The sensing mechanism at the gate input will therefore be challenged and the accuracy of the external sensors/comparators must be considered while attempting to measure and diagnose the RMS input current.

Table 2. TYPICAL GATE INPUT PARAMETERS

Device	R_{g1} (kΩ)	R_{g2} (kΩ)	I_g @ 5V (μA), T_J = 25 °C	I_g @ 5V (μA), $T_J > T_{lim}$
NCV8411	9.9	5.0	50	633
NCV8413	13.5	9.0	50	500
NCV8412	10	90	52	630
NCV8412D	10	90	52	630
NCV8415	30	20	50	240

Table 2. TYPICAL GATE INPUT PARAMETERS (continued)

Device	R_{g1} (kΩ)	R_{g2} (kΩ)	I_g @ 5V (μA), T_J = 25 °C	I_g @ 5V (μA), $T_J > T_{lim}$
NCV8401A	9.9	5.0	50	600
NCV8401B*	9.9	5.0	50	600
NCV8403A	13.5	9.0	50	450
NCV8403B*	13.5	9.0	50	450
NCV8402A	60	40	50	150
NCV8402AD	60	40	50	150
NCV8405A	30	20	50	220
NCV8405B*	30	20	50	220
NCV8406A	1.0	0.5	30	5900
NCV8406B*	1.0	0.5	30	5900
NCV8406D**	1.0	0.5	30	5900
NCV8408	14.4	11	25	440

The resistances, R_{g1} and R_{g2}, in addition to affecting minimum input source current requirements, also affect switching speed and EMI/RFI requirements for the gate drive design. The gate of the power MOSFET essentially is a capacitive load to the gate drive supply, so any resistance in series with the gate input will slow down the rising and falling switching transitions of load current and voltage. Many discrete MOSFET circuit designs add 1.0 kΩ or more of external series gate resistance in order to slow the normally nanosecond rise and fall times, especially in applications with strict EMI/RFI limitations. Since all low side SmartFETs have integrated series gate resistance, addition of external series gate resistance may not be necessary.

Lastly, the gate input pin of a MOSFET device may be subjected to ESD during the assembly, test, installation, and service of the circuit board. All low side devices incorporate back to back ESD diodes (Figure 4) at the gate input pin. These diodes, coupled with the internal series gate resistance, provide the required ESD capability. For specifications on zener breakdowns and ESD performance, refer to product datasheets.

Current Limit Protection

The current limit protection is invoked in case the drain current exceeds a set threshold. In most cases, a short circuit across the load (short to supply when the FET is ON per Figure 3) causes the drain current to increase. Very seldom, an overload condition may also exist because of an anomaly in the load including its degradation over lifetime. In either case, the current in the output MOSFET can increase to detrimental levels if not limited internally by the device.

Figure 5 shows a simplified current limit block architecture used in low-side devices. The current limit function utilizes a load current sensing technique in which a part of the power FET is sectioned off as Sense FET. The vertical DMOS FET is comprised of individual “FET fingers” in parallel. The source metal can be patterned in a way such that it allows for separate source contacts– one for the power FET and other over the Sense FET. The sense FET, with its gate and drain still connected to power FET, conducts a current proportional to that in the power FET with a ratio governed by the ratio of the active areas of two FETs. The source connection of the Sense transistor is known as the mirror connection and the ratio of current through the larger device to the current through the Sense device is known as the current mirror ratio and is symbolized by the letter n. This means a sense current equal to only 1/n of the load current flows through the current mirror MOSFET. The lower power dissipation in the sense path allows for the integration of a sense resistor in the control circuit. More detailed information regarding SENSEFET technology is found in **onsemi** application note AND8093/D.

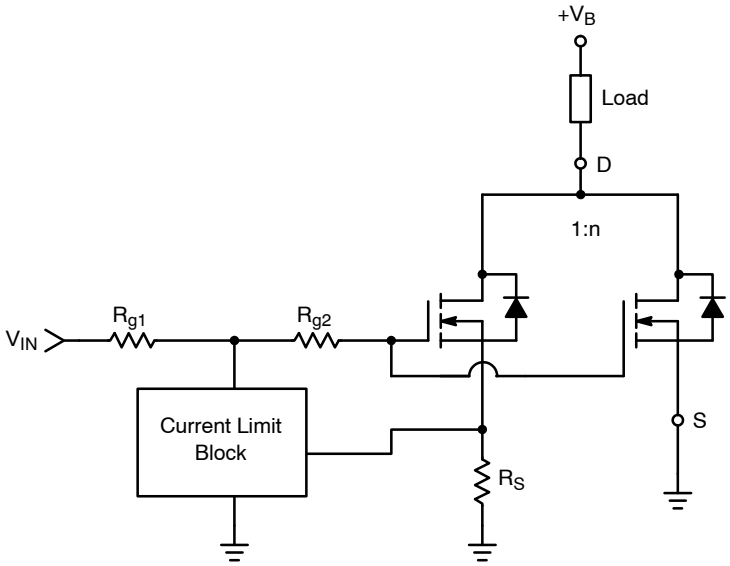
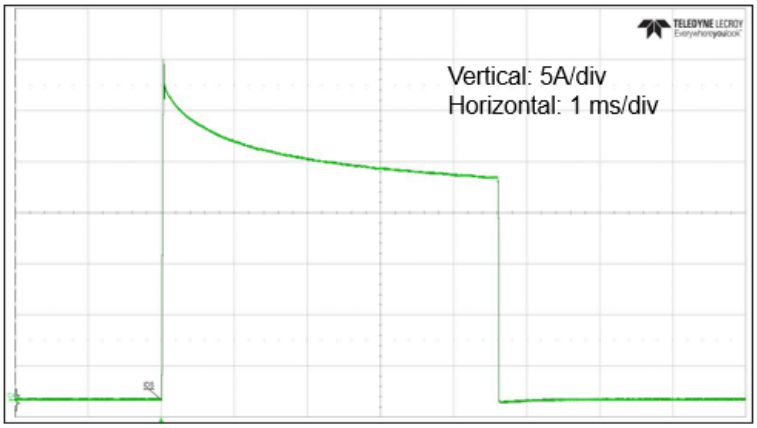


Figure 5. Simplified Current Limit Circuit

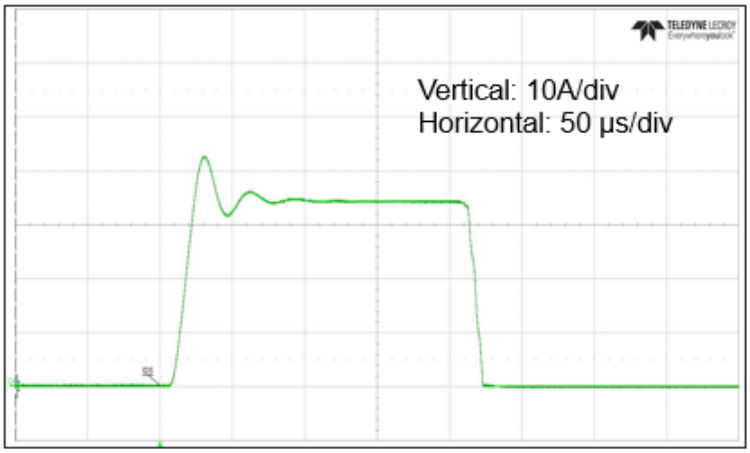
The voltage developed across R_{Sense} is fed to the current limit control block which then controls the gate of the output stage. As the load current increases, the sense current increases proportionally and so does the voltage developed across R_{Sense}. When the voltage across R_{Sense} exceeds an internal pre−set threshold (in accordance with the desired current limit trip threshold), the voltage at the gate of the power FET is reduced such that it operates in a linear, or regulation mode. This feedback loop ensures that the channel is not fully enhanced but sufficient to maintain the load current at the setpoint value while the current limit circuit is active. Not only is the device conducting high current, but it is conducting this current at high drain to source voltage. In the case of a near perfect short across the load, nearly all of the load supply voltage is across the drain to source of the power MOSFET. Thus, in the current limit operation mode, the device dissipates significant power. A sustained operation in current limit is therefore not recommended as it may affect the device performance over lifetime.

In the older generation devices, the current limit block primarily constituted a pull−down FET (at the gate of the power MOSFET) whose input threshold is controlled by the voltage across R_{Sense}. The new NCV841X devices utilize an active op−amp based circuit to control the gate of the power MOSFET. The new architecture offers a stable current limit threshold across temperature as explained below.

As the power MOSFET heats up during the current limit operation, the adjacent control circuit also observes a rapid increase in temperature. The sense resistor and the threshold of the pull-down FET exhibit a strong dependence on temperature which causes a wide variation in the limited current in case of a persistent overload or short circuit condition. The threshold of the pull−down FET usually reduces with increase in temperature which is reflected in the sharp negative slope of the regulated current with time in the oscilloscope waveform per Figure 6a). The new architecture eliminates this dependence on the threshold voltage to regulate the output MOSFET by replacing the pull−down FET with a more efficient circuit. The resulting current limit is more stable and predictable across temperature as shown in Figure 6b).



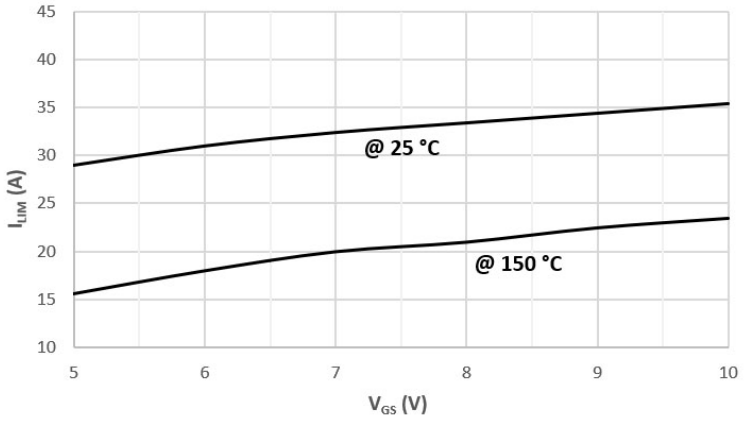
a) Typical Current Limit profile in NCV8401 at room temperature



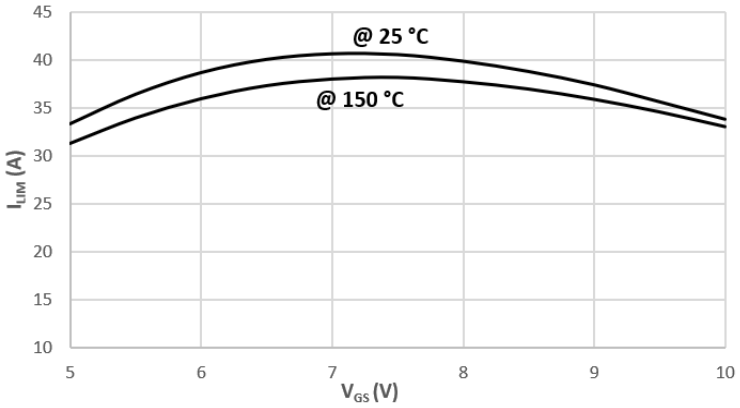
b) Typical Current Limit profile in NCV8411 at room temperature

Figure 6. Typical Current Limit Profile

The current limit value not only varies with temperature, as discussed above, but also with applied gate voltage. A higher gate voltage requires more current in the current limit block so as to discharge or pull this potential down which in turn requires a higher voltage developed across the sense resistor. Since this voltage is directly related to sense or load current, a higher gate voltage essentially implies an increase in the current limit trip threshold. Figure 7a) shows the variation of typical measured current limit in NCV8401 across Gate−Source voltage. With the improved circuit in NCV841X devices, the dependence on gate voltage is also weakened, especially at higher gate voltages where the current limit is pulled back close to its value at VGS = 5V. The typical measured current limit on NCV8411 is plotted in Figure 7b).



a) Measured current limit across gate−source voltage in NCV8401



b) Measured current limit across gate−source voltage in NCV8411

Figure 7. Measured Current Limit across Gate−Source Voltage

The series resistance R_{g2} limits how fast the current limit circuit reacts to load current exceeding the current limit setpoint. Discharging the power MOSFET capacitance through R_{g2} limits the current in the current limit block. This results in limiting the dv/dt observed at the power MOSFET drain as the drain voltage transitions from low on-state magnitude to a higher magnitude in linear operation. This is important because a high magnitude dv/dt, especially coupled with higher supply voltages, may result in latchup of one or more NMOS control transistors. Latchup can occur when enough current is injected into the NMOS structure so that a normally shunted parasitic P−N junction is forward biased. The injected current comes from the capacitance formed by the depletion region between the drain and P-tub source region, from the relation i = CdV/dt. In the low-side device process, each NMOS transistor layout is optimized to reduce susceptibility to injected currents and R_{g2} is added as an additional structure to eliminate device latchup.

Over−temperature Shutdown Protection

An over−temperature condition can be absolute− in which the junction temperature on the die exceeds a pre−set threshold; or can be differential− in which there is a rapid gradient in junction temperature due to a transient high-power dissipation through the device. While the older generation devices offer protection only in case of an absolute over−temperature event, the new NCV841X family is equipped with both absolute as well as dynamic over−temperature protection schemes.

Figure 8 diagrams a simplified overtemperature detection and shutdown circuit.

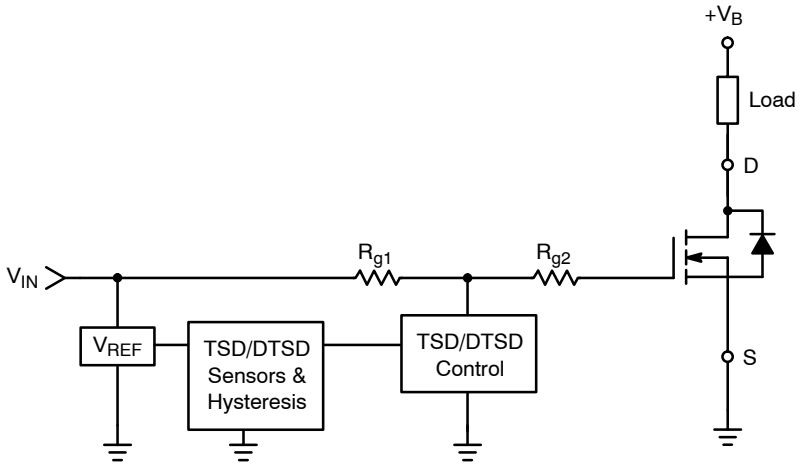


Figure 8. Simplified Over−temperature Shutdown Circuit

An internal reference voltage generated off the input supply biases the on−chip temperature sensitive elements. These sensors are generally realized close to the center of the power FET active area on the die which is expected to observe maximum temperature in case of power dissipation through the device. If a temperature exceeding the TSD threshold is sensed, then the TSD protection circuit pulls down the gate voltage of the power FET thereby shutting off the output stage. A hysteresis circuit allows the output stage to turn back on after the junction temperature on the die cools down to a defined setpoint.

In case of differential thermal protection, another sensing element, at the periphery of the FET active area, is utilized. In case of a sudden “thermal shock” to the die, the difference between the two sensed temperatures is monitored and compared to a preset threshold. Figure 9 is a pictorial representation of the sensors termed as “hot” and “cold” in accordance with their anticipated relative temperatures in case of power dissipation through the device. Intuitively, the sensor at the periphery of the FET active area will observe a lower temperature than that at the center as the heat wave propagates through the die. Shutting off the output stage in case of large temperature gradients prevents the die from getting “worn−out” over the lifetime as explained below.

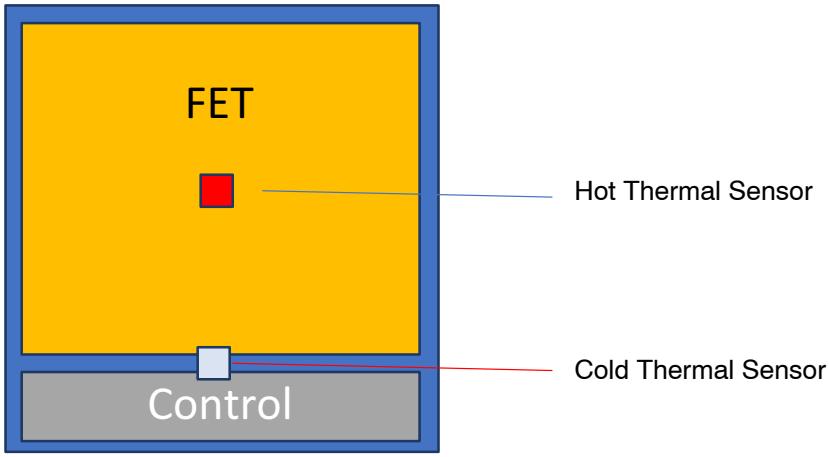


Figure 9. Sensing Elements in Differential Thermal Shutdown

Consider the idealized set of waveforms in Figure 10 depicting a short circuit to supply. The ambient temperature in this case is −40°C. When the current exceeds the ILIM threshold, the output stage is regulated and power dissipation through the FET increases. As the die heats up, the gradient between the hot and cold sensors increases and eventually the output stage is turned off when the difference between the two sensors reaches ~ 60°C (typical DTSD threshold in most low side devices). The FET is turned on with a hysteresis as in case of absolute TSD. If the short is persistent, the temperatures measured by both the sensors increase with each “retry” and after some cycles, an absolute thermal shutdown threshold will be attained which will then override and protect the device thereafter. In the absence of a differential thermal shutdown mechanism, the output stage will not be turned off until the junction temperature reaches ~ 175°C (typical TSD threshold in most devices). This implies an initial gradient of more than 200°C considering

an ambient temp of −40°C at the beginning. Such high temperature gradients inflict a huge amount of stress on the die and reduce its lifetime and reliability, especially when such stresses are applied repetitively.

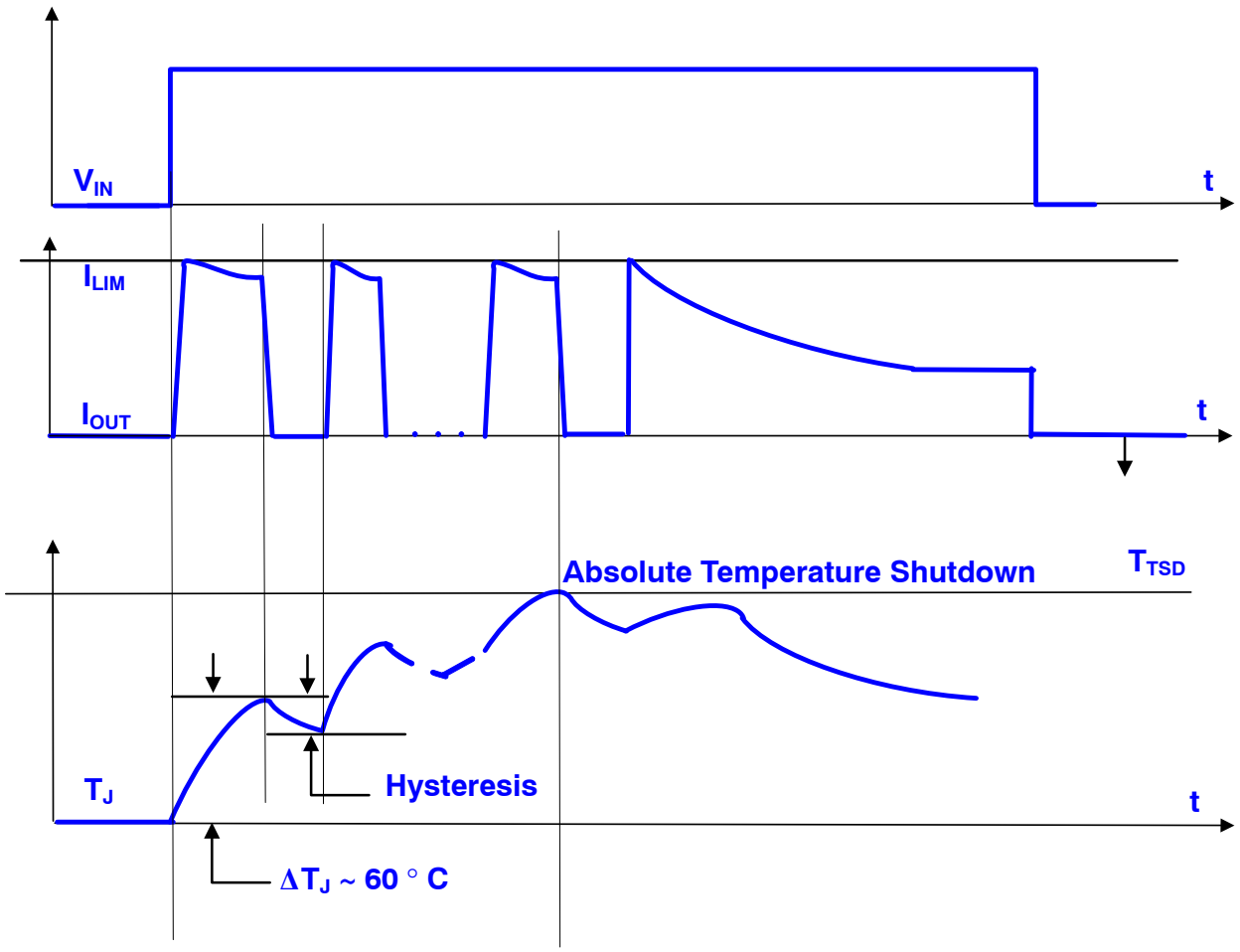


Figure 10. Idealized Wave−set depicting DTSD Protection (not drawn to scale)

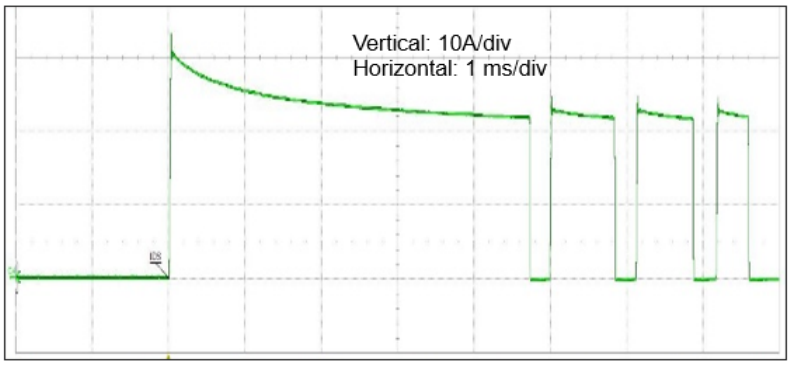
The repetitive short circuit (RSC) performance of these products is quantified in terms of the number of cycles withstood without a failure per the AEC−Q100−012 standard. The standard also grades the devices based on their short circuit performance per the table below. The NCV841X family of devices, equipped with Differential Thermal Shutdown, offer a superior RSC performance than the older generation of devices.

Table 3. RSC Grades per the Number of Cycles Applied in accordance with AEC−Q100−012

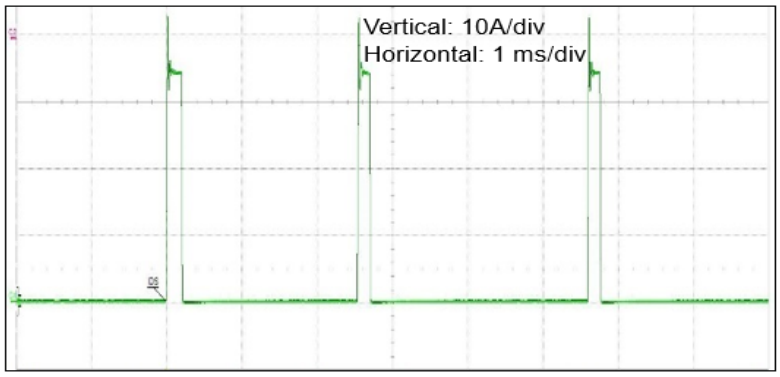
Grade	No. Cycles	Lots	Samples / Lot	No. Fails
A	>1,000,000	3	10	0
B	300,000 .. 1,000,000	3	10	0
C	100,000 .. 300,000	3	10	0
D	30,000 .. 100,000	3	10	0
E	10,000 .. 30,000	3	10	0
F	3,000 . .10,000	3	10	0
G	1,000 .. 3,000	3	10	0
H	300 .. 1,000	3	10	0
O	<300	3	10	0

Oscilloscope captures below depict the absolute and differential thermal shutdowns associated with the current limit pulse trains in case of a short circuit applied to NCV8401 and NCV8411 respectively. As can be noticed that the output stage turns off in NCV8411 earlier in time because of the DTSD control as compared to the absolute

TSD control in NCV8401. Both the waveforms were measured at an ambient temperature of 25°C with V_{GS} = 5 V and V_{BAT} = 12 V. It should also be noted that while the waveforms hold a comparative significance in time, the absolute response times will depend on the thermal management in the application and may differ from one application to another.



a) TSD Thermal Cycling in NCV8401



b) DTSD Thermal Cycling in NCV8411

Figure 11. Thermal Cycling

While the majority of low side SmartFETs from **onsemi** are designed with hysteretic auto−restart capability in an over−temperature scenario, certain devices such as NCV8408 are designed to latch off the power MOSFET with thermal shutdown and allow a restart only after the input pin is toggled. It is recommended to refer to individual product datasheets for device specific retry strategy.

Since the reference voltage for the temperature sensing elements is affected by the magnitude of the gate input supply voltage, especially at lower gate voltages, the overtemperature setpoint decreases as the gate input voltage increases up to approximately 5.0 V. As depicted in Figure 12, the overtemperature threshold can reach high values of more than 200°C at gate voltages less than 4 V. This implies that driving the device with low gate voltages, for instance with a 3.3 V input, may expose the die to high temperatures that can potentially damage the device. It is, therefore, not recommended to employ low gate drive voltages. In addition, while using external protection resistors at the input pin, the drop across this resistor must be accounted for as this drop would reduce the available voltage at the input pin to bias the TSD block. In general, onsemi recommends using a standard 5V supply at the gate input with sufficient current capability for both normal and fault mode gate drive. This also ensures performance adherence to specification since datasheet parameters are generally specified at 5 V (or 10 V) gate voltage. As the applied gate voltage increases above 5.0 V, the temperature shutdown limit marginally increases with increasing gate voltage. This is illustrated in Figure 12. The slight increase in the temperature shutdown limit for gate voltage above 5.0 V is due to the increased gate drive required by the NMOS pulldown transistor as the NMOS drain voltage increases.

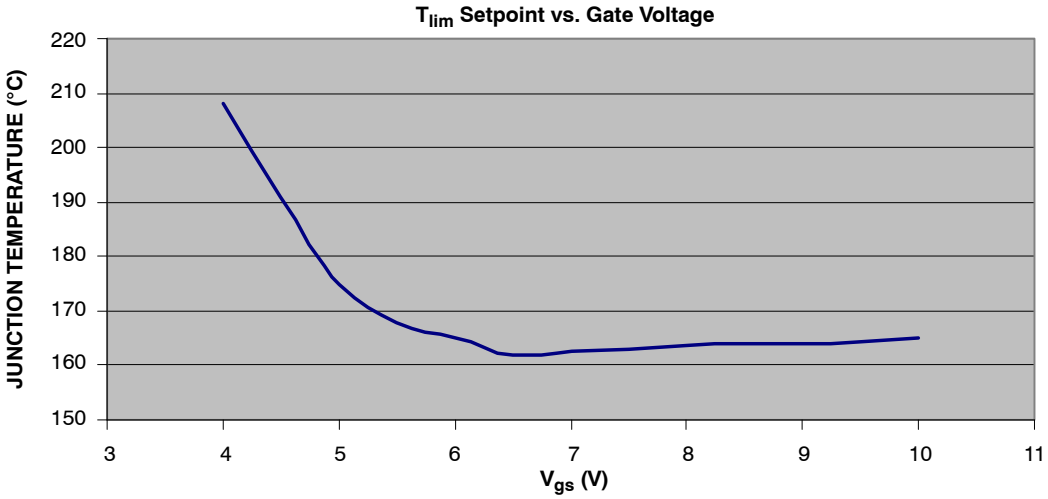


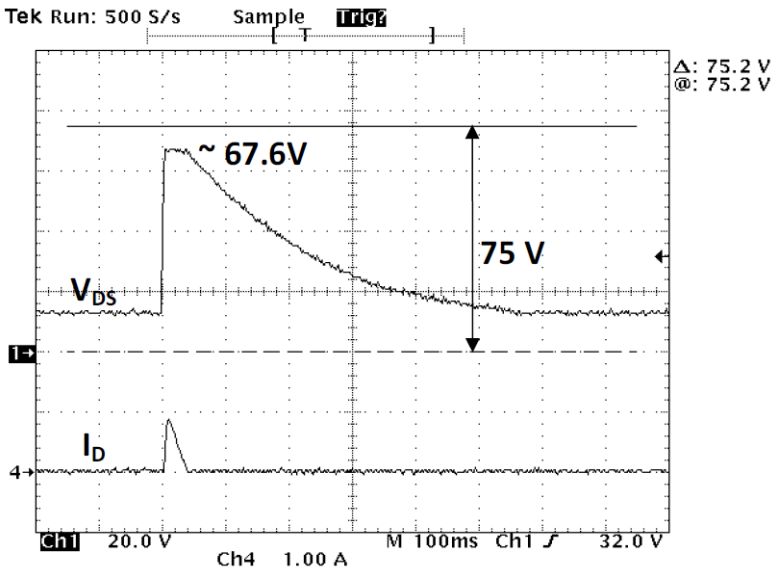
Figure 12. Typical Temperature Limit Shutdown as a Function of Gate Voltage

Over−voltage Protection

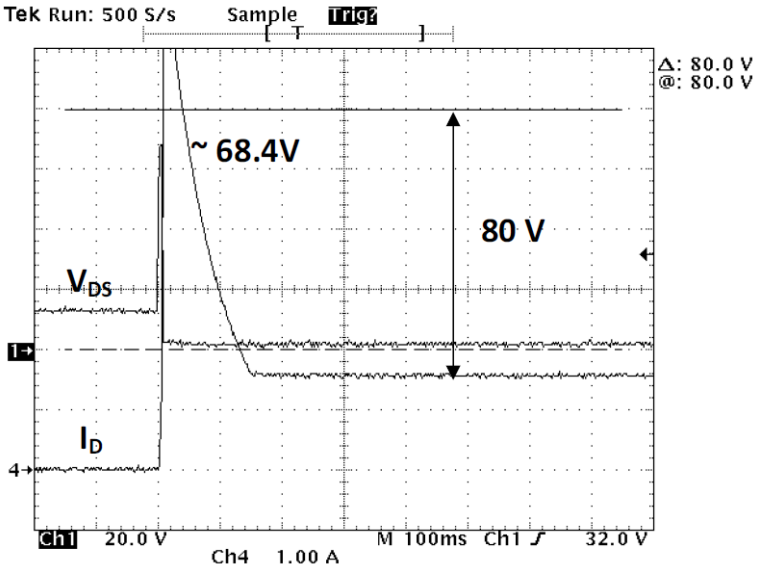
Automotive environment is susceptible to high voltage transients often inflicted in the form of ESD (Electro−Static discharge) overstresses, alternator load dumps, as well as parasitic supply line transients modelled in ISO 7637−2. Further, an inductive load discharge can also expose the device to high voltage levels. onsemi low side SmartFETs have integrated over−voltage protection structures designed to handle these stresses. Figure 13 highlights these structures. The ESD diodes from gate−source limit the transients observed across the gate−stack structure and thereby protect the gate oxide from getting damaged. In case an application is expected to frequently observe high voltages at the input drive, it is recommended to place protection resistors at the input pin of the SmartFET to limit the current through these ESD diodes. Further, in applications employing a sense resistor at the source terminal, caution must be exercised to ensure that the gate−source differential voltage does not exceed the breakdown of these protection diodes. The absolute maximum rating section of the respective product datasheets must be referred to for specifications on these ESD structures.

The alternator load−dumps and supply line transients seldom present a high voltage at the output terminal. The over−voltage protection clamps between drain and gate protect the device in such case. If the voltage at the drain increases over and above the clamp breakdown, and the input command to the device is turned off, the protection diodes are activated and regulate the device with the active clamping mechanism (as described in *Inductive Switching* section). If the input is turned on, the load impedance limits the current through the device and at high supply levels, current limitation can be triggered. In either case, if the over−voltage event is expected to last over an extended duration, then the thermal capability of the device must be considered while selecting the device for an application.

For instance, the waveforms in Figure 13 depict the stimulated load dump capability of NCV8406. The measurements were performed with a 7 Ω load resistor at room temperature. As can be seen in the waveforms, the device passes a load dump level of 75 V (typically sustained over 100's of milliseconds) while gets damaged at a load dump level of 80 V with the output stage latching on and current being limited by the load impedance. The input command to the device was off in both scenarios implying that the protection features were not available during load dump stress. While the clamp is engaged in both cases, the power dissipation in the regulation mode at the higher load dump level is sufficient to increase the die temperature beyond it's max capability which causes the device to fail. It can also be observed that the clamp breakdown is "stretched" as the applied voltage increases. This is because the breakdown characteristics of protection diodes exhibit a resistive component and do not mimic that of ideal zeners. A higher load dump level essentially forces a higher current through the clamps thereby yielding a slightly higher clamp breakdown. The instantaneous power dissipation through the device can simply be calculated as $(V_{pk(transeint)}(t) - V_{Clamp}(t)/R)_L{}^*V_{Clamp}(t)$ where R_L includes both the external resistance and any resistance internal to the load dump supply. If the cumulative power dissipation, at any point while the clamps are engaged, causes the die temperature to exceed maximum device capability, then the gate will lose control of the output stage resulting in permanent damage to the device. It can thus be inferred that the thermal management in the application is also crucial to surviving such over−voltage events. It should be noted that the damage to the device in this case was obvious in the waveforms. In many cases, however, the damage is not noticeable and over−voltage stress manifests itself as a non−conformance to the guaranteed electrical parametric specification. The device performance is therefore assessed by checking key performance parameters such as $R_{DS(ON)}$, leakage, threshold etc. before and after the stress is applied. In general, the higher the clamp voltage, the greater the load resistance and the larger the device active area, the greater the peak transient drain voltage that the device can survive.



a) Pass: V_{GS} = 0 V, Va + Vs = 75 V (Device clamps at 67.6 V)



b) Fail: V_{GS} = 0 V, Va + Vs = 75 V (Device clamps at 68.4 V)

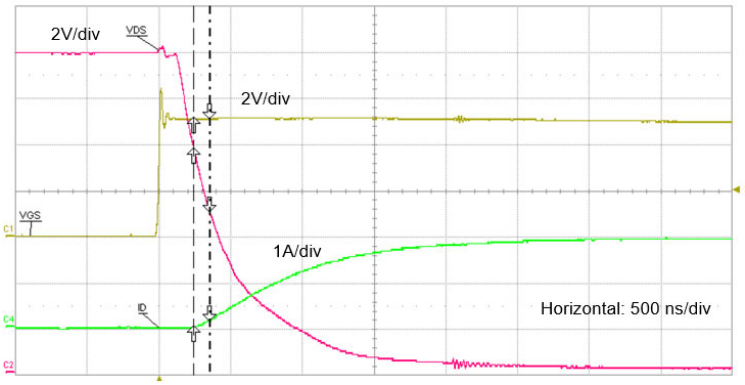
Figure 13. Stimulated Load Dump Capability in NCV8406

Load Switching

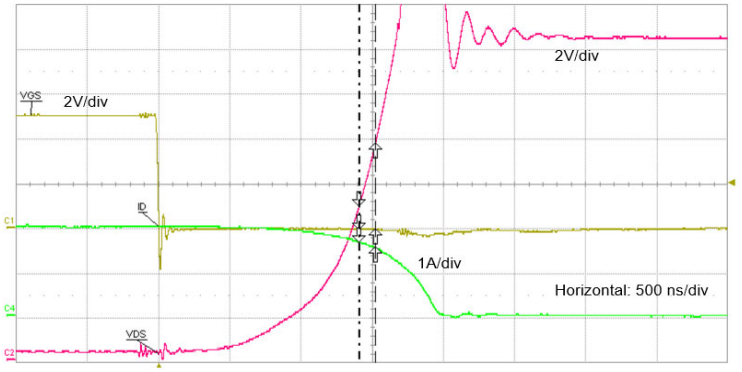
Resistive Switching

onsemi low side SmartFETs can be used to switch a variety of resistive loads including, but not limited to, LEDs, squibs, heating elements etc. The internal resistors connected to the gate terminal limit the output slew rate thereby improving the EMI performance of the device in addition to serving the protection features. Most automotive loads require switching frequency in the range of a few hundreds of Hz. The turn on and turn off times of a device must be referred to while making the selection for the application. For certain applications that require fast switching, devices such as NCV8406 offer faster turn off and turn off times with intentionally reduced internal resistors− Refer Figure 14 a) and 14 b) for typical measured turn on and turn off response in NCV8406 at room temperature with no external gate resistor. Switching times also relate to the efficiency of a SmartFET in the form of switching energy losses. In a high−speed application, switching losses can contribute to a significant proportion of overall losses and may even override conduction state losses. It should also be noted that switching times in the datasheet are specified against a set of conditions such as the load resistor, external input resistor, gate voltage etc. While selecting a device for an application, it is recommended to ensure that any difference in conditions with regards to the

application conditions is accounted for. For example, a higher gate voltage forces a faster turn on time; an external gate resistor, on the other hand, will slow down the switching times. In addition to switching times, the datasheets also specify slew rates during turn on and turn off. These allow the user to calculate the turn on times specific to a battery voltage.



a) Turn−on response in NCV8406



b) Turn−off response in NCV8406

Figure 14.

Inductive Switching

A wide majority of automotive loads, including solenoids, relays, motors, actuators etc., are inductive in nature ranging from a few mH's all the way to 100's of mH's. Automotive cables and harness, to a certain extent, present an inductive impedance (to the order of a few μH's), making it imperative for the SmartFETs to be able to drive inductive loads. Unlike resistive loads, the voltage and current polarity in inductive loads is opposite to each other and load switching is often accompanied by high voltage transients (dependent on the rate of output current decay and the value of inductance). The low side devices are equipped with an internal clamp to limit the output voltage excursions in case of an inductive flyback event.

Figure 15 and Figure 16 depict the schematic representation and a typical oscilloscope wave capture in case of inductive load switching.

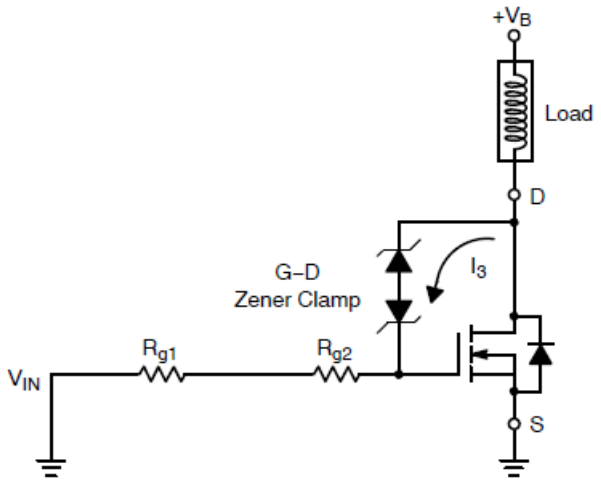


Figure 15. Inductive Switching Circuit Diagram

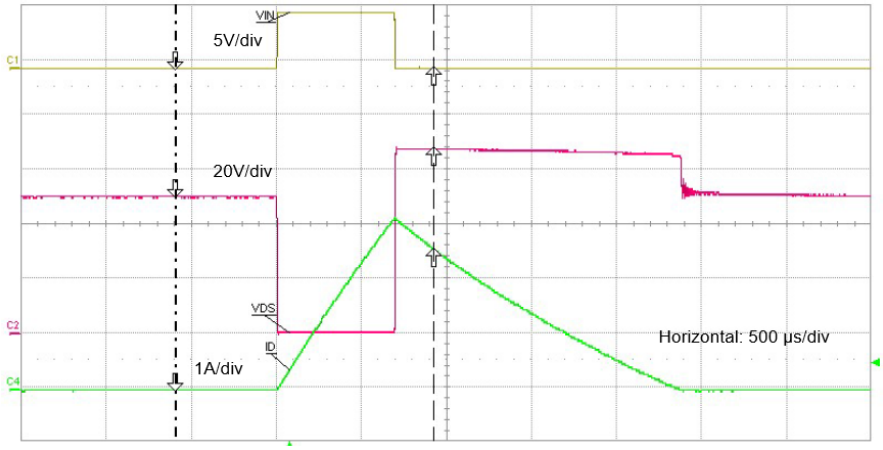


Figure 16. Inductive Switching Oscilloscope Capture on NCV8406D with L = 10 mH

As the device turns on, the inductive load is charged to a current defined by the power supply voltage, conduction losses across the device and the duty cycle of the input PWM drive. Most inductive loads have a resistive component as well which limits the peak load. Ignoring the line resistance, the time required to charge the inductance to a pre−defined current level can be expressed with the equation below:

$$t_{ON} = \frac{I_{pk} \times L}{V_{BATT} - V_{DS(ON)}}$$

While switching inductive loads, the most critical aspect is the driver's ability to handle the inductive flyback energy at switch−off. As the input command to the driver observes a high → low transition, the current flow in the inductor is interrupted and it develops a voltage at the output terminal to oppose the change in current flow. As the current starts to decay, the output voltage increases. In the absence of an internal voltage limiting mechanism, the output voltage can reach detrimentally high levels. To preclude such a scenario, **onsemi** low side SmartFETs have integrated drain−gate clamps as shown in Figure 15. The breakdown voltage of these clamps is set lower than the process breakdown of the output FET. This prevents the body diode of the output FET from avalanching each time when an inductive discharge happens. Repetitive avalanche breakdowns of the body diode can present a reliability concern over the lifetime of the device. Similar to the charge time, the discharge time (ignoring the line resistance) can be expressed as below:

$$t_{OFF} = \frac{I_{pk} \times L}{V_{CLAMP} - V_{BATT}}$$

It should be noted that the switching times are entirely dependent on the external conditions because of the underlying assumption that the value of inductance, or peak current is not too low to infringe with the response times of the device and the integrated clamp. In other words, the speed and response of the clamp to the inductive stimulus is very fast and the resulting switching times are entirely dependent on the external factors such as the peak current or the value of the inductance itself.

In addition to voltage limitation, the drain to gate clamps engage an active clamping mechanism by developing a voltage at the gate of the output FET. When the clamps are active, the current through these clamps bias the internal

gate resistors, and the voltage at the gate node becomes greater than the threshold voltage of the FET. The output stage is, thus, regulated in a linear mode and the inductive current is discharged across the entire FET active area. As the current decays, the gate voltage slightly reduces but is still maintained over and above the threshold until the current entirely discharges to zero. At this point, the output voltage and gate voltage also drop to zero and the output stage is turned off. Such a mechanism is called Self Clamped Inductive Switching (SCIS) capability. Without these clamps, the inductive current is discharged across the body diode which limits the energy handling capability of the device. The energy capability is defined by the maximum current that can be discharged across the device corresponding to a given inductor. As the device operates with a high voltage across drain−source, the temperature in an SCIS event can increase rapidly as the power is dissipated during inductive discharge. An important consideration here is the absence of over−temperature protection feature during the flyback. Since an inductive discharge only happens when the input observes a high → low transition, the TSD sensors and the protection circuit (Refer Over−temperature shutdown), that are biased off the input supply rail, remain inactive. This implies that the temperature can reach destructive levels at high discharge currents, which then puts a ceiling on the maximum allowed current, or correspondingly a maximum allowed SCIS energy. The energy capability is a quantitative metric widely used to qualify the performance of a SmartFET. In simplistic terms, energy can be specified as $E = 0.5 \times L \times I^2$.

However, as with any other parameter, due emphasis must be placed on the set of conditions against which the energy capability is specified. The value of inductance, battery voltage, external gate resistor, if any, and ambient temperature affect the energy capability specification. In addition, any resistance in line, tends to increase the available voltage across the inductor for discharge and thereby presents a smaller “effective inductance”. The datasheet curves provide extensive information on the variation in SCIS energy with these factors. The condition set and energy requirements must be considered while selecting a device for an application.

Since most applications drive the load continuously in a PWM fashion, it becomes intuitive to consider the repetitive clamp (RCL) performance of the device as well. The RCL performance is specified in terms of max current (or energy) that can be switched with a known inductor over one million cycles such that the temperature at the beginning of each cycle is equal to the ambient temperature. In other words, successive cycles do not inflict a cumulative temperature increase.

Lastly, many applications use external clamps to discharge the inductive load as shown in Figure 17. For instance, many solenoid actuators maintain a relatively constant pressure by virtue of an RMS current established by the PWM rate of the input drive. In order to prevent a fast output current discharge (attributed to a high clamp voltage), the SmartFET is shunted with a parallel diode that reduces the available voltage across the inductor to a diode drop (~0.7 V), thereby maintaining a near constant current because of the slow discharge. While employing such components in tandem with the device, their breakdown and parasitic effects must be considered so as to avoid any interference during the normal operation of the device.

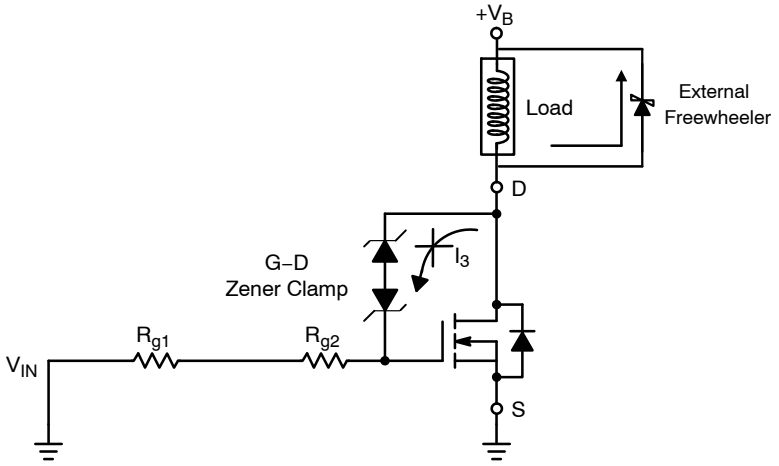


Figure 17. Application Example with External Diode for Inductive Flyback

Bulb Switching

While external lamps such as headlamp or turn signal indicator utilize high side drivers, most internal lamps such as the cabin lamp, or instrument cluster lamps are driven in low side configuration. Bulbs, or incandescent lamps are primarily capacitive in nature with a resistive element as well. The application note *AND9733* describes different types of bulb loads and their characteristics in great detail. To summarize, each bulb is characterized in terms of rated wattage at a given voltage and the inrush required at turn on. The nominal filament resistance can be calculated as:

$$R_{Nom} = \frac{V_{Nom}^2}{P_{Nom}}$$

Where P_{NOM} is the rated wattage and V_{NOM} is the specified voltage. The nominal load current can also be calculated similarly. While a nominal current signifies the load requirement in steady state operation, all bulbs also require an inrush current at turn on in order to heat the filament. Figure 18 shows the inrush profile of a 4*R10W when it is switched on by NCV8411 at an ambient temperature of −40°C.

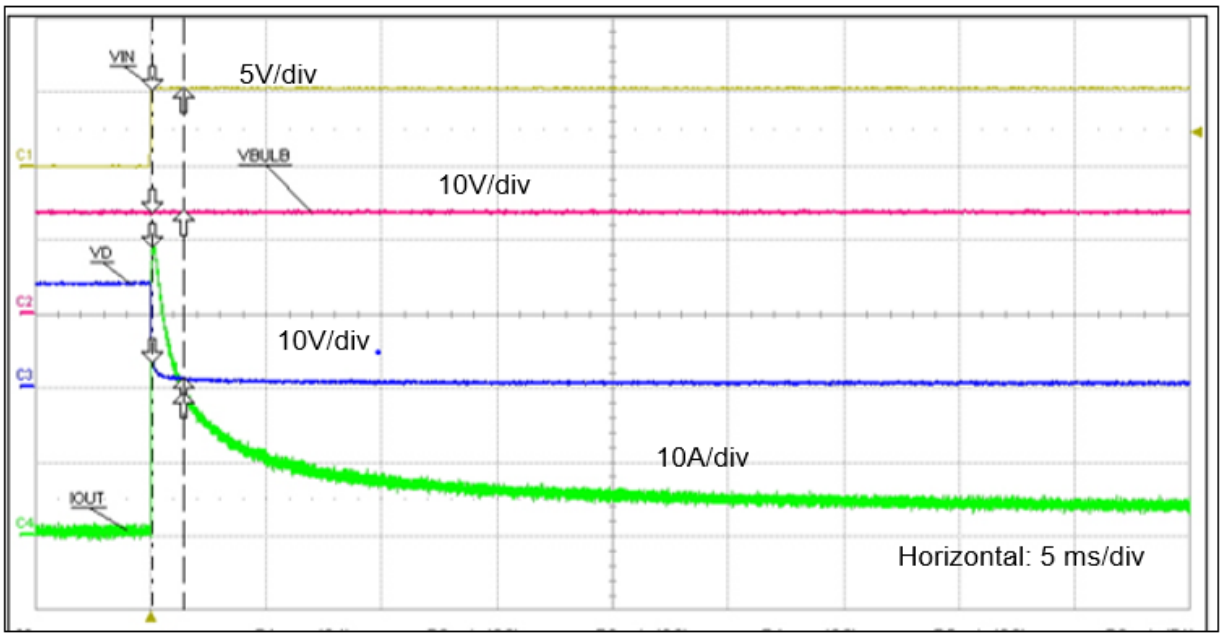


Figure 18. Inrush Profile of 4*R10W when Switched On at −40°C

It should be noted that as the bulb turns on, the filament is cold and consequently its resistance is very small which causes the current to increase. As the filament heats up, the resistance increases and load gradually reduces until it reaches a steady value. This dynamic nature of the filament resistance emulates that of a capacitor which also presents a low impedance at turn on followed by a gradual reduction of the load. The time interval during which the output current reduces to 50% of its peak value is generally termed as the inrush time and most automotive manufacturers place a maximum allowance on the inrush timing. As with any other load activation, the set of external conditions determine the inrush profile and the ability of a driver to power on a load in the required inrush time. In this case, the ambient temperature of the bulb and that of the driver, the voltage available to power on the bulb, any parasitic line resistance etc. impact the inrush profile. For example, a low ambient temperature will ensue a long inrush phase whereas a low parasitic resistance will imply that most of the supply is available for the activation of bulb load. Since these factors vary from one application to another, it becomes very challenging to select the driver for an application, especially in the absence of empirical relationships between practical bulb turn on profiles and their controlling factors.

To circumvent the challenge presented above, an idealized circuit as depicted below is utilized to characterize the inrush profile of a bulb:

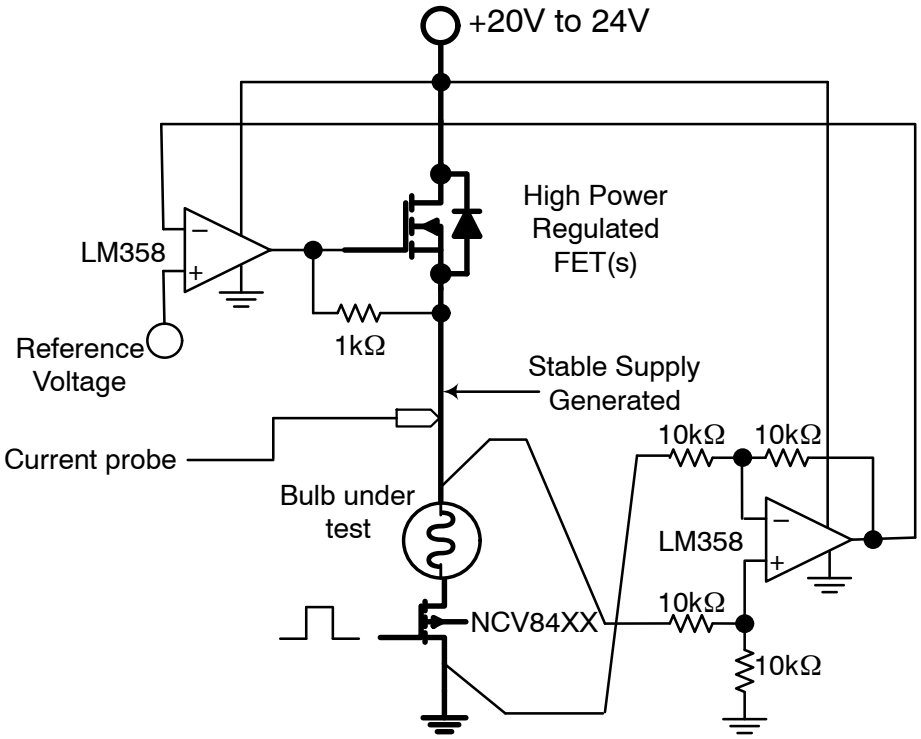


Figure 19. Idealized Circuit to measure the Inrush Profile of a Bulb against a known Driver

This circuit configuration ensures that the supply available to activate the bulb is held constant at a known reference voltage level. Further, a low line resistance constituted with short power cables provides a near ideal condition for activating the bulb. The inrush times measured with this setup are compared with the customer requirements and then used to make device recommendations corresponding to a bulb load. While this is a standard setup, **onsemi** can test the required bulbs under application conditions based on specific customer requests.

The description above is focused on the set of external conditions dominating the inrush profile without much emphasis on driver constraints. In reality, the driver characteristics also influence the inrush profile and timing to a great extent. Since an inrush event observes higher than nominal current levels, the internal current limitation of the SmartFET can be triggered during the inrush phase. If the current is regulated for an extended time then thermal shutdown may be triggered thereby forcing the output stage to shut off and subsequently retry with the thermal hysteresis. The retry strategy, although designed to protect the device, will impact the inrush timing for a given bulb load. The waveform below depicts an 8*R10W being switched on with NCV8411. The ambient temperature for the bulb is −40°C and that for the device is 25°C.

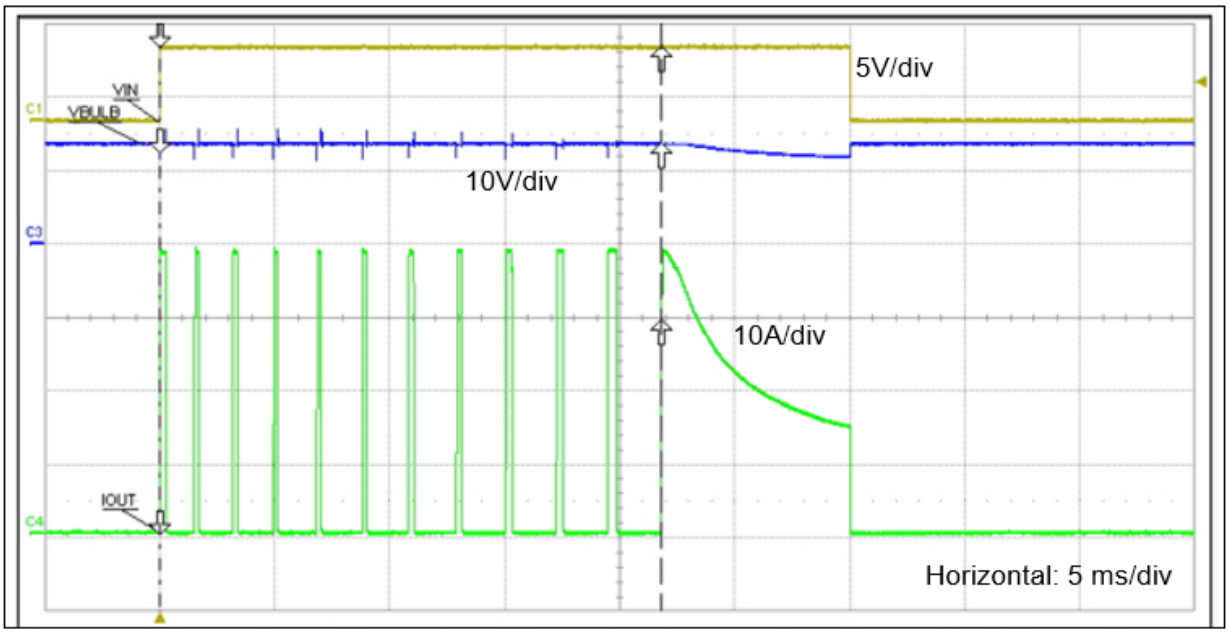


Figure 20. Inrush Profile with Retry Strategy

As can be seen in the waveform, the current is regulated at the current limit for a while after which the differential thermal shutdown intervenes and shuts off the device. The inrush time in case of retry strategy being invoked is defined as the time interval between turn on and the beginning of the last retry as highlighted by the cursors in the waveform. In NCV840X devices with no differential thermal shutdown, the device is shut off only because of absolute thermal shutdown which implies a longer time in regulation as compared to the retries in waveform above. Although an absolute TSD helps deliver more power to the load, it overstresses the device at each load activation because of the associated high temperature transient. On the other hand, the temperature sensitivity of the current limit is significantly higher in NCV840X family of devices and the current in each retry observes a steeper slope (resulting in lower power delivered per retry) as compared to the waveform above. Accounting for all these factors, the device recommendations are made while ensuring that the inrush time is within the allowed limit as well as the device is not overstressed in the application.

The last consideration with regards to a bulb load drive capability is the steady state conduction loss through the driver. As stated before, once the filaments heats up, its resistance gradually increases and reaches a steady value of R_{NOM}. The driver, in addition to satisfying the inrush requirements, should also be capable of handling the power dissipation in steady state. As with any load, a calculation of the maximum anticipated junction temperature must be made using the expected power dissipation in steady state. Since most bulb loads are operated in PWM mode with a nominal resistive load, the average power over the pulse train should be considered while doing these calculations.

Summary of Failure Modes

A summary table of potential device failure modes and mitigation strategies is shown below.

Table 4. POTENTIAL DEVICE FAILURE MODES AND MITIGATION STRATEGIES

Potential Failure Mode	Mitigation
Insufficient gate drive during fault condition	– Increase current source/sink capability of gate drive circuit – Increase gate drive voltage
Excessive dV/dt at drain	– Increase series gate resistance – Filter or snubber circuits to eliminate fast edge transients – Reduce supply voltage
Excessive die temperature during SCIS operation	– Reduce load inductance – Reduce circuit parasitic inductance – Use lower clamp voltage device – Use device with proper energy rating – Decrease device duty cycle or frequency or both – Use parallel devices
Excessive die temperature during load dump or other transient event	– Increase load resistance – Improve transient thermal response via better thermal pathway or larger silicon active area – Use parallel devices

Summary

The low-side device family offers an efficient monolithic solution to integrating protection features with vertical power MOSFET technology. The operation and application of these devices is the same as standard MOSFETs, assuming the gate drive circuit design allows for fault operation modes as described in this application note. Moreover, while designing an application, it is important to consider the mitigation mechanisms described above to avoid over−stressing the SmartFET.

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