NCD(V)57000/57001 Gate Driver Design Note

AND9949/D

Introduction

The NCD(V)5700x is a high−current single channel gate driver with internal galvanic isolation, designed for high system efficiency and reliability in high power applications. Its features include complementary inputs (IN+ and IN−), open drain fault ($\overline{FLT}$) and ready (RDY) outputs, reset or clear fault function ($\overline{RST}$), active miller clamp (CLAMP), de−saturation protection (DESAT), soft turn−off at de−saturation condition, separate source (OUTH) and sink (OUTL) driving outputs (for NCD(V)57000 only), accurate under voltage lock−out (UVLO), low propagation delay 90 ns (Max.) and small pulse distortion 25 ns (Max.), higher common mode transient immunity (CMTI) withstand 100kV/us (Min.) at V_{CM} = 1500 V condition, input signal range covering both 5 V and 3.3 V, output differential biasvoltage (*VDD2 − VEE2*) up to 25 V (Max.), with VDD2 rated to 25 V (Max.) and VEE2 rated to negative 10 V (Max). The NCD(V)5700x provides 5 kVrms galvanic isolation and 1.2 kV working voltage capabilities at least with guaranteed 8 mm creepage distance between input and output. The wide−body SOIC−16 package fulfills reinforced safety insulation requirement.

This application note describes some parameters, functions, and design tips of NCD(V)5700x in system application.

Input (IN) and Output (OUT) Signal

The relation between complementary input logic signals and output is shown in Table 1.

Table 1. INPUT AND OUTPUT SIGNAL LOGIC

		57000		57001
IN+	IN−	OUTH	OUTL	OUT
Low	Low	Hi−Z	Low	Low
Low	High	Hi−Z	Low	Low
High	Low	High	Hi−Z	High
High	High	Hi−Z	Low	Low
Low	X			
High	X			
X	High			
X	Low			
X	X			

NOTES: X: Floating, Internal pull−down 50 kΩ resistor lets IN+ go to GND1, and internal pull−up 50 kΩ resistor lets IN− go to VDD1.
Hi−Z: High impedance state.

The input logic signal block diagram shows in Figure 1.

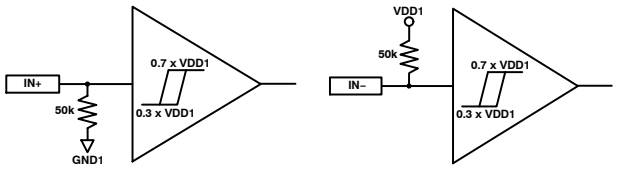


Figure 1. Input Logic Signal Block Diagram

In order to have good signal quality and noise immunity, an input filter RC network could be placed between microcontroller and gate driver inputs (IN+, IN−,$\overline{RST}$). The RC value will depend on input frequency range, duty cycle, and time delay according to system requirement. The application circuit for this RC filter shows in Figure 2. This RC filter needs to place the gate driver pin lead as near as possible. The common mode transient noise can be interfering from high voltage output circuit to the low voltage input side. The input digital control inputs should have low impedance signal source to prevent the glitch or unexpected switching. The standard CMOS or push−pull drive circuit is preferred, the open−drain configuration was avoided.

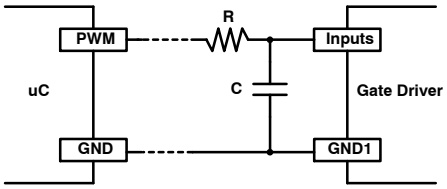


Figure 2. RC Filter Network for Input Signals

Based on the Table 1, the function of inverting input (IN−) can be used for input signal enable/disable when the PWM signal is applied to non−inverting input (IN+). The example circuit of signal enable/disable is shown in Figure 3.

This configuration is to control the output signal only, not reset function for any protections (UVLO and De−saturation) and output follows the non−inverting signal.

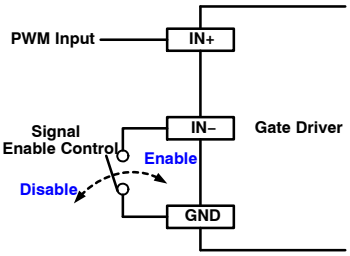


Figure 3. Signal Enable Control by Inverting Input (IN−)

Input Bias Supply (VDD1)

The series resistor and de−coupling capacitor have to be placed between VDD1 and GND1. The capacitor needs to be as close as possible to the gate driver pin leads to filter out any high frequency noise and sustain input bias voltage. In general, low ESL and ESR chip capacitors (MLCC) of value 0.1 μF and 2.2 μF are placed as shown in Figure 4. The typical input bias operation supply currents for 5.0 V and 3.3 V conditions are shown in Figure 5 and power demand can be estimated when 5.0 V or 3.3 V supplied.

Output Positive and Negative Bias Supply (VDD2 and VEE2)

The NCD5700x series has high source and sink current capability. This requires extra layout precautions especially when external gate resistance value is small. High peak current transient will be present due to internal power MOSFETs turning−on. The de−coupling capacitors that have to be placed between VDD2, VEE2 and GND2 need to be as close as possible to the driver pin leads to prevent bias voltage over and under shoot due to the parasitic inductance from PCB trace and package. The major current demand comes from external load capacitance, and hence the peak current depends on external gate resistance. In general application, the 10 μF capacitor per each of positive (VDD2) and negative (VEE2) bias are required when the gate resistance value is large than 10 Ω. When the gate resistance is small than 10 Ω, the 20 μF capacitor is suggested. Of course, low ESL and ESR chip capacitors (MLCC) are preferred. The example circuit is shown in Figure 6. The typical output bias operation supply currents function of input frequency, ambient temperature, and load capacitance are shown in Figure 7, Figure 8 and Figure 9 accordingly.

Note that these curves represent the extreme switching condition with external age resistance only at 1 Ω. Most applications will use higher value of gate resistance and hence, the currents will be lower than those depicted in these curves. The power demand can be estimated for positive and negative bias supply.

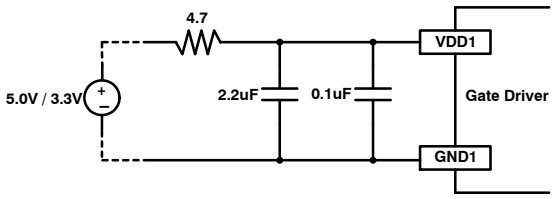


Figure 4. De−coupling Capacitors for Input Supply Bias (VDD1)

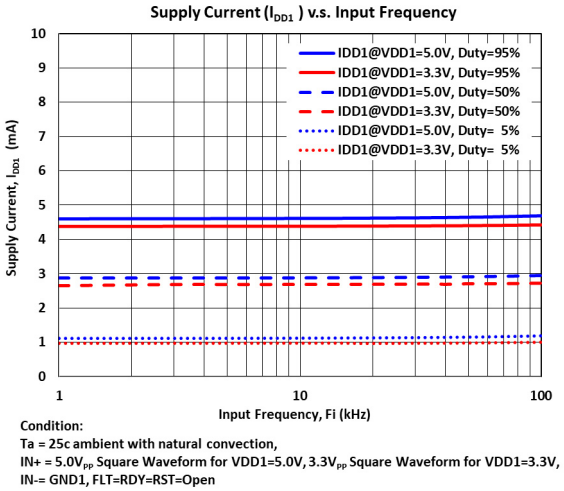


Figure 5. Input Supply Current (I_{DD1}) v.s. Input Frequency

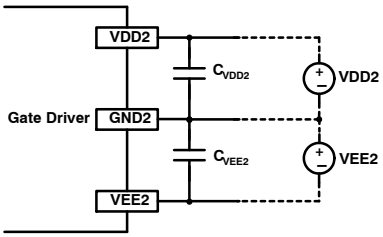


Figure 6. De−coupling Capacitors for Output Supply Bias (VDD2 and VEE2)

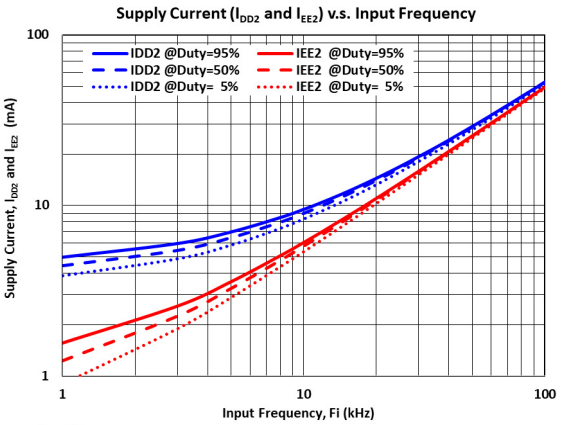


Figure 7. Output Supply Current (I_{DD2} and I_{EE2}) v.s. Input Frequency

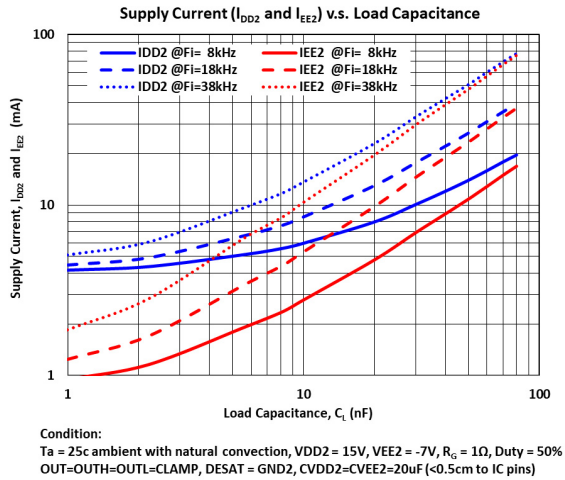


Figure 8. Output Supply Current (I_{DD2} and I_{EE2}) v.s. Load Capacitance

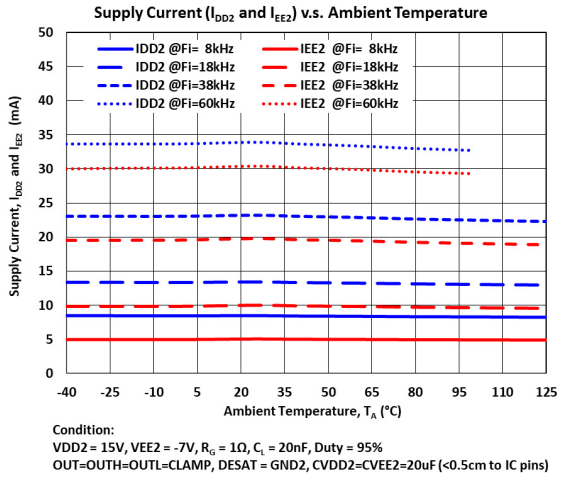


Figure 9. Output Supply Current (I_{DD2} and I_{EE2}) v.s. Ambient Temperature

Power Consumption (P_D) and Junction Temperature (T_J)

It is important to review the power dissipation of gate driver when the external gate resistance and supply bias value fixed. The design has to make sure that the device maximum junction temperature is not exceeded while the device operates within desired temperature range. The power dissipation equation of gate driver can be descripted as below.

$$P_{D-total} = P_{D-input} + P_{D-output} \quad \text{(eq. 1)}$$

Where:

$P_{D-total}$ is total device power dissipation (W)

$P_{D-input}$ is input bias (VDD1) power dissipation (W)

$P_{D-output}$ is output bias (VDD2, VEE2) power dissipation (W)

For calculation of the input bias power dissipation ($P_{D-input}$), the input supply current values provided in Figure 5 or the maximum bias current in datasheet can be used. The equation is

$$P_{D-input} = VDD1 \times IDD1 \quad \text{(eq. 2)}$$

The block diagram in Figure 10 shows the output bias power delivery path. For calculation of the output bias power dissipation ($P_{D-output}$), two factors must be considered. First is the essential operation power demand for the internal logic circuit and junction capacitance charging/discharge loss of source/sink power MOSFETs. This can be measured by no−load condition which shown in Figure 11 with specific VDD2 and VEE2 voltage bias condition. Second is power dissipation of the output bias is dividing between the equivalent on−resistance of internal source/sink power MOSFETs and external gate resistance when output drives the load condition.

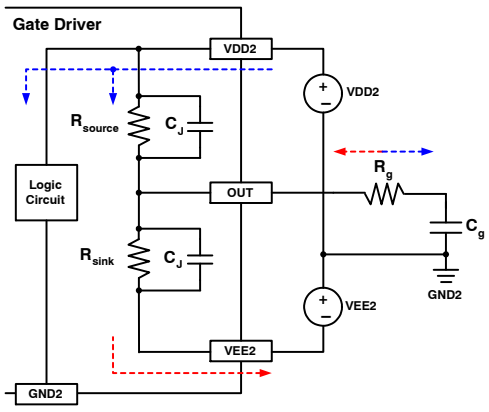


Figure 10. Power Delivery Path for Output Bias

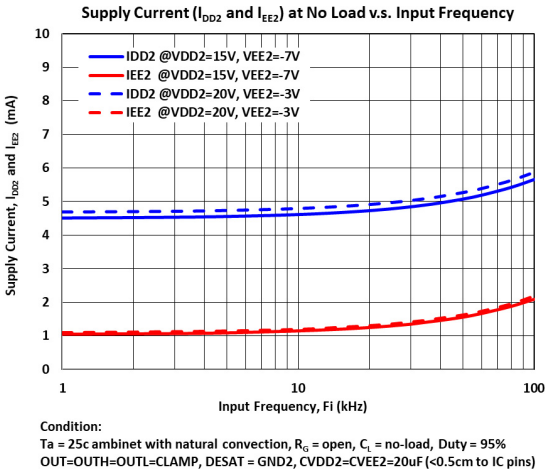


Figure 11. Output Supply Current (IDD2, IEE2) at No−load v.s. Input Frequency

The equation of $P_{D-output}$ is

$$P_{D-output} = \left(P_{D-output}\right)_{no-load} + \left(P_{D-output}\right)_{load} \quad \text{(eq. 3)}$$

Where:

$$\left(P_{D-output}\right)_{no-load} = (VDD2 \times IDD2)_{no-load} + (VEE2 \times IEE2)_{no-load}$$

$$\left(P_{D-output}\right)_{load} = \frac{1}{2} \times F_i \times Q_g \times (VDD2 + VEE2) \times \left(\frac{R_{source}}{R_{source} + R_g} + \frac{R_{sink}}{R_{sink} + R_g}\right)$$

F_i = Input Frequency
Q_g = Gate Charge
R_{source} = Internal Source MOSFET On Resistance ≅ 1Ω
R_{sink} = Internal Sink MOSFET On Resistance ≅ 1Ω
R_g = External Gate Resistance

The junction temperature can be estimated by

$$T_J = P_{D-total} \times R_{th(JA)} + T_A \quad \text{(eq. 4)}$$

Where:

$R_{th(JA)}$ = Junction to Ambient Thermal Resistance
T_A = Ambient Temperatur
$T_{th(JA)}$ = 150°C/W at 100 mm^2, 1 oz Copper, 1 Surface Layer
$T_{th(JA)}$ = 84°C/W at 650 mm^2, 1 oz Copper, 1 Surface Layer and 2 Internal Power Plane Layers

(Eq. 4) can also be used to compute the maximum allowable power dissipation (P_D) with ambient temperature (T_A) when maximum junction temperature, $T_{J(MAX)}$, is 150°C. Figure 12 shows this power de−rating curve when the junction to ambient thermal resistance, of NCD(V)5700x series based on specific PCB layout, layer, and surface area.

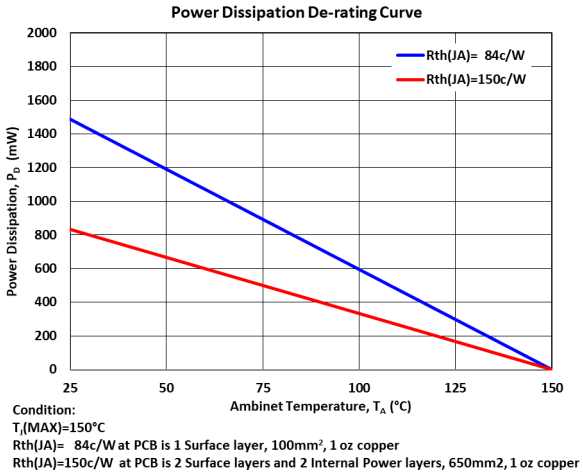


Figure 12. Power Dissipation de−rating Curve of NCD(V) 5700x Series

Under Voltage Lockout (UVLO) and READY (RDY)

To ensure the correct voltage in driving operation, the input (VDD1) and output (VDD2) bias supply is monitored by under voltage non−latch protection. When UVLO protection is tripped, the output signal logic will be low immediately with less prorogation delay. The power good (READY) signal on RDY pin indicates this UVLOs event only and may has 8 μs (Typ.) delay time. The RDY pin output interface is an internal open drain with pull−up 50 kΩ resistor to VDD1. The block diagram of Figure 13 shows the UVLO and RDY function. The detail timing chart is shown in datasheet already. Figures 14 and Figure 15 show that the RDY is related to under voltage lockout protection only.

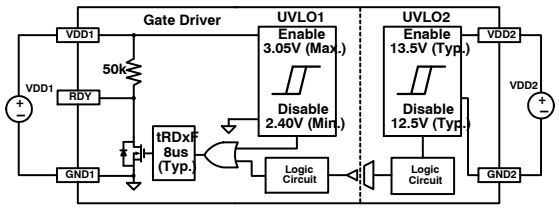


Figure 13. UVLOs and RDY Functional Block Diagram of NCD(V) 5700x Series

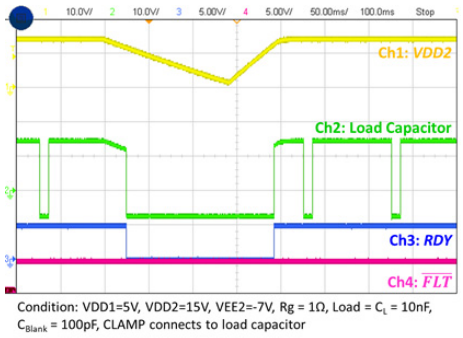


Figure 14. RDY Waveform When UVLO2 Triggered for NCD(V) 5700x Series

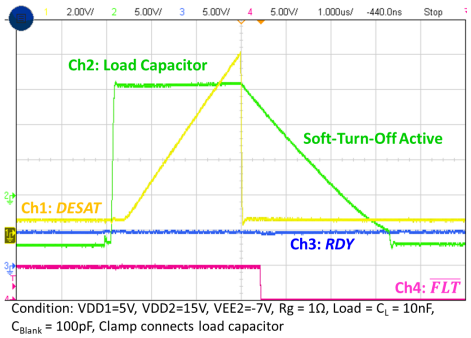


Figure 15. FAULT Waveform When DESAT Protection Triggered for NCD(V) 5700x Series

De−Saturation (DESAT) Protection and Soft−Turn−Off (STO)

In order to prevent the power semiconductor device from dissipating too much power of over current or short circuit event, the De−saturation protection function is an effective and low cost method to implement into gate driver. By using power device forward characteristic property, it can be detected when the high device current results in higher saturation voltage or transition into active region in bipolar device or saturation region in unipolar device. In turning off during over current condition, high *di*/*dt* occurs if the gate voltage is turned off rapidly as in normal switching operation. In conjunction with the parasitic loop inductance in the power path, this produces higher turn−off *dV*/*dt* that can lead to overvoltage stress and potentially damage the switch. The Soft−Turn−Off (STO) feature can reduce the stress on the power device when DESAT protection tripped. The extra MOSFET (STO) with lower sink current capability in gate driver will be active in place of the normal turn−off transistor with high sink current capability. The gate discharge current is reduced and the gate voltage is turned−off slowly, in lower turning−off *di*/*dt* and *dV*/*dt*. The STO function does not impact the switching loss in normal operation. The typical saturation current for sink MOSFET and Soft−Turn−Off MOSFET are shown in Figure 16 (sink MOSFET, Q_{Sink}) and Figure 17 (Soft−Turn−Off MOSFET, Q_{STO}). Therefore, Figure 15 shows load capacitor voltage falling down slowly when STO is active. Figure 18 is a block diagram of De−Saturation Protection with Soft−Turn−Off and detail timing chart is shown in the datasheet.

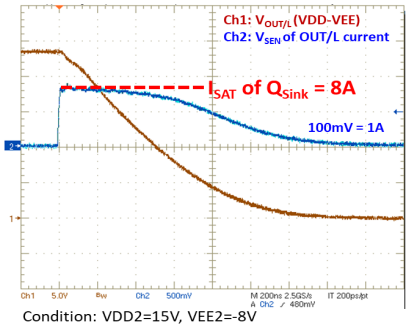


Figure 16. Typical Saturation Current of Internal Sink MOSFET (Q_{sink})

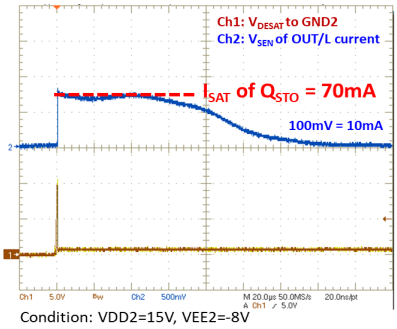


Figure 17. Typical Saturation Current of Internal Soft−Turn−Off MOSFET (Q_{STO})

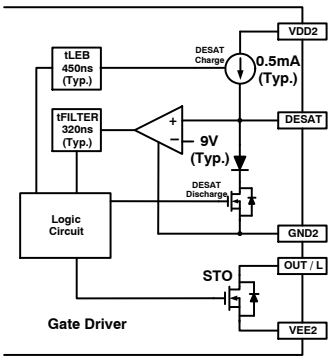


Figure 18. De−Saturation Protection Diagram for NCD(V) 5700x Series

The DESAT protection circuit still needs to avoid false triggering for short transient time of power device turning−on to allow the Collector/Drain voltage falling below the DESAT threshold. This transient time duration is named "DESAT Blanking Time (t_{Blank})". The blanking time is controlled by the internal constant charge current source ($I_{DESAT-CHG}$), the DESAT threshold voltage ($V_{DESAT-THR}$), and the external blanking capacitor (C_B). The blanking capacitor discharged by DESAT discharge MOSFET when the input signals is active to let output low and then the blanking time is reset for next turning−on cycle. The typical application circuit is shown in Figure 19.

The blanking time equation is shown in (Eq. 5) which includes leading edge blanking and the blanking time function of blanking capacitance is plotted in Figure 20.

$$t_{Blank} = \frac{C_B \times (V_{DESAT-THR} - V_{D-OFFSET})}{I_{DESAT-CHG}} + t_{LEB} \quad \text{(eq. 5)}$$

Where:

$V_{DESAT-THR}$ = 9 V (Typ.)
$V_{D-OFFSET}$ = 0.7 V (Typ.)
$I_{DESAT-CHG}$ = 0.5 mA (Typ.)
$tLEB$ = 450 ns (Typ.)

In steady state, the voltage at DESAT to GND2 is sum of the voltage across resistor (R_{DESAT}), forward voltage of diode (D_{DESAT}), and saturation voltage of power device (V_{CE-SAT}). The tripped threshold of saturation voltage for power device ($V_{CE-SAT-THR}$) can be arranged as

$$V_{CE-SAT-THR} = V_{DESAT-THR} - (I_{DESAT-CHG} \times R_{DESAT}) - V_{F-DESAT} \quad \text{(eq. 6)}$$

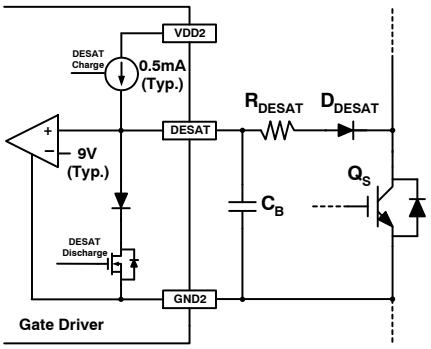


Figure 19. Typical De−Saturation Protection Application Circuit

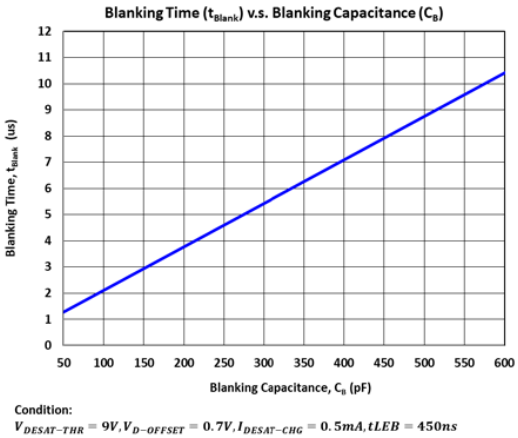


Figure 20. Blanking Time (t_{Blank}) as a Function of Blanking Capacitance (C_B) for NCD(V) 5700x Series

The DESAT protection may have false trigger or unexpected current trip out of calculation value by some parasitic elements in this sensing loop. Figure 21 shows the junction capacitor of de−saturation block diode ($C_{J-DESAT}$) and parasitic inductor (L_k) in power loop which needs to consider in the circuit when DESAT protection applied.

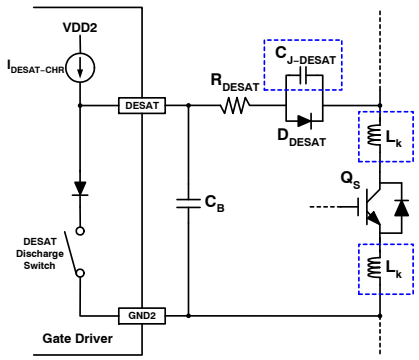


Figure 21. Consider Parasitic Elements in De−Saturation Protection Circuit

The mechanism of negative voltage on DESAT is caused primarily by the discharge of $C_{J-DESAT}$. The principal of this negative voltage is shown in Figure 22. In Q_S switch off−state, the voltage of D_{DESAT} junction capacitance ($C_{J-DESAT}$) is near to BUS voltage, because the DESAT discharge switch is turned on to let D_{DESAT} withstand the BUS voltage. The junction capacitance has a stored energy $E_{CJ-DESAT}$ = 1/2 $C_{J-DESAT}$ $V_{BUS}{}^2$. When Q_S is turned−on, $C_{J-DESAT}$ is discharged and its energy is transferred to the blanking capacitor C_B, resulting in negative voltage across C_B. If the junction capacitance has higher value than the blanking capacitor, the negative voltage of blanking capacitor will be higher due to more energy coming from the junction capacitance. This negative voltage will be recovered quickly by $I_{DESAT-CHG}$ current source until goes to positive voltage and follows the saturation voltage of IGBT. It may add extra time delay for De−saturation trip function that causes the higher short circuit peak current of IGBT, if not accounted for by adjusting the blanking capacitor value. Figure 23 shows the simulation result of DESAT voltage with reference to GND2. The NCD(V)5700x series DESAT pin has been designed to withstand up to −9 V negative voltage without damaging the IC.

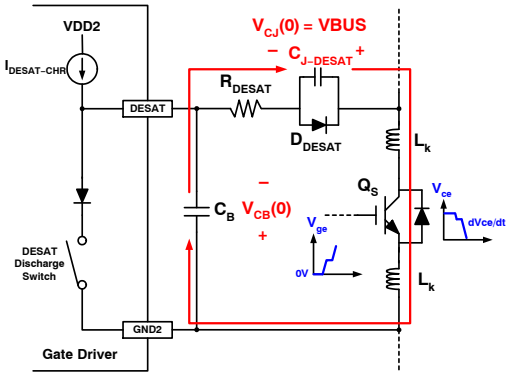


Figure 22. When the Q_S Turning−on and DESAT Discharge Switch Turned−off

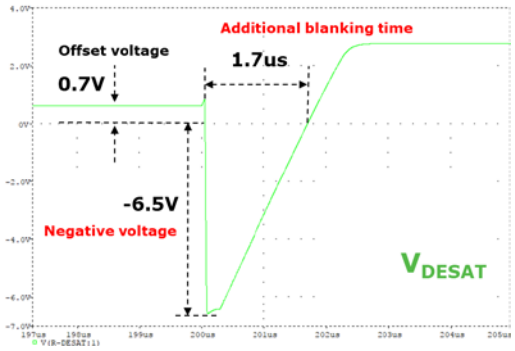


Figure 23. DESAT Waveform (Simulated) during Q_S Turn−on

If an external negative voltage protection is desired, a protection diode D_p can be paralleled with blanking capacitor. This diode can limit the negative voltage and the time delay can be improved. Figures 24 and Figure 25 are shown the circuit and simulation result with protection diode. Based on this analysis, the De−Saturation block diode (D_{DESAT}) should have a low junction capacitance value and fast reverse recovery performance. The protection diode (D_p) should have a low forward voltage and low leakage current. Suggested diodes for D_{DESAT} and D_p are listed in Table 2 and Table 3.

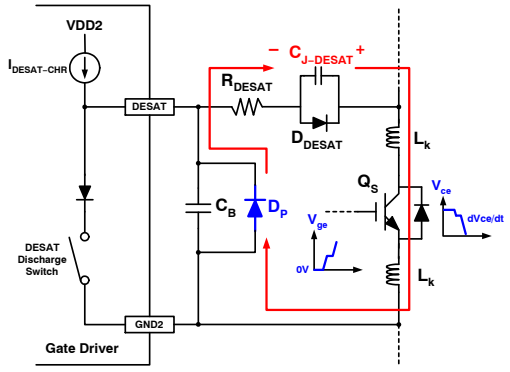


Figure 24. With the Protection Diode (D_p) between DESAT and GND2

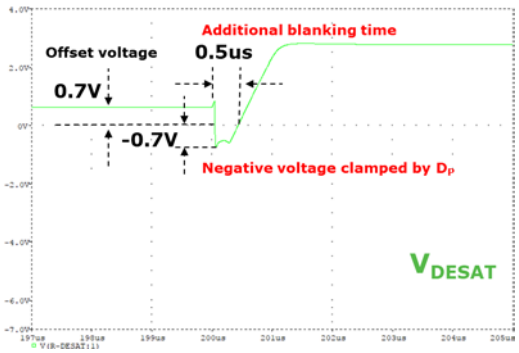


Figure 25. DESAT Waveform (Simulated) with Protection Diode during Q_S Turn−on

Table 2. DE−SATURATION PROTECTION BLOCK DIODE (*D−DESAT*)

Part Number	V_{RRM}(V)	$I_{F(AV)}$ (A)	T_{RR} (ns)	Packge
NHP160SF	600	1	50	SOD123−FL
ES1JAF	600	1	35	SMA−FL
US2KA	800	1.5	75	SMA
US2MA	1000	1.5	75	SMA

Table 3. PROTECTION DIODE (D_p)

Part Number	V_{RRM}(V)	$I_{F(AV)}$ (A)	I_R (μA)	Packge
NHP120SF	200	1	10	SOD123−FL
MBR1H100SF	100	1	250	SOD123−FL
NRVBSS13HE	60	1	300	SOD323−HE

NOTE: The leakage current at VR < 20 V, Ta = 125°C or 150°C

When the protection diode is placed, the impact of extra junction capacitance and leakage current on blanking time needs to be considered. The power path parasitic inductance will produce high frequency voltage (V_{Lk}) based on the $-dI_c/dt$ coming at the condition of reverse recovery current of power rectifier or IGBT turning−off. This high frequency noise could inject into gate driver via the De−Saturation pin and GND2. The De−Saturation resistor (R_{DESAT}) can suppress this to let this noise current goes to power loop, not into sensing loop if the resistance value large enough. In general, around 1 kΩ and 2.2 Ω for R_{DESAT} are suggested. It also can have two De−Saturation block diodes to reduce the total junction capacitance if the higher dV_{CE}/dt or dVds/dt are created by using fast switching speed power devices. Certainly, the tripped threshold voltage will be changed if the resultant forward voltage on the De−Saturation block diodes and De−Saturation resistor is higher. The suggestion application circuit is shown in Figure 26.

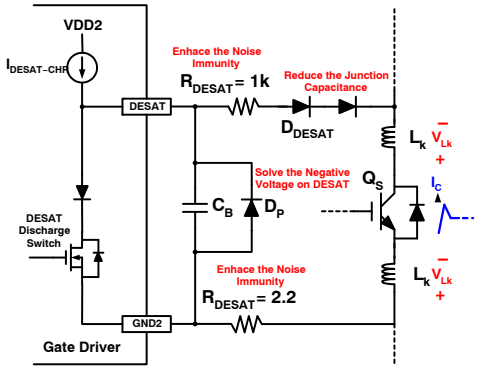


Figure 26. Suggested Application Circuit for Improved De−Saturation Protection

The ideal diagram of DESAT voltage waveform and blanking time design concept is shown in Figure 27. The sum of blanking and filter time has to be less than the short circuit capability duration time of power device that prevent to stress the reliability life time, and blanking time should be more than power device's collector/drain voltage falling down duration in normal operation to prevent any false triggered.

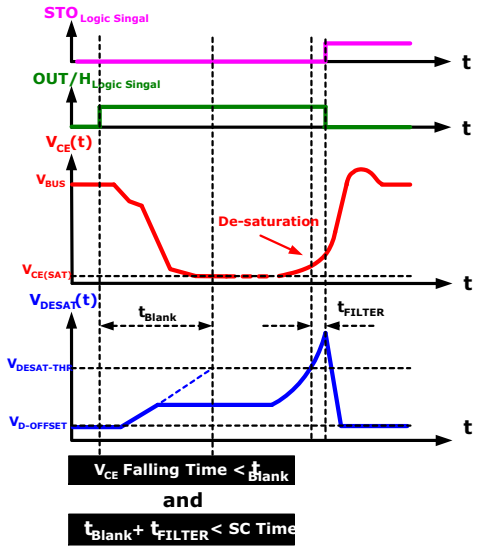


Figure 27. De−Saturation Waveform (V_{DESAT}) Diagram and Blanking Time Design Concept

Considering the Soft−Turn−Off (STO) with External BJT Buffer

The external BJT buffer for boosting the drive current is used widely to drive higher current power semiconductor devices with large gate charges. In order to have higher driving current from buffer, the DC gain of BJT needs to be high. In addition, high base current is provided for the buffer by use of lower value base resistor (R_B). A typical application circuit is shown in Figure 28 which includes the internal power switch and the STO switch. While lower base resistor value helps achieve higher drive current, it still needs to be high enough to limit the base current in Desaturation condition. In this trade off, the Soft−Turn−Off may not be able to suppress the overvoltage spike sufficiently during the short circuit condition. Figure 29 shows the current path in normal operation and Soft−Turn−Off when DESAT active.

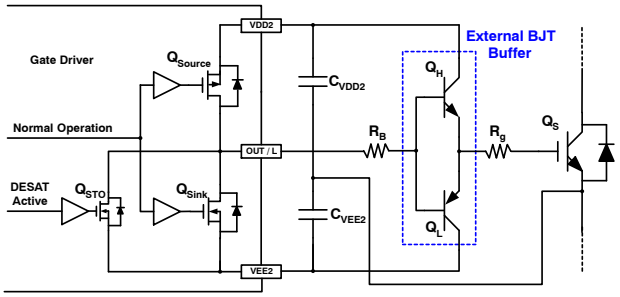


Figure 28. Typical Application Circuit of External BJT Buffer

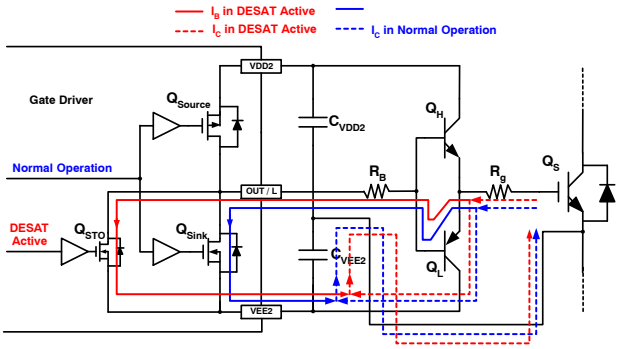


Figure 29. Sinking Current Path for Normal Operation and DESAT Active

In order to reduce the base current, an extra RC network can produce a voltage between the base resistor and OUT/L node. This extra voltage node can reduce the base current in DESAT condition and prevent the PNP BJT (Q_L) from going to hard saturation and allowing it to turn−on slowly. The schematic of extra RC network is shown in Figure 30. The approximate equation of voltage and current can be written as below.

$$V_x(t) \approx V_{CEX}(0) \cdot e^{\frac{-t}{(R_{EX}+R_{STO})\cdot C_{EX}}} \cdot \frac{R_{STO}}{R_{STO}+R_{EX}} \quad \text{(eq. 7)}$$

$$I_B(t) \approx \frac{V_{Cies}(0) - V_{BE} - V_x(t) - (-VEE2)}{R_g(\beta+1) + R_B + R_{STO}} \quad \text{(eq. 8)}$$

While

$R_{EX} << R_B$ and R_{STO}

RSTO = Internal STO MOSFET On Resistance
$\cong 200\Omega$

$V_{cies}(0) \approx V_{x(t)} \approx$ VDD2

Considering the BJT operates in Active Mode Region

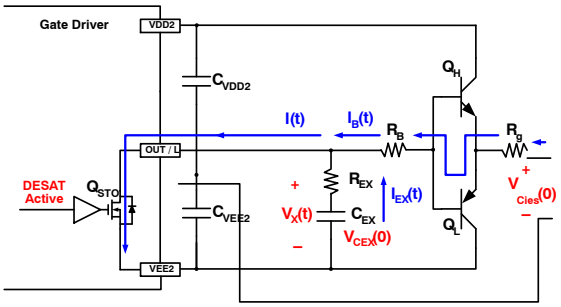


Figure 30. Typical Application Circuit of External BJT Buffer

The R_{EX} is derived considering the current stress of source/sink MOSFET in gate driver IC. It needs to be a compromise between current stress and $V_x(t)$. Usually, the R_{EX} value should be less R_B or equal to R_B. The C_{EX} value is derived considering the power dissipation of R_{EX} and still needs to have enough time constant that lets $V_x(t)$ decay slowly. If C_{EX} is higher, the Soft−Turn−Off (STO) will be achieved more easily. In general, the R_{EX} will be fixed then let C_{EX} be adjustable to make IGBT soft turning−off in short circuit condition.

The example circuit with extra RC network (R_{EX} and C_{EX}) with external BJT buffer is shown in Figure 31. The comparison waveforms are shown in Figure 32 (without the RC network) and Figure 33 (with RC network). These RC waveforms demonstrate of the RC network has the effect of producing a Soft−Turn−Off waveform at the IGBT gate in DESAT condition. The RC network should be designed so that there is no impact on the driving in normal operation. Figure 34 and Figure 35 show that with the chosen value of R_{EX} and C_{EX}, the RC network doesn't affect the turning−on rise time, Figure 36 and Figure 37 show the same outcome for turning−off fall time.

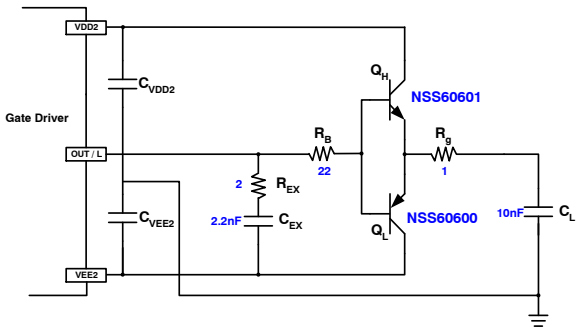
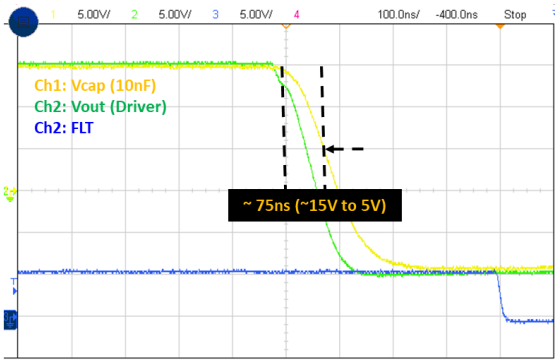
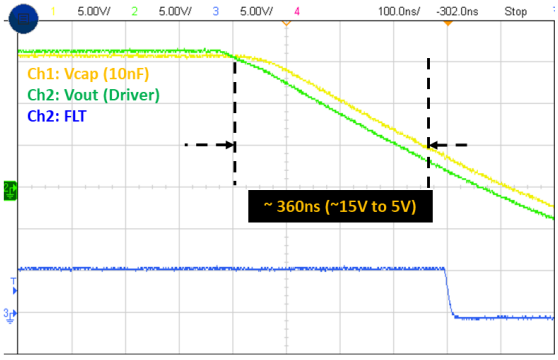


Figure 31. Typical Application Circuit of External BJT Buffer



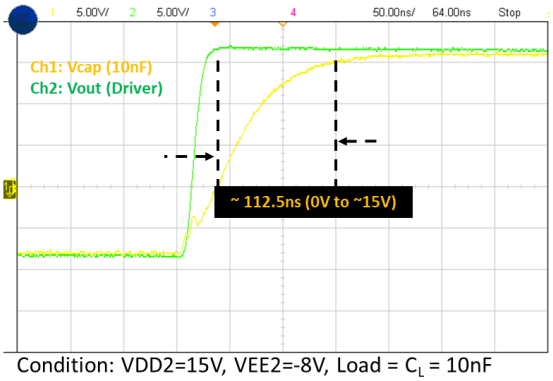
Condition: VDD2=15V, VEE2=-8V, Load = C_L = 10nF

Figure 32. Output and Load Voltage Waveforms without RC Network when DESAT Active



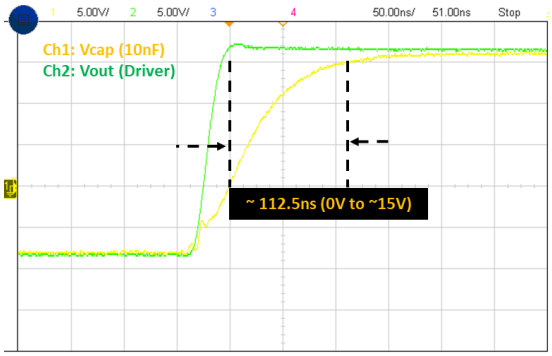
Condition: VDD2=15V, VEE2=-8V, Load = C_L = 10nF, R_{EX} = 2Ω, C_{EX} = 2.2nF

Figure 33. Output and Load Voltage Waveforms with RC Network when DESAT Active



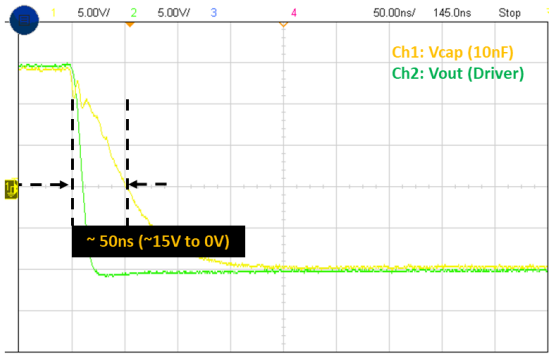
Condition: VDD2=15V, VEE2=-8V, Load = C_L = 10nF

Figure 34. Output and Load Voltage Waveforms without RC Network at Turning−On



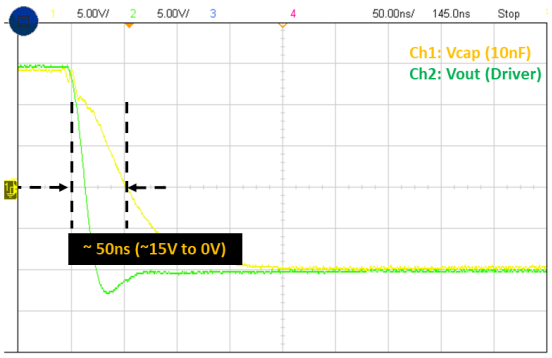
Condition: VDD2=15V, VEE2=-8V, Load = C_L = 10nF, R_{EX} = 2Ω, C_{EX} = 2.2nF

Figure 35. Output and Load Voltage Waveform with RC Network at Turning−On



Condition: VDD2=15V, VEE2=-8V, Load = C_L = 10nF

Figure 36. Output and Load Voltage Waveform without RC Network at Turning−Off



Condition: VDD2=15V, VEE2=-8V, Load = C_L = 10nF, R_{EX} = 2Ω, C_{EX} = 2.2nF

Figure 37. Output and Load Voltage Waveform with RC Network at Turning−Off

Zener Split Voltage Regulator for Bias Supply

The Zener Split Voltage Regulator is widely used in applications as a cost effective solution for biasing the gate drivers because it reduces the winding in transformer and reduce components. It can generate positive and negative bias voltage from unipolar voltage for driver bias requirements (which include negative bias VEE2). Figure 38 shows a typical schematic of an isolation converter output with Zener Split Voltage Regulator.

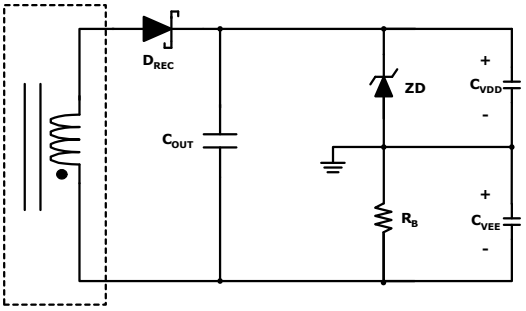


Figure 38. Typical Circuit of Zener Split Voltage Regulator

The positive bias supplies the VDD2 and negative bias supplies the VEE2 of gate driver. The VDD2 voltage is clamped by Zener breakdown voltage of Zener diode and VEE2 voltage will be remaining from total DC output voltage. According to this, the Zener diode has to breakdown to sustain the positive voltage of VDD2 upon all of loading current range, otherwise the positive and negative voltage cannot be sustained as expectation and swing up and down that results UVLO tripped in risk. The equivalent circuit is shown in Figure 39.

The positive and negative bias supply current (I_{DD2} *and* I_{EE2}) of NCD(V)5700x series has already shown in Figure 7 and Figure 8 with difference input signal frequency and load capacitance. It can be converted to equivalent load resistance for positive and negative bias $R_{L(VDD2)}$, $R_{L(VEE2)}$. In order to make sure the Zener diode breakdown, the bias resistance will be equal as below equation.

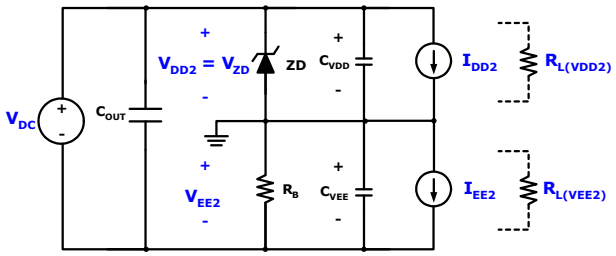


Figure 39. The Equivalent Circuit of Zener Split Voltage Regulator

$$R_B < \frac{R_{L(VDD2)} \cdot R_{L(VEE2)} \cdot (V_{ZD} - V_{DC})}{V_{DC} \cdot R_{L(VDD2)} - V_{ZD} \cdot (R_{L(VDD2)} + R_{L(VEE2)})} \quad \text{(eq. 9)}$$

While

$R_{L(VDD2)}$ = equalvent load resistance of VDD2

$R_{L(VEE2)}$ = equalvent load resistance of VEE2

$V_{DC} = V_{DD2} + V_{EE2}$

$$P_{ZD} > V_{DD2} \times \frac{V_{EE2}}{R_B} \quad \text{(eq. 10)}$$

$$P_{RB} > \frac{(V_{EE2})2}{R_B} \qquad \text{(eq. 11)}$$

Zener voltage (V_{ZD}) of Zener diode needs to consider the tolerance shift with temperature. The maximum DC Zener current (I_{ZM}) should be concerned when bias resistance R_B determined. The power dissipation limited of Zener Diode and R_B must be considered. The device tolerance should be considered to sustain the $V_{DD2} > V_{ZD}$ enough. The power rating of Zener Diode and bias resistance can be knew and the recommendation of Zener Diode shown in Table 4.

Table 4. ZENER DIODE (*ZD*)

Part Number	V_{ZD}(V)	P_D (W)	I_{ZM} (mA)	Packge
1SMA5929B	15.0	1.5	100	SMA
1SMB5929B	15.0	3	100	SMB
1N5352B	15.0	5	315	Axial−Lead
1SMA5930B	16.0	1.5	94	SMA
1SMB5930B	16.0	3	93	SMB
1N5353B	16.0	5	295	Axial−Lead
1SMA5932B	20.0	1.5	75	SMA
1SMB5932B	20.0	3	75	SMB
1N5357B	20.0	5	237	Axial−Lead
1SMA5933B	22.0	1.5	68	SMA
1SMB5933B	22.0	3	68	SMB
1N5358B	22.0	5	216	Axial−Lead

NOTE: The Zener breakdown is typical value and defined at room temperature.

Clamping Diode in Gate Driving Circuit

The parasitic inductance in power loop and driving loop is not easy to avoid due to layout placement and device package. The higher *di*/*dt* will be occurred no matter in driving loop by higher peak driving current or in power loop by power device current. This higher *di*/*dt* will produce higher *dv*/*dt* by parasitic inductance (L_k) and this fast transient voltage could be higher positive bias (V_{DD2}) or lower than negative bias (V_{EE2}) that results in the high frequency circuiting current into gate driver. The high frequency circuiting current path shows in Figure 40 if positive *di*/*dt* comes and Figure 41 if negative *di*/*dt* comes. The suggestion of clamping diode was added as shown in Figure 42. The high frequency circuiting current can pass through to bias capacitor directly, not go to gate driver. Besides, the positive clamping diode ($D_{C(VDD2)}$) can sustain that gate voltage of IGBT equals bias voltage to prevent the gate voltage rise−up and results in higher peak short circuit current in short circuit condition.

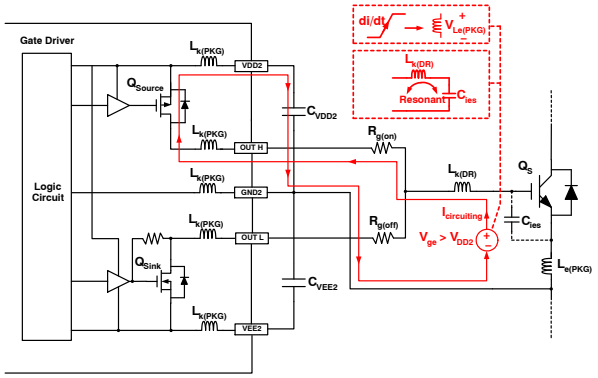


Figure 40. The Circuiting Current Path in Positive *di/dt*

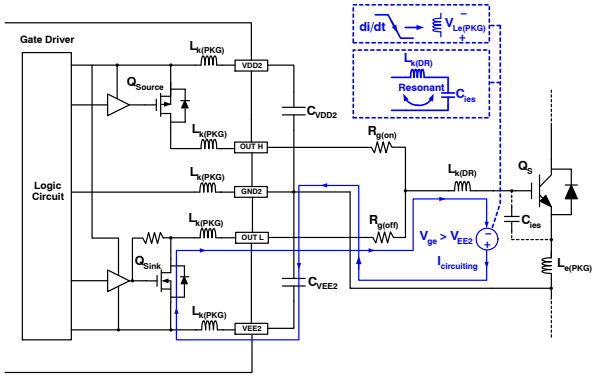


Figure 41. The Circuiting Current Path in Negative *di/dt*

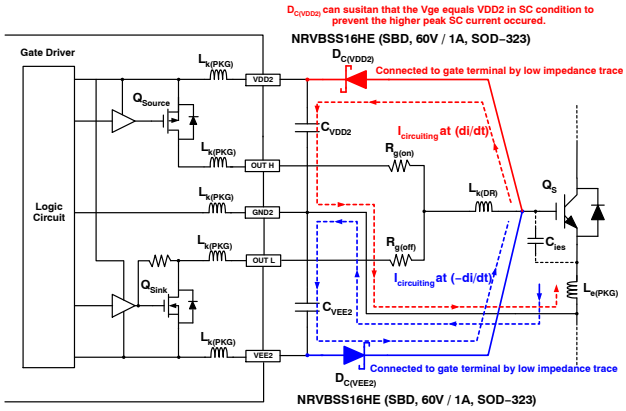


Figure 42. The Circuiting Current Path in Negative *di/dt*

Layout and Placement Consideration

In order to has good noise immunity and stable operation, the layout and placement have to consider in application when using gate driver. The driving current path of

turning−on and turning−off are shown in Figure 43. It shows the major driving loop from gate driver to power device. The driving loop should as small as possible and lower impedance to reduce stray inductance of the loop. This high driving current path is via the bias capacitors and internal MOSFET to IGBT gate only. The bias capacitor needs to be placed as near *VDD2* and *VEE2* of gate driver pin lead. The return path has a low impedance trace or plane to connect emitter of IGBT.

Considering a good quality De−Saturation sensing, high *dV*/*dt* and *dI*/*dt* cross talk noise prevention is importantly in high power application. The De−saturation sensing loop and driving loop should be spilt which can to avoid the cross talk noise into. Figure 44 shows the schematic that is separated the signal bias capacitor $C_{VDD2(S)}$, $C_{VEE2(S)}$ and driving bias capacitor $C_{VDD2(P)}$, $C_{VEE2(P)}$ by ground resistor R_{GND}. This individual sensing trace from IGBT collector to emitter can have a good noise immunity for De−saturation protection. The suggestion of signal capacitors value $C_{VDD2(S)}$ and $C_{VEE2(S)}$ are 1.0 μF at least, driving capacitor value $C_{VDD2(P)}$ and $C_{VEE2(P)}$ are 10 μF at least, and ground resistor value R_{GND} is 4.7Ω above. The recommendation layout and placement concepts are shown in Figure 45 (without BJT buffer) and Figure 46 (with BJT buffer).

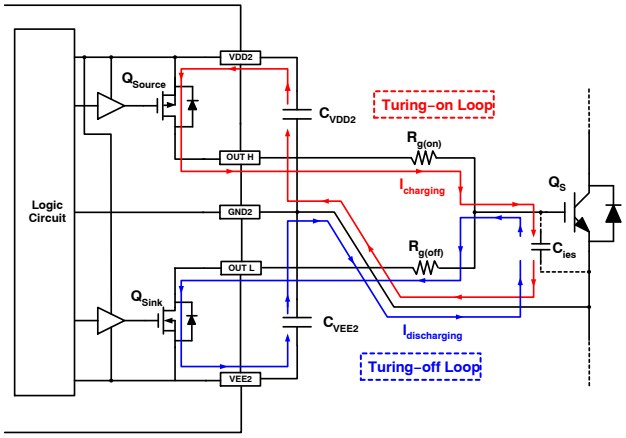


Figure 43. Driving Current Path for Turning−on and Turning−off

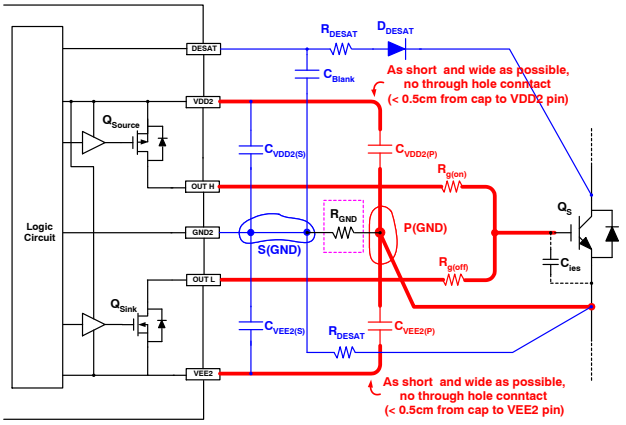


Figure 44. Schematic of Signal and Driving Loop Split

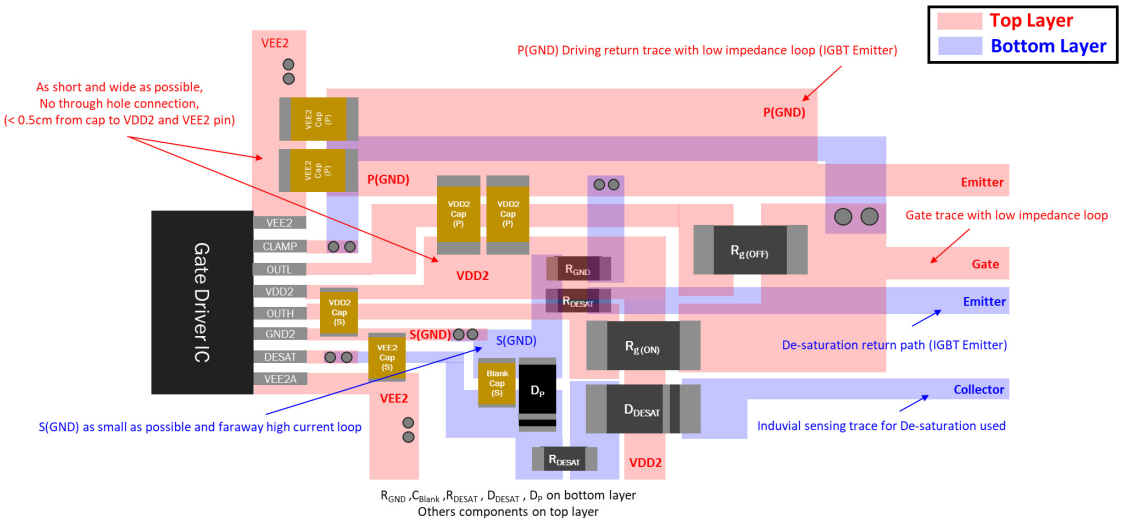


Figure 45. Layout and Placement Concept (without BJT Buffer)

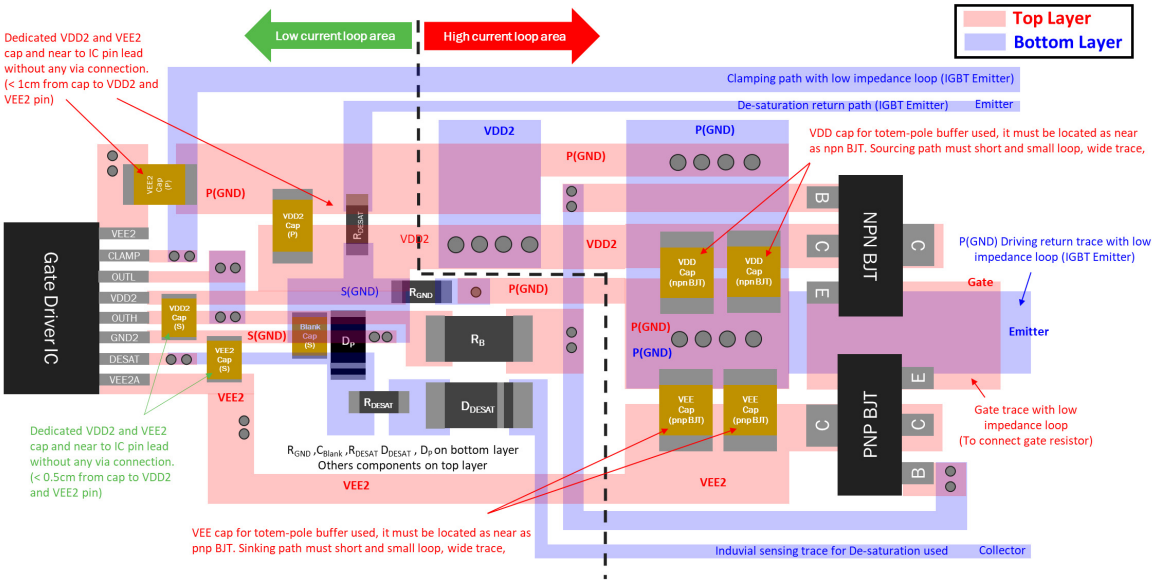


Figure 46. Layout and Placement Concept (with BJT Buffer)

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