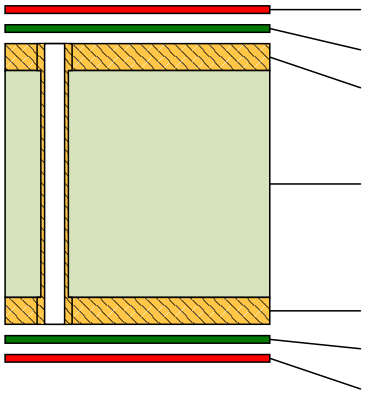
1. Material: Isola IS400 or similar recommended
2. Finish: ENIG (Electroless Nickel Immersion Gold), nickel layer 1 ÷ 4 µm, gold layer 0.076 ÷ 0.2 µm
3. All gerber files generated as a top view
4. Fabricate according IPC-A-600
5. Non-conductive epoxy ink recommended for silkscreen
6. Silkscreen should not cover any exposed copper, silkcreen gerber data have to be trimmed eventually
7. All holes diameter refer to final diameter after eventual plating

Gerber and drill file extensions table

Gerber files	Description
.GTO	Top side silkscreen
.GTP	Top side solder paste mask
.GTS	Top side solder mask
.GTL	L1_TOP - Top Layer
.GBL	L2_BOTTOM - Bottom Layer
.GBS	Bottom side solder mask
.GBP	Bottom side solder paste mask
.GBO	Botom side silkscreen
.GM1	Board outline
Drill files	
.TXT	Layer pair L1_TOP to L2_BOTTOM Layer

DCDC for SiC driver		**Revision: rev 1.0**	**State: released**
PCB fabrication notes and requirements		Fabrication document	Sheet 1 / 13
Engineer: Peter Dubravka	Date: 09/09/2020		
PCB File: DCDC_for_SiC_driver_flyback_NCV3064.PcbDoc		**ON Semiconductor** Solution Engineering Center Piestany	
Repository revision: not in repository revision			

Layer Stack



Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.0102mm(0.400mil)	Solder Resist	Solder Mask	GTS
Copper	Top Layer	0.0711mm(2.800mil)		Signal	GTL
Core		*1.5240mm(60.000mil)*	*FR-4*	*Dielectric*	
Copper	Bottom Layer	0.0711mm(2.800mil)		Signal	GBL
Surface Material	Bottom Solder	0.0102mm(0.400mil)	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

Total thickness: 1.6866mm(66.400mil)

DCDC for SiC driver		**Revision: rev 1.0**	**State: released**
Layer stack details		Fabrication document	Sheet 2 / 13
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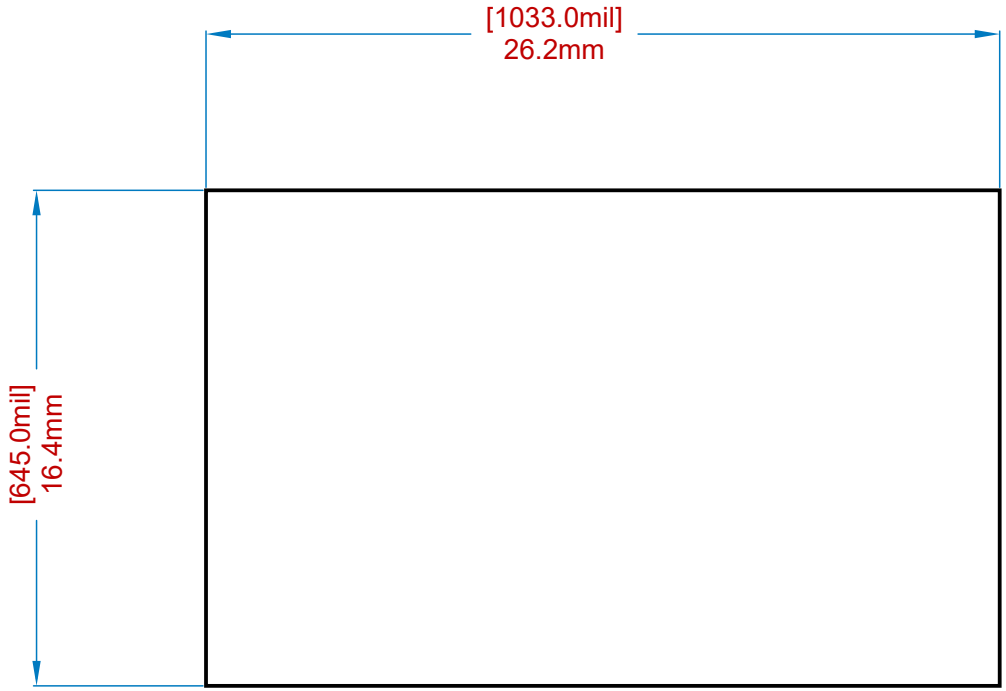

DCDC for SiC driver		Revision: rev 1.0	State: released
Board outline definition - top view 2:3		Fabrication document	Sheet 3 / 13
Engineer: Peter Dubravka	Date: 09/09/2020		
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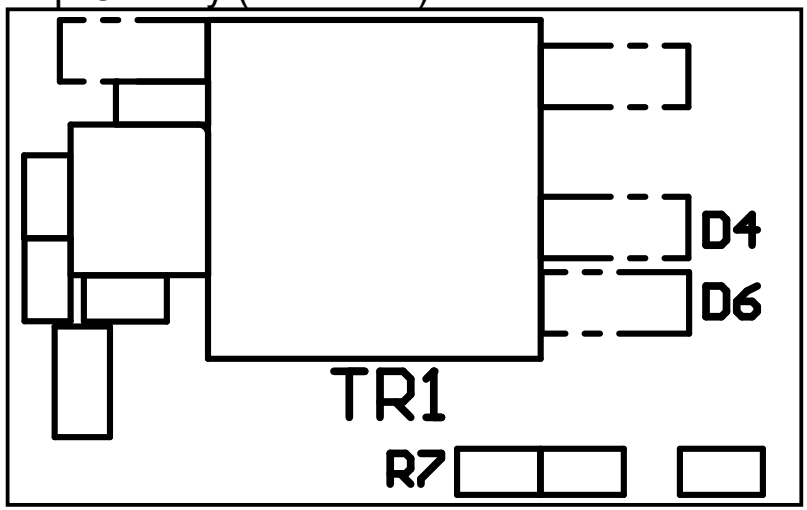
Top Overlay (Scale 4:1)



DCDC for SiC driver		**Revision: rev 1.0**	**State: released**
Top side silkscreen - top view		Fabrication document	Sheet 4 / 13
Engineer: Peter Dubravka	Date: 09/09/2020		
PCB File: DCDC_for_SiC_driver_flyback_NCV3064.PcbDoc		**ON Semiconductor** Solution Engineering Center Piestany	
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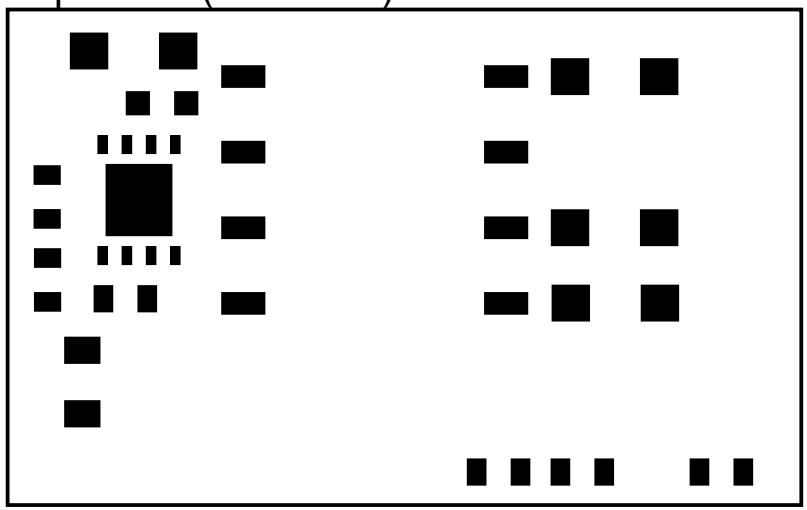
Top Paste (Scale 4:1)



DCDC for SiC driver		**Revision: rev 1.0**	**State: released**
Top side solder paste - top view		Fabrication document	Sheet 5 / 13
Engineer: Peter Dubravka	Date: 09/09/2020		
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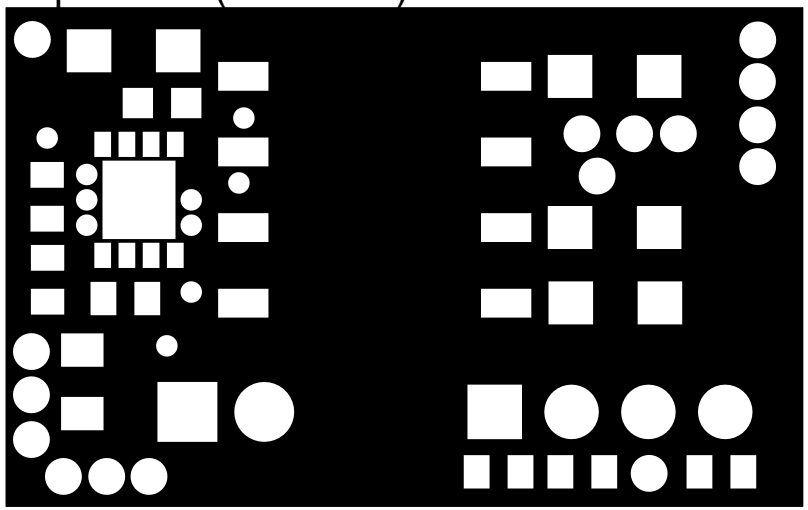
Top Solder (Scale 4:1)



DCDC for SiC driver		**Revision: rev 1.0**	**State: released**
Top side solder mask - top view		Fabrication document	Sheet 6 / 13
Engineer: Peter Dubravka	Date: 09/09/2020		
PCB File: DCDC_for_SiC_driver_flyback_NCV3064.PcbDoc		**ON Semiconductor** Solution Engineering Center Piestany	
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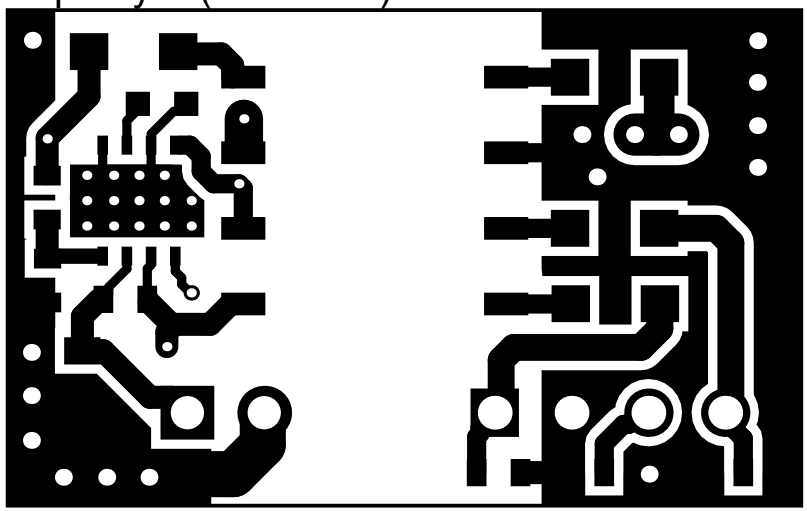
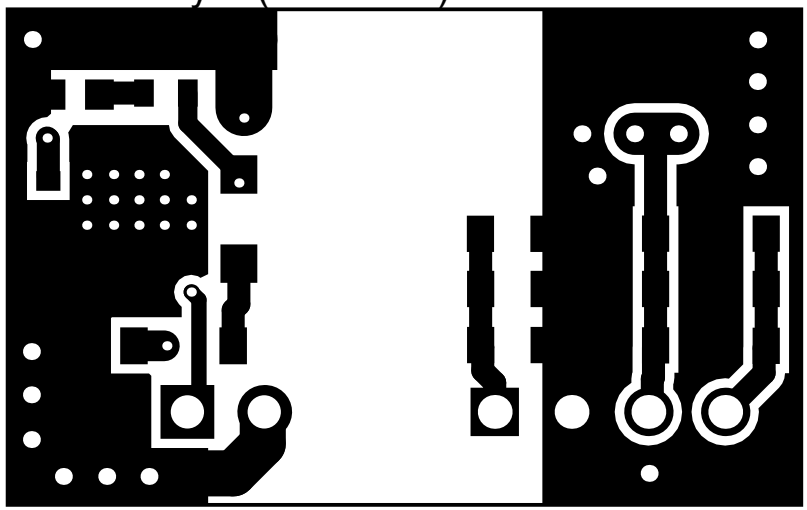
Top Layer (Scale 4:1)



DCDC for SiC driver		**Revision: rev 1.0**	**State: released**
Top Layer - top view		Fabrication document	Sheet 7 / 13
Engineer: Peter Dubravka	Date: 09/09/2020		
PCB File: DCDC_for_SiC_driver_flyback_NCV3064.PcbDoc		**ON Semiconductor** Solution Engineering Center Piestany	
Repository revision: not in repository revision			

Bottom Layer (Scale 4:1)



DCDC for SiC driver		**Revision: rev 1.0**	**State: released**
Bottom Layer - top view		Fabrication document	Sheet 8 / 13
Engineer: Peter Dubravka	Date: 09/09/2020		
PCB File: DCDC_for_SiC_driver_flyback_NCV3064.PcbDoc		**ON Semiconductor** Solution Engineering Center Piestany	
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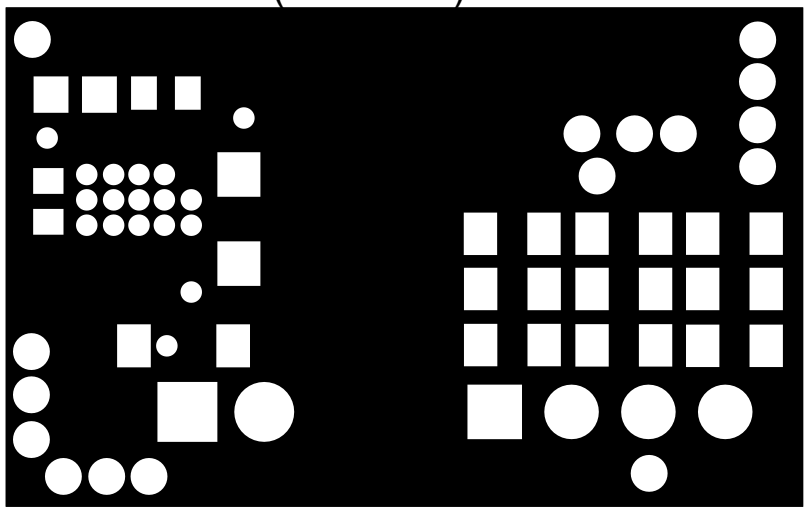
Bottom Solder (Scale 4:1)



DCDC for SiC driver		**Revision: rev 1.0**	**State: released**
Bottom side solder mask - top view		Fabrication document	Sheet 9 / 13
Engineer: Peter Dubravka	Date: 09/09/2020		
PCB File: DCDC_for_SiC_driver_flyback_NCV3064.PcbDoc		**ON Semiconductor** Solution Engineering Center Piestany	
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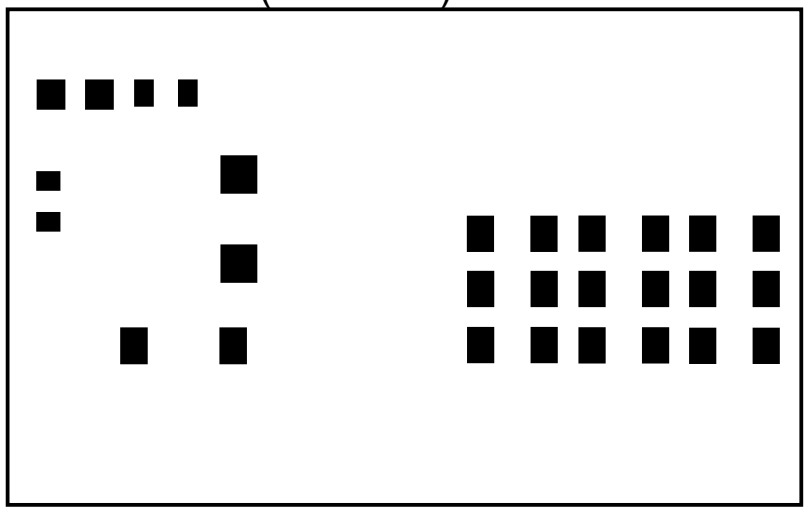
Bottom Paste (Scale 4:1)



DCDC for SiC driver		**Revision: rev 1.0**	**State: released**
Bottom side solder paste - top view		Fabrication document	Sheet 10 / 13
Engineer: Peter Dubravka	Date: 09/09/2020		
PCB File: DCDC_for_SiC_driver_flyback_NCV3064.PcbDoc		**ON Semiconductor** Solution Engineering Center Piestany	
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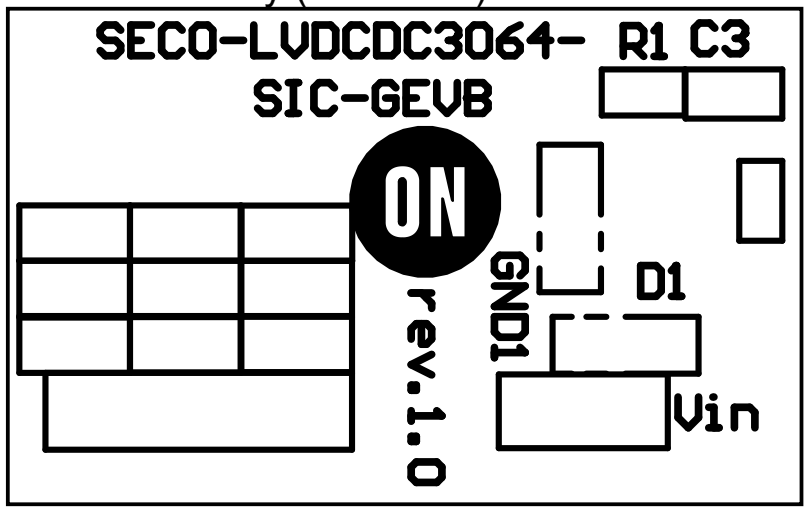
Bottom Overlay (Scale 4:1)



DCDC for SiC driver		**Revision: rev 1.0**	**State: released**
Bottom side silkscreen - bottom view		Fabrication document	Sheet 11 / 13
Engineer: Peter Dubravka	Date: 09/09/2020		
PCB File: DCDC_for_SiC_driver_flyback_NCV3064.PcbDoc		**ON Semiconductor** Solution Engineering Center Piestany	
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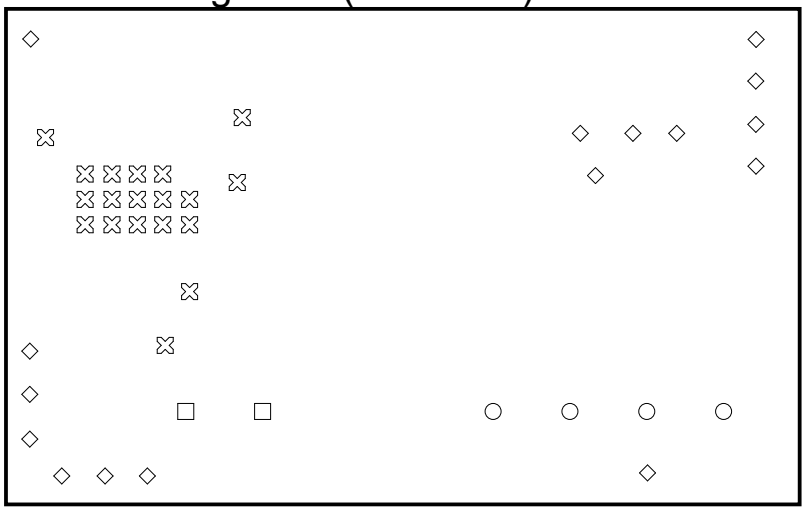
Drill Drawing View (Scale 4:1)



(8) Related drill table can be found on page 13

DCDC for SiC driver		**Revision: rev 1.0**	**State: released**
Drill drawing		Fabrication document	Sheet 12 / 13
Engineer: Peter Dubravka	Date: 09/09/2020		
PCB File: DCDC_for_SiC_driver_flyback_NCV3064.PcbDoc		**ON Semiconductor** Solution Engineering Center Piestany	
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Drill Table

Symbol	Count	Hole Size	Plated	Drill Layer Pair	Via / Pad	Template
⊠	19	0.305mm(12.0mil)	Plated	Top Layer - Bottom Layer	Via	v51h30
◇	16	0.559mm(22.0mil)	Plated	Top Layer - Bottom Layer	Via	v102h56
□	2	1.100mm(43.3mil)	Plated	Top Layer - Bottom Layer	Pad	(Mixed)
○	4	1.118mm(44.0mil)	Plated	Top Layer - Bottom Layer	Pad	(Mixed)
	41 Total					

(9) Related drill drawing can be found on page 12

DCDC for SiC driver		**Revision: rev 1.0**	**State: released**
Drill table		Fabrication document	Sheet 13 / 13
Engineer: Peter Dubravka	Date: 09/09/2020		
PCB File: DCDC_for_SiC_driver_flyback_NCV3064.PcbDoc		**ON Semiconductor** Solution Engineering Center Piestany	
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